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PTO/SB/05 (4/98)

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. MI40-273

First Inventor or Application Identifier James E. O'Toole

Title Method of Speeding Power-Up of an Amplifier, and Amplifier

Express Mail Label No. EL169869536US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 367]
(preferred arrangement set forth below)
 - Descriptive title of the Invention Including Title Page
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 423]
(INFORMAL)
4. Oath or Declaration (3) [Total Pages 16]
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☒ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. ☐ Computer Readable Copy
 - b. ☐ Paper Copy (identical to computer copy)
 - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☒ Information Disclosure (2) ☒ Copies of IDS
Statement (IDS)/PTO-1449 Citations
11. ☒ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ * Small Entity ☐ Statement filed in prior application
Statement(s) Status still proper and desired
(PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☒ Other: Check: Associate Power of Attorney...

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No: 09/152,662

Prior application information: Examiner S. Mottola

Group / Art Unit: 2817

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Registration No. (Attorney/Agent)

33,560

Signature

Deepak Malhotra

Date

February 11, 2000

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EL169869536

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Priority Application Serial No. 09/152,662
3 Priority Filing Date September 14, 1998
4 Inventor James O'Toole et al.
5 Assignee Micron Communications, Inc.
6 Priority Group Art Unit 2817
7 Priority Examiner Steven Mottola
8 Attorney's Docket No. MI40-168
9 Title: Radio Frequency Data Communications Device

10 **PRELIMINARY AMENDMENT**

11 To: Assistant Commissioner for Patents
12 Washington, D.C. 20231

13 From: Deepak Malhotra (Tel. 509-624-4276; Fax 509-838-3424)
14 Wells, St. John, Roberts, Gregory & Matkin P.S.
15 601 W. First Avenue, Suite 1300
16 Spokane, WA 99201-3828

17 **AMENDMENTS**

18 **In the Title**

19 Please change the title to --METHOD OF SPEEDING POWER-UP
20 OF AN AMPLIFIER, AND AMPLIFIER--

21 **In the Specification**

22 Page 1, after the title, please insert:

23 **--CROSS REFERENCE TO RELATED APPLICATION**

 This is a Continuation of U.S. Patent Application Serial No.
 09/152,662, filed September 14, 1998, and titled "Radio Frequency Data

1 Communications Device" (incorporated herein by reference), which in
2 turn is a Division of U.S. Patent Application Serial No. 08/705,043, filed
3 August 29, 1996 (incorporated herein by reference), which in turn claims
4 priority from U.S. Provisional application Serial No. 60/017,900, filed May
5 13, 1996.--

6 Page 42, line 7, after "functions." insert --Fig. 69 is a logic circuit
7 diagram illustrating a logic circuit derived using the Karnaugh map of
8 Fig. 67. Fig 70 is a logic diagram circuit illustrating a logic circuit
9 derived using the Karnaugh map of Fig. 68.--

10 Page 59, line 3, replace "©;" with --(c);--.

11 Page 86, line 24, after "as inventors," insert --now U.S. Patent No.
12 5,432,027;--.

13 Page 87, line 2, after "as inventor," insert --now U.S. Patent No.
14 5,494,495;--.

15 Page 87, line 5, after "as inventor," insert --now U.S. Patent No.
16 5,662,718.--.

17 Page 89, line 4, after "Communications System" insert --now
18 abandoned,--.

19 Page 89, line 6, after "Communications System" insert --now U.S.
20 Patent No. 5,790,946;--.

21 Page 89, line 7, after "Frequency Control" insert --now U.S. Patent
22 No. 5,568,512;--.

1 Page 89, line 18, replace "now allowed" with --now U.S. Patent
2 No. 5,539,775.--.

3 Page 137, line 23, after "as inventors," insert --now U.S. Patent
4 No. 5,480,834--.

5 Page 185, line 2, change "show" to --shown--.

6 Page 188, line 20, after "diagram" insert --(see Figs. 69 and 70)--.

7
8 In the Claims

9 Cancel claims 1-252 in favor of new claims as follows.

10
11 --253. An amplifier configured to be powered by a selectively
12 engageable voltage source, the amplifier comprising:

13 a differential amplifier having first and second inputs for receiving
14 an input signal to be amplified, and having an output;

15 first resistances between the voltage source and respective inputs
16 of the differential amplifier; and

17 second, selectively engageable, resistances between the voltage
18 source and respective inputs of the differential amplifier, the second
19 resistances respectively having smaller resistance values than the first
20 resistances, the second resistances being engaged then disengaged in
21 response to the voltage source being engaged.

1 254. An amplifier in accordance with claim 253 and further
2 comprising coupling capacitors respectively coupled to the first and
3 second inputs.

4
5 255. An amplifier in accordance with claim 253 and further
6 comprising a voltage divider, and wherein the first and second resistances
7 are coupled to the voltage source via the voltage divider.

8
9 256. An amplifier in accordance with claim 253 wherein the first
10 resistances comprise respective transistors.

11
12 257. An amplifier in accordance with claim 253 wherein the first
13 resistances comprise respective p-type transistors.

14
15 258. An amplifier in accordance with claim 253 wherein the
16 second resistances comprise respective transistors.

17
18 259. An amplifier in accordance with claim 253 wherein the
19 second resistances comprise respective p-type transistors.

1 260. A method of speeding power up of an amplifier stage
2 configured to be powered by a voltage source and including a differential
3 amplifier having first and second inputs configured to receive an input
4 signal to be amplified, and having an output; and resistances between the
5 voltage source and respective inputs of the differential amplifier, the
6 method comprising:

7 shorting around the selectively resistances for an amount of time
8 in response to the voltage source being engaged.
9

10 261. A method in accordance with claim 260 wherein the shorting
11 comprises engaging selectively engageable second resistances respectively
12 coupled in parallel with the first mentioned resistances and having
13 respective resistance values lower than the first mentioned resistances.
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1 262. A method of speeding power up of an amplifier stage
2 configured to be powered by a voltage source and including first and
3 second electrodes configured to receive an input signal to be amplified,
4 the input electrodes being adapted to be respectively coupled to coupling
5 capacitors; a differential amplifier having inputs respectively connected to
6 the first and second electrodes, and having an output; and resistances
7 between the voltage source and respective inputs of the differential
8 amplifier, the method comprising:

9 shorting around the resistances for a predetermined amount of time
10 in response to the voltage source being engaged, the shorting comprising
11 engaging selectively engageable second resistances respectively coupled in
12 parallel with the first mentioned resistances and having respective
13 resistance values lower than the first mentioned resistances.

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263. A receiver comprising:

a Schottky diode detector;

an amplifier coupled to the Schottky diode detector and configured to be powered by a selectively engageable voltage source, the amplifier including:

a differential amplifier having first and second inputs coupled to the Schottky diode detector to amplify a signal generated by the Schottky diode detector, and having an output;

first resistances between the voltage source and respective inputs of the differential amplifier; and

second, selectively engageable, resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller resistance values than the first resistances, the second resistances being engaged then disengaged in response to the voltage source being engaged.

264. A receiver in accordance with claim 263 and further comprising coupling capacitors respectively coupled between the Schottky diode detector and the first and second inputs of the differential amplifier.

1 265. A receiver in accordance with claim 263 wherein the
2 amplifier further comprises a voltage divider, and wherein the first
3 mentioned and second resistances are coupled to the voltage source via
4 the voltage divider.

5
6 266. A receiver in accordance with claim 263 wherein the first
7 mentioned resistances of the amplifier comprise respective transistors.

8
9 267. A receiver in accordance with claim 263 wherein the first
10 mentioned resistances of the amplifier comprise respective p-type
11 transistors.

12
13 268. A receiver in accordance with claim 263 wherein the second
14 resistances of the amplifier comprise respective transistors.

15
16 269. A receiver in accordance with claim 263 wherein the second
17 resistances comprise respective p-type transistors.

1 270. A method of speeding power-up of an amplifier stage of a
2 receiver having a Schottky diode detector, the amplifier stage being
3 configured to be powered by a voltage source and including a differential
4 amplifier having first and second inputs configured to receive an input
5 signal to be amplified from the Schottky diode detector, and having an
6 output; and selectively resistances between the voltage source and
7 respective inputs of the differential amplifier, the method comprising:

8 shorting around the resistances for an amount of time in response
9 to the voltage source being engaged.
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11 271. A method in accordance with claim 270 wherein the shorting
12 comprises engaging selectively engageable second resistances respectively
13 coupled in parallel with the first mentioned resistances and having
14 respective resistance values lower than the first mentioned resistances.
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1 272. A method of speeding power up of an amplifier stage of a
2 receiver having a Schottky diode detector, the amplifier stage being
3 configured to be powered by a voltage source and including first and
4 second electrodes configured to receive an input signal to be amplified,
5 the input electrodes being adapted to be respectively coupled to the
6 Schottky diode detector by coupling capacitors to amplify a signal
7 generated by the Schottky diode detector; the amplifier stage further
8 including a differential amplifier having inputs respectively connected to
9 the first and second electrodes, and having an output; and selectively
10 engageable resistances between the voltage source and respective inputs
11 of the differential amplifier, the method comprising:

12 shorting around the selectively engageable resistances for a
13 predetermined amount of time in response to the voltage source being
14 engaged, the shorting comprising engaging selectively engageable second
15 resistances respectively coupled in parallel with the first mentioned
16 resistances and having respective resistance values lower than the first
17 mentioned resistances.

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273. A receiver comprising:

an RF detector;

an amplifier coupled to the RF detector and configured to be powered by a selectively engageable voltage source, the amplifier including:

a differential amplifier having first and second inputs coupled to the Schottky diode detector to amplify a signal generated by the Schottky diode detector, and having an output;

first resistances between the voltage source and respective inputs of the differential amplifier; and

second, selectively engageable, resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller resistance values than the first resistances, the second resistances being engaged then disengaged in response to the voltage source being engaged.

274. A receiver in accordance with claim 273 wherein the RF detector comprises a Schottky diode detector.

275. A receiver in accordance with claim 273 wherein the second resistances comprise transistors.

1 276. An amplifier configured to be powered by a selectively
2 engageable voltage source, the amplifier comprising:

3 a differential amplifier having first and second inputs for receiving
4 an input signal to be amplified, and having an output;

5 a first resistance between the voltage source and the first input of
6 the differential amplifier;

7 a second resistance between the voltage source and the second
8 input of the differential amplifier;

9 a third, selectively engageable, resistance between the voltage
10 source and the first input of the differential amplifier, the third
11 resistance having a smaller resistance value than the first resistance; and

12 a fourth, selectively engageable, resistance between the voltage
13 source and the first input of the differential amplifier, the fourth
14 resistance having a smaller resistance value than the first resistance, the
15 third and fourth resistances being engaged then disengaged in response
16 to the voltage source being engaged.

17
18 277. An amplifier in accordance with claim 276 wherein the third
19 and fourth resistances are simultaneously engaged then disengaged in
20 response to the voltage source being engaged.

21
22 278. An amplifier in accordance with claim 276 wherein the first
23 resistance comprises a transistor.

1 279. An amplifier in accordance with claim 278 wherein the
2 second resistance comprises a transistor.

3
4 280. An amplifier in accordance with claim 276 wherein the third
5 resistance comprises a transistor.

6
7 281. An amplifier in accordance with claim 280 wherein the fourth
8 resistance comprises a transistor.

9
10 282. A method of speeding power up of an amplifier stage
11 configured to be powered by a voltage source and including a differential
12 amplifier having first and second inputs configured to receive an input
13 signal to be amplified, and having an output, a first resistance between
14 the voltage source and the first input of the differential amplifier, and
15 a second resistance between the voltage source and the second input of
16 the differential amplifier, the method comprising:

17 simultaneously shorting around the first and second resistances for
18 an amount of time in response to the voltage source being engaged.

1 283. An amplifier configured to be powered by a selectively
2 engageable voltage source, the amplifier comprising:

3 a differential amplifier having first and second inputs for receiving
4 an input signal to be amplified, and having an output;

5 a first resistance between the voltage source and the first input of
6 the differential amplifier;

7 a second resistance between the voltage source and the second
8 input of the differential amplifier;

9 circuitry configured to switch around the third and fourth
10 resistances for a predetermined amount of time, to cause the inputs to
11 the differential amplifier to come up to a bias voltage more quickly, in
12 response to the voltage source being engaged.

13
14 284. An amplifier in accordance with claim 283 wherein the
15 circuitry configured to switch around the third and fourth resistances
16 comprises respective transistors.

17
18 285. An amplifier in accordance with claim 284 wherein the first
19 resistance comprises a transistor.

20
21 286. An amplifier in accordance with claim 285 wherein the
22 second resistance comprises a transistor.

23

1 287. A method of speeding power up of an amplifier stage
2 configured to be powered by a voltage source and including a differential
3 amplifier having first and second inputs configured to receive an input
4 signal to be amplified, and having an output, a first resistance between
5 the voltage source and the first input of the differential amplifier, and
6 a second resistance between the voltage source and the second input of
7 the differential amplifier, the method comprising:

8 simultaneously switching around the first and second resistances for
9 a predetermined amount of time in response to the voltage source being
10 engaged.--
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REMARKS

This preliminary amendment accompanies a request for continuation of allowed patent application Serial No. 09/152,662.


The specification has been amended to provide a cross reference to the parent application, and to make various other amendments that were made and approved during prosecution of the parent application.

The new claims are similar to, but different from, claims allowed in the parent application.

Examination on the merits is requested. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: February 11, 2000

By: 
Deepak Malhotra
Reg. No. 33,560

IN THE UNITED STATES' PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

RADIO FREQUENCY DATA COMMUNICATIONS
DEVICE

* * * *

INVENTORS

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ATTORNEY'S DOCKET NO. MI40-030

EL 169869536

EL 169833885

RADIO FREQUENCY DATA COMMUNICATIONS DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Application 60/017,900, filed May 13, 1996, titled "Radio Frequency Data Communication Device."

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REFERENCE TO MICROFICHE

Appended hereto is a microfiche copy of a software guide entitled "Micron RFID Systems Developer's Guide," May 2, 1996. This appendix has 5 microfiche providing 266 total frames.

TECHNICAL FIELD

This invention relates to radio frequency communication devices. More particularly, the invention relates to radio frequency identification

1 devices for inventory control, object monitoring, or for determining the
2 existence, location or movement of objects.

3 4 BACKGROUND OF THE INVENTION

5 As large numbers of objects are moved in inventory, product
6 manufacturing, and merchandising operations, there is a continuous
7 challenge to accurately monitor the location and flow of objects.
8 Additionally, there is a continuing goal to interrogate the location of
9 objects in an inexpensive and streamlined manner. Furthermore, there
10 is a need for tag devices suitably configured to mount to a variety of
11 objects including goods, items, persons, or animals, or substantially any
12 moving or stationary and animate or inanimate object. One way of
13 tracking objects is with an electronic identification system.

14 One presently available electronic identification system utilizes a
15 magnetic field modulation system to monitor tag devices. An
16 interrogator creates a magnetic field that becomes detuned when the tag
17 device is passed through the magnetic field. In some cases, the tag
18 device may be provided with a unique identification code in order to
19 distinguish between a number of different tags. Typically, the tag
20 devices are entirely passive (have no power supply), which results in a
21 small and portable package. However, this identification system is only
22 capable of distinguishing a limited number of tag devices, over a
23 relatively short range, limited by the size of a magnetic field used to
24 supply power to the tags and to communicate with the tags.

Another electronic identification system utilizes an RF transponder device affixed to an object to be monitored, in which an interrogator transmits an interrogation signal to the device. The device receives the signal, then generates and transmits a responsive signal. The interrogation signal and the responsive signal are typically radio-frequency (RF) signals produced by an RF transmitter circuit. Since RF signals can be transmitted over greater distances than magnetic fields, RF-based transponder devices tend to be more suitable for applications requiring tracking of a tagged device that may not be in close proximity to an interrogator. For example, RF-based transponder devices tend to be more suitable for inventory control or tracking.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings. Like names for circuit blocks indicate like components. Where there are a plurality of identical circuit blocks, detailed drawings are provided for one such circuit block. Some circuit schematics have been numbered in a hierarchial manner to reflect the hierarchial nature of these drawings. Notwithstanding the order in which the figures are numbered, note that some detailed drawings provide details to blocks included in more than one higher level drawing. Some circuit schematics have been broken up into many portions due to size requirements for patent drawings.

1 Fig. 1 is a high level circuit schematic showing a circuit
2 embodying the invention.

3 Fig. 2 is a front view of an employee badge according to but one
4 embodiment the invention.

5 Fig. 3 is a front view of a radio frequency identification tag
6 according to another embodiment of the invention.

7 Fig. 4 is a block diagram of an electronic identification system
8 according to the invention and including an interrogator and the tag of
9 Fig. 3.

10 Fig. 5 is a high level circuit schematic of a monolithic
11 semiconductor integrated circuit utilized in the devices of Figs. 1-4.

12 Fig. 6 is a graph illustrating how Figs. 6AA-EK are to be
13 assembled. After such assembly, Figs. 6AA-EK provide a circuit
14 drawing of another high level circuit schematic of the monolithic
15 semiconductor integrated circuit of Fig. 5, showing pads and other
16 details.

17 Fig. 6.01 is a layout diagram illustrating the physical layout of
18 various components on an integrated circuit die, in accordance with one
19 embodiment of the invention. The physical locations and sizes of
20 components relative to other components are shown. Boundaries
21 between various blocks may be approximate in the sense that portions
22 of certain blocks may extend into other blocks.

1 Fig. 7 is a graph illustrating how Figs. 7AA-HJ are to be
2 assembled. After such assembly, Figs. 7AA-HJ provide a circuit drawing
3 of a data processor "dataproc" included in the circuit of Figs. 6AA-EK.

4 Fig. 7.01 is a graph illustrating how Figs. 7.01AA-BB are to
5 be assembled. After such assembly, Figs. 7.01AA-BB provide a circuit
6 drawing of a processor clock generator "clk" included in the circuit of
7 Figs. 7AA-HJ.

8 Fig. 7.0101 is a graph illustrating how Figs.
9 7.0101AA-BB are to be assembled. After such assembly, Figs.
10 7.0101AA-BB provide a circuit drawing of a processor clock controller
11 "clkctl" included in the circuit of Figs. 7.01AA-BB.

12 Fig. 7.0102 is a graph illustrating how Figs.
13 7.0102AE-DJ are to be assembled. After such assembly, Figs.
14 7.0102AE-DJ provide a circuit drawing of a phase generator "clkph"
15 included in the circuit of Figs. 7.01AA-BB.

16 Fig. 7.0103 is a graph illustrating how Figs.
17 7.0103AA-BD are to be assembled. After such assembly, Figs.
18 7.0103AA-BD provide a circuit drawing of a state generator "clkst"
19 included in the circuit of Figs. 7.01AA-BB.

20 Fig. 7.010301 is a graph illustrating how Figs.
21 7.010301AA-BB are to be assembled. After such assembly, Figs.
22 7.010301AA-BB provide a circuit drawing of a clock generator counter
23 bit "clkcbt" included in the circuit of Figs. 7.0103AA-BD.

1 Fig. 7.02 is a graph illustrating how Figs. 7.02AA-BF are to
2 be assembled. After such assembly, Figs. 7.02AA-BF provide a circuit
3 drawing of an address decoder "adrdec" included in the circuit of
4 Figs. 7AA-BF.

5 Fig. 7.03 is a graph illustrating how Figs. 7.03AA-EH are
6 to be assembled. After such assembly, Figs. 7.03AA-EH provide a
7 circuit drawing of a 512 byte RAM "ram" included in the circuit of
8 Figs. 7AA-HJ.

9 Fig. 7.0301 is a graph illustrating how Figs.
10 7.0301AA-BB are to be assembled. After such assembly, Figs.
11 7.0301AA-BB provide a circuit drawing of a RAM control circuit
12 "ramctl" included in the circuit of Figs. 7.03AA-BB.

13 Fig. 7.0302 is a graph illustrating how Figs.
14 7.0302AA-AC are to be assembled. After such assembly, Figs.
15 7.0302AA-AC provide a circuit drawing of an 8x4 RAM array "ram8x4"
16 included in the circuit of Figs. 7.03AA-EH.

17 Fig. 7.030201 is a circuit drawing of a six
18 transistor RAM cell "ramcell" included in the circuit of
19 Figs. 7.0302AA-AC.

20 Fig. 7.0303 is a graph illustrating how Figs.
21 7.0303AA-AD are to be assembled. After such assembly, Figs.
22 7.0303AA-AD provide a circuit drawing of a RAM precharge circuit
23 "rampch" included in the circuit of Figs. 7.03AA-EH.
24

1 Fig. 7.0304 is a graph illustrating how Figs.
2 7.0304AA-AD are to be assembled. After such assembly, Figs.
3 7.0304AA-AD provide a circuit drawing of a second RAM precharge
4 circuit "ramdch" included in the circuit of Figs. 7.03AA-EH.

5 Fig. 7.0305 is a circuit drawing of a RAM address
6 buffer "ramadb" included in the circuit of Figs. 7.03AA-EH.

7 Fig. 7.0306 is a graph illustrating how Figs.
8 7.0306AA-BA are to be assembled. After such assembly, Figs.
9 7.0306AA-BA provide a circuit drawing of a RAM word line driver
10 "ramwdr" included in the circuit of Figs. 7.03AA-EH.

11 Fig. 7.0307 is a graph illustrating how Figs.
12 7.0307AA-BB are to be assembled. After such assembly, Figs.
13 7.0307AA-BB provide a circuit drawing of a RAM word line decoder
14 "ramwdec" included in the circuit of Figs. 7.03AA-EH.

15 Fig. 7.0308 is a graph illustrating how Figs.
16 7.0308AA-BB are to be assembled. After such assembly, Figs.
17 7.0308AA-BB provide a circuit drawing of a RAM column select decode
18 circuit "ramcdec" included in the circuit of Figs. 7.03AA-EH.

19 Fig. 7.0309 is a graph illustrating how Figs.
20 7.0309AA-BG are to be assembled. After such assembly, Figs.
21 7.0309AA-BG provide a circuit drawing of a RAM column selector
22 "ramcsel" included in the circuit of Figs. 7.03AA-EH.

23 Fig. 7.0310 is a graph illustrating how Figs.
24 7.0310AA-BB are to be assembled. After such assembly, Figs.

1 7.0310AA-BB provide a circuit drawing of a RAM databus interface
2 "ramdb" included in the circuit of Figs. 7.03AA-EH.

3 Fig. 7.04 is a graph illustrating how Figs. 7.04AA-HJ are to
4 be assembled. After such assembly, Figs. 7.04AA-HJ provide a circuit
5 drawing of a ROM "rom" included in the circuit of Figs. 7AA-HJ.

6 Fig. 7.0401 is a graph illustrating how Figs.
7 7.0401AA-BB are to be assembled. After such assembly, Figs.
8 7.0401AA-BB provide a circuit drawing of a ROM control logic circuit
9 "romctl" included in the circuit of Figs. 7.04AA-HJ.

10 Fig. 7.0402 is a graph illustrating how Figs.
11 7.0402AA-AB are to be assembled. After such assembly, Figs.
12 7.0402AA-AB provide a circuit drawing of a ROM bit line precharge
13 circuit "rompch" included in the circuit of Figs. 7.04AA-HJ.

14 Fig. 7.0403 is a graph illustrating how Figs.
15 7.0403AA-BB are to be assembled. After such assembly, Figs.
16 7.0403AA-BB provide a circuit drawing of a ROM word line driver
17 "romwdr" included in the circuit of Figs. 7.04AA-HJ.

18 Fig. 7.0404 is a graph illustrating how Figs.
19 7.0404AB-DC are to be assembled. After such assembly, Figs.
20 7.0404AA-DC provide a circuit drawing of a ROM word block decoder
21 "romwdec_rev" included in the circuit of Figs. 7.04AA-HJ.

22 Fig. 7.0405 is a graph illustrating how Figs.
23 7.0405AA-BA are to be assembled. After such assembly, Figs.
24

1 7.0405AA-BA provide a circuit drawing of a ROM bit line address
2 driver "rombldr" included in the circuit of Figs. 7.04AA-HJ.

3 Fig. 7.0406 is a graph illustrating how Figs.
4 7.0406AA-CK are to be assembled. After such assembly, Figs.
5 7.0406AA-CK provide a circuit drawing of a ROM bit line decoder
6 "rombldec" included in the circuit of Figs. 7.04AA-HJ.

7 Fig. 7.0407 is a graph illustrating how Figs.
8 7.0407AA-AB are to be assembled. After such assembly, Figs.
9 7.0407AA-AB provide a circuit drawing of a ROM sense amplifier
10 "romsns" included in the circuit of Figs. 7.04AA-HJ.

11 Fig. 7.05 is a graph illustrating how Figs. 7.05AA-CB are to
12 be assembled. After such assembly, Figs. 7.05AA-CB provide a circuit
13 drawing of an instruction register "insreg" included in the circuit of
14 Figs. 7AA-HJ.

15 Fig. 7.0501 is a graph illustrating how Figs.
16 7.0501AA-AB are to be assembled. After such assembly, Figs.
17 7.0501AA-AB provide a circuit drawing of an instruction register cell
18 "insrcel" included in the circuit of Figs. 7.05AA-CB.

19 Fig. 7.06 is a graph illustrating how Figs. 7.06AA-CN are
20 to be assembled. After such assembly, Figs. 7.06AA-CN provide a
21 circuit drawing of an instruction decoder PLA "insdec" included in the
22 circuit of Figs. 7AA-HJ.

23 Fig. 7.0601 is a graph illustrating how Figs.
24 7.0601AA-HI are to be assembled. After such assembly, Figs.

1 7.0601AA-HI provide a circuit drawing of an instruction decoder
2 "insdec1" included in the circuit of Figs. 7AA-HJ.

3 Fig. 7.0602 is a graph illustrating how Figs.
4 7.0602AA-JH are to be assembled. After such assembly, Figs.
5 7.0602AA-JH provide a circuit drawing of an instruction decoder (second
6 section) "insdec2" included in the circuit of Figs. 7AA-HJ.

7 Fig. 7.0603 is a graph illustrating how Figs.
8 7.0603AA-JI are to be assembled. After such assembly, Figs.
9 7.0603AA-JI provide a circuit drawing of an instruction decoder (third
10 section) "insdec3" included in the circuit of Figs. 7AA-HJ.

11 Fig. 7.0604 is a graph illustrating how Figs.
12 7.0604AA-JI are to be assembled. After such assembly, Figs.
13 7.0604AA-JI provide a circuit drawing of an instruction decoder (fourth
14 section) "insdec4" included in the circuit of Figs. 7AA-HJ.

15 Fig. 7.060401 is a circuit drawing of an
16 instruction decoder ROM amp "insramp" included in the circuit of
17 Figs. 7.0604AA-JI.

18 Fig. 7.060402 is a circuit drawing of an
19 instruction decoder PLA amp "inspamp" included in the circuit of
20 Figs. 7.0604AA-JI.

21 Fig. 7.060403 is a circuit drawing of an
22 instruction decoder PLA latch "insplat" included in the circuit of
23 Figs. 7.0604AA-JI.

1 Fig. 7.07 is a graph illustrating how Figs. 7.07AA-BB are to
2 be assembled. After such assembly, Figs. 7.07AA-BB provide a circuit
3 drawing of a conditional qualifier decoder "cqualdec" included in the
4 circuit of Figs. 7AA-HJ.

5 Fig. 7.08 is a graph illustrating how Figs. 7.08AA-CA are
6 to be assembled. After such assembly, Figs. 7.08AA-CA provide a
7 circuit drawing of a databus latch/precharge circuit "dblatch" included in
8 the circuit of Figs. 7AA-HJ.

9 Fig. 7.09 is a graph illustrating how Figs. 7.09AA-BF are to
10 be assembled. After such assembly, Figs. 7.09AA-BF provide a circuit
11 drawing of an arithmetic logic unit "alu" included in the circuit of
12 Figs. 7AA-HJ.

13 Fig. 7.0901 is a graph illustrating how Figs.
14 7.0901AA-CE are to be assembled. After such assembly, Figs.
15 7.0901AA-CE provide a circuit drawing of an ALU low byte "alubyt1"
16 included in the circuit of Figs. 7.09AA-BF.

17 Fig. 7.090101 is a graph illustrating how Figs.
18 7.090101AA-AD are to be assembled. After such assembly, Figs.
19 7.090101AA-AD provide a circuit drawing of a bit "alubit1" included in
20 the circuit of Figs. 7.0901AA-CE.

21 Fig. 7.09010101 is a circuit drawing of an
22 ALU bit decoder cell "alubdec" included in the circuit of
23 Figs. 7.090101AA-AD.

1 Fig. 7.09010102 is a circuit drawing of an
2 ALU B register cell "alubcell" included in the circuit of
3 Figs. 7.090101AA-AD.

4 Fig. 7.09010103 is a graph illustrating how
5 Figs. 7.09010103AA-AB are to be assembled. After such assembly, Figs.
6 7.09010103AA-AB provide a circuit drawing of an ALU A register cell
7 "aluacell" included in the circuit of Figs. 7.090101AA-AD.

8 Fig. 7.09010104 is a graph illustrating how
9 Figs. 7.09010104AA-AB are to be assembled. After such assembly, Figs.
10 7.09010104AA-AB provide a circuit drawing of an ALU register cell
11 "alupc" included in the circuit of Figs. 7.090101AA-AD.

12 Fig. 7.09010105 is a circuit drawing of an
13 ALU register cell "alurcell" included in the circuit of Figs. 7.090101AA-
14 AD. Such register cells are used for a stack pointer and data pointer.

15 Fig. 7.09010106 is a graph illustrating how
16 Figs. 7.09010106AA-AB are to be assembled. After such assembly, Figs.
17 7.09010106AA-AB provide a circuit drawing of an ALU memory address
18 register "alumar" included in the circuit of Figs. 7.090101AA-AD.

19 Fig. 7.09010107 is a circuit drawing of an
20 ALU slave cell "aluslave" included in the circuit of Figs. 7.090101AA-
21 AD.

22 Fig. 7.09010108 is a graph illustrating how
23 Figs. 7.09010108AA-BC are to be assembled. After such assembly, Figs.
24

1 7.09010108AA-BC provide a circuit drawing of an ALU adder "aluadd"
2 included in the circuit of Figs. 7.090101AA-AD.

3 Fig. 7.0902 is a graph illustrating how Figs.
4 7.0902AA-BD are to be assembled. After such assembly, Figs.
5 7.0902AA-BD provide a circuit drawing of an ALU high byte "alubyth"
6 included in the circuit of Figs. 7.09AA-BF.

7 Fig. 7.090201 is a graph illustrating how Figs.
8 7.090201AA-AC are to be assembled. After such assembly, Figs.
9 7.090201AA-AC provide a circuit drawing of a bit "alubith" included in
10 the circuit of Figs. 7.09AA-BF.

11 Fig. 7.10 is a graph illustrating how Figs. 7.10AA-CC are
12 to be assembled. After such assembly, Figs. 7.10AA-CC provide a
13 circuit drawing of a timed lockout divider "tld" included in the circuit
14 of Figs. 7AA-HJ.

15 Fig. 7.1001 is a circuit drawing of a timed lockout
16 divider cell "tldcel" included in the circuit of Figs. 7.10AA-CC.

17 Fig. 7.11 is a graph illustrating how Figs. 7.11AA-AB are
18 to be assembled. After such assembly, Figs. 7.11AA-AB provide a
19 circuit drawing of a timed lockout register "tlorege" included in the
20 circuit of Figs. 7AA-HJ.

21 Fig. 7.1101 is a graph illustrating how Figs.
22 7.1101AA-AC are to be assembled. After such assembly, Figs.
23 7.1101AA-AC provide a circuit drawing of a timed lockout register cell
24 "tlorcel" included in the circuit of Figs. 7.11AA-AB.

1 Fig. 7.12 is a graph illustrating how Figs. 7.12AA-AC are
2 to be assembled. After such assembly, Figs. 7.12AA-AC provide a
3 circuit drawing of a R/W control register "oreg" included in the circuit
4 of Figs. 7AA-HJ.

5 Fig. 7.1201 is a circuit drawing of a R/W control
6 register cell "regcell" included in the circuit of Figs. 7.12AA-AC.

7 Fig. 7.13 is a graph illustrating how Figs. 7.13AA-BA are
8 to be assembled. After such assembly, Figs. 7.13AA-BA provide a
9 circuit drawing of a status register "sreg" included in the circuit of
10 Figs. 7AA-HJ.

11 Fig. 7.1301 is a circuit drawing of a status register
12 cell "sregcel" included in the circuit of Figs. 7.13AA-BA.

13 Fig. 7.14 is a graph illustrating how Figs. 7.14AA-AB are
14 to be assembled. After such assembly, Figs. 7.14AA-AB provide a
15 circuit drawing of a serial input/output block "sio" included in the circuit
16 of Figs. 7AA-HJ.

17 Fig. 7.1401 is a graph illustrating how Figs. 7.1401AA-
18 GF are to be assembled. After such assembly, Figs. 7.1401AA-GF
19 provide a circuit drawing of a serial input/output data path "siodata"
20 included in the circuit of Figs. 7.14AA-AB.

21 Fig. 7.140101 is a graph illustrating how Figs.
22 7.140101AA-AB are to be assembled. After such assembly, Figs.
23 7.140101AA-AB provide a circuit drawing of a serial input/output register
24 cell "sioreg" included in the circuit of Figs. 7.1401AA-AB.

1 Fig. 7.140102 is a circuit drawing of a serial
2 input/output XOR circuit "sioxor" included in the circuit of
3 Figs. 7.1401AA-GF.

4 Fig. 7.140103 is a graph illustrating how Figs.
5 7.140103AA-AB are to be assembled. After such assembly, Figs.
6 7.140103AA-AB provide a circuit drawing of a bidirectional latch
7 "siobdlat_inv" included in the circuit of Figs. 7.1401AA-GF.

8 Fig. 7.140104 is a graph illustrating how Figs.
9 7.140104AA-AB are to be assembled. After such assembly, Figs.
10 7.140104AA-AB provide a circuit drawing of a shift register "sioshr"
11 included in the circuit of Figs. 7.1401AA-GF.

12 Fig. 7.140105 is a graph illustrating how Figs.
13 7.140105AA-AB are to be assembled. After such assembly, Figs.
14 7.140105AA-AB provide a circuit drawing of a bidirectional latch
15 "siobdlat" included in the circuit of Figs. 7.1401AA-GF.

16 Fig. 7.1402 is a graph illustrating how Figs. 7.1402BA-
17 EI are to be assembled. After such assembly, Figs. 7.1402BA-EI
18 provide a circuit drawing of serial input/output control logic "sioctl"
19 included in the circuit of Figs. 7.14AA-AB.

20 Fig. 7.140201 is a graph illustrating how Figs.
21 7.140201AA-BB are to be assembled. After such assembly, Figs.
22 7.140201AA-BB provide a circuit drawing of a counter bit "siocbit"
23 included in the circuit of Figs. 7.1402AA-AB
24

1 Fig. 7.15 is a graph illustrating how Figs. 7.15AA-EC are
2 to be assembled. After such assembly, Figs. 7.15AA-EC provide a
3 circuit drawing of a data interleaver (which interleaves two thirteen bit
4 words) "dil" included in the circuit of Figs. 7AA-HJ.

5 Fig. 7.1501 is a graph illustrating how Figs. 7.1501AA-
6 CA are to be assembled. After such assembly, Figs. 7.1501AA-CA
7 provide a circuit drawing of a data interleaver shift register "dil_sreg"
8 included in the circuit of Figs. 7.15AA-EC.

9 Fig. 7.1502 is a graph illustrating how Figs. 7.1502AA-
10 CA are to be assembled. After such assembly, Figs. 7.1502AA-CA
11 provide a circuit drawing of a data interleaver shift register with
12 parallel load "dil_plsreg" included in the circuit of Figs. 7.15AA-EC.

13 Fig. 7.150201 is a circuit drawing of a data
14 interleaver shift register bit "dil_sregbit" included in the circuit of
15 Figs. 7.1502AA-CA.

16 Fig. 7.16 is a graph illustrating how Figs. 7.16AA-CD are
17 to be assembled. After such assembly, Figs. 7.16AA-CD provide a
18 circuit drawing of a convolutional encoder and preamble generator
19 "conv" included in the circuit of Figs. 7AA-HJ.

20 Fig. 7.1601 is a circuit drawing of a shift register cell
21 "convshr" included in the circuit of Figs. 7.16AA-CD.

22 Fig. 7.1602 is a circuit drawing of a summer "convsum"
23 included in the circuit of Figs. 7.16AA-CD.
24

1 Fig. 7.17 is a graph illustrating how Figs. 7.17AA-BB are to
2 be assembled. After such assembly, Figs. 7.17AA-BB provide a circuit
3 drawing of a shift register input data MUX "shdcel" included in the
4 circuit of Figs. 7AA-HJ.

5 Fig. 7.18 is a graph illustrating how Figs. 7.18AA-CC are
6 to be assembled. After such assembly, Figs. 7.18AA-CC provide a
7 circuit drawing of a digital port output controller "doutport" included in
8 the circuit of Figs. 7AA-HJ.

9 Fig. 8 is a graph illustrating how Figs. 8AA-CB are to be
10 assembled. After such assembly, Figs. 8AA-CB provide a circuit drawing
11 of an RF processor "rfproc" included in the circuit of Figs. 6AA-EK.

12 Fig. 8.01 is a graph illustrating how Figs. 8.01AA-DE are
13 to be assembled. After such assembly, Figs. 8.01AA-DE provide a
14 circuit drawing of a receiver "rx" included in the circuit of
15 Figs. 8AA-CB.

16 Fig. 8.0101 is a graph illustrating how Figs.
17 8.0101AA-CB are to be assembled. After such assembly, Figs.
18 8.0101AA-CB provide a circuit drawing of a Schottky diode detector
19 "diodedet" included in the circuit of Figs. 8.01AA-DE.

20 Fig. 8.0102 is a graph illustrating how Figs.
21 8.0102AA-BD are to be assembled. After such assembly, Figs.
22 8.0102AA-BD provide a circuit drawing of a CMOS square law detector
23 "cmosdet" included in the circuit of Figs. 8.01AA-DE.
24

1 Fig. 8.0103 is a graph illustrating how Figs.
2 8.0103AA-CF are to be assembled. After such assembly, Figs.
3 8.0103AA-CF provide a circuit drawing of a video amplifier "videoamp1"
4 included in the circuit of Figs. 8.01AA-DE.

5 Fig. 8.0104 is a graph illustrating how Figs.
6 8.0104AA-BC are to be assembled. After such assembly, Figs.
7 8.0104AA-BC provide a circuit drawing of a second video amplifier
8 "videoamp2" included in the circuit of Figs. 8.01AA-DE.

9 Fig. 8.0105 is a graph illustrating how Figs.
10 8.0105AA-ED are to be assembled. After such assembly, Figs.
11 8.0105AA-ED provide a circuit drawing of a comparator "comparator"
12 included in the circuit of Figs. 8.01AA-DE.

13 Fig. 8.0106 is a graph illustrating how Figs.
14 8.0106AA-CD are to be assembled. After such assembly, Figs.
15 8.0106AA-CD provide a circuit drawing of an RF detect circuit "rxdet"
16 included in the circuit of Figs. 8.01AA-DE.

17 Fig. 8.0107 is a graph illustrating how Figs.
18 8.0107AA-GN are to be assembled. After such assembly, Figs.
19 8.0107AA-GN provide a circuit drawing of a receiver bias generator
20 "rxbias" included in the circuit of Figs. 8.01AA-DE.

21 Fig. 8.0108 is a graph illustrating how Figs.
22 8.0108AA-AC are to be assembled. After such assembly, Figs.
23 8.0108AA-AC provide a circuit drawing of a data transition detector
24 "datatx" included in the circuit of Figs. 8.01AA-DE.

1 Fig. 8.02 is a graph illustrating how Figs. 8.02AA-BC are to
2 be assembled. After such assembly, Figs. 8.02A-BC provide a circuit
3 drawing of a low power frequency locked loop "lpfl" included in the
4 circuit of Figs. 8AA-CB.

5 Fig. 8.0201 is a graph illustrating how Figs.
6 8.0201AA-AB are to be assembled. After such assembly, Figs.
7 8.0201AA-AB provide a circuit drawing of a timed lockout divider cell
8 "tldcel_bypass" included in the circuit of Figs. 8.02AA-BC.

9 Fig. 8.0202 is a graph illustrating how Figs.
10 8.0202AA-CD are to be assembled. After such assembly, Figs.
11 8.0202AA-CD provide a circuit drawing of a low power frequency locked
12 loop frequency comparator "freqcomp" included in the circuit of
13 Figs. 8.02AA-BC.

14 Fig. 8.0203 is a graph illustrating how Figs.
15 8.0203AA-BC are to be assembled. After such assembly, Figs.
16 8.0203AA-BC provide a circuit drawing of an up/down counter
17 "udcounter" included in the circuit of Figs. 8.02AA-BC.

18 Fig. 8.020301 is a graph illustrating how Figs.
19 8.020301AA-BB are to be assembled. After such assembly, Figs.
20 8.020301AA-BB provide a circuit drawing of an adder "udcounter_adder"
21 included in the circuit of Figs. 8.0203AA-BC.

22 Fig. 8.020302 is a graph illustrating how Figs.
23 8.020302AA-AB are to be assembled. After such assembly, Figs.
24

1 8.020302AA-AB provide a circuit drawing of a D type flip-flop
2 "udcounter_dff" included in the circuit of Figs. 8.0203AA-BC.

3 Fig. 8.0204 is a graph illustrating how Figs.
4 8.0204AA-EJ are to be assembled. After such assembly, Figs.
5 8.0204AA-EJ provide a circuit drawing of a low power current controlled
6 oscillator "lpcco" included in the circuit of Figs. 8.02AA-BC.

7 Fig. 8.0205 is a circuit drawing of a timed lockout
8 divider cell "tldcel" included in the circuit of Figs. 8.02AA-BC.

9 Fig. 8.03 is a graph illustrating how Figs. 8.03AA-AB are
10 to be assembled. After such assembly, Figs. 8.03AA-AB provide a
11 circuit drawing of a counter bit "lpfl_cbit" included in the circuit of
12 Figs. 8AA-CB.

13 Fig. 8.04 is a graph illustrating how Figs. 8.04AA-EE are
14 to be assembled. After such assembly, Figs. 8.04AA-EE provide a
15 circuit drawing of a receiver wake up controller "rxwu" included in the
16 circuit of Figs. 8AA-CB.

17 Fig. 8.0401 is a graph illustrating how Figs.
18 8.0401AA-AB are to be assembled. After such assembly, Figs.
19 8.0401AA-AB provide a circuit drawing of wake up abort logic "wuabort"
20 included in the circuit of Figs. 8.04AA-EE.

21 Fig. 8.040101 is a graph illustrating how Figs.
22 8.040101AA-AB are to be assembled. After such assembly, Figs.
23 8.040101AA-AB provide a circuit drawing of wake up abort logic
24 counter bit "wuabort_cbit" included in the circuit of Figs. 8.0401AA-AB.

1 Fig. 8.0402 is a graph illustrating how Figs.
2 8.0402AA-AB are to be assembled. After such assembly, Figs.
3 8.0402AA-AB provide a circuit drawing of a timed lockout divider cell
4 "tldcel" included in the circuit of Figs. 8.04AA-EE.

5 Fig. 8.05 is a graph illustrating how Figs. 8.05AA-DE are
6 to be assembled. After such assembly, Figs. 8.05AA-DE provide a
7 circuit drawing of a digital clock and data recovery circuit "dcr" included
8 in the circuit of Figs. 8AA-CB.

9 Fig. 8.0501 is a graph illustrating how Figs.
10 8.0501AA-BE are to be assembled. After such assembly, Figs.
11 8.0501AA-BE provide a circuit drawing of a PLL start-up circuit
12 "dcr_startup" included in the circuit of Figs. 8.05AA-DE.

13 Fig. 8.050101 is a graph illustrating how Figs.
14 8.050101AA-AB are to be assembled. After such assembly, Figs.
15 8.050101AA-AB provide a circuit drawing of a shift register cell
16 "dcr_sreg" included in the circuit of Figs. 8.0501AA-BE.

17 Fig. 8.050102 is a graph illustrating how Figs.
18 8.050102AA-AB are to be assembled. After such assembly, Figs.
19 8.050102AA-AB provide a circuit drawing of a counter bit
20 "dcr_counterbit" included in the circuit of Figs. 8.0501AA-BE.

21 Fig. 8.0502 is a graph illustrating how Figs.
22 8.0502AA-CD are to be assembled. After such assembly, Figs.
23 8.0502AA-CD provide a circuit drawing of a PLL state machine
24 "dcr_statemachine" included in the circuit of Figs. 8.05AA-DE.

1 Fig. 8.0503 is a graph illustrating how Figs.
2 8.0503AA-FN are to be assembled. After such assembly, Figs.
3 8.0503AA-FN provide a circuit drawing of a DCR bias generator
4 "dcr_bias" included in the circuit of Figs. 8.05AA-DE.

5 Fig. 8.0504 is a graph illustrating how Figs.
6 8.0504AA-EE are to be assembled. After such assembly, Figs.
7 8.0504AA-EE provide a circuit drawing of a VCO control voltage
8 generator "dcr_vcocontrol" included in the circuit of Figs. 8.05AA-DE.

9 Fig. 8.050401 is a graph illustrating how Figs.
10 8.050401AA-CK are to be assembled. After such assembly, Figs.
11 8.050401AA-CK provide a circuit drawing of a coarse step generator
12 "dcr_coarsestepgen" included in the circuit of Figs. 8.0504AA-EE.

13 Fig. 8.050402 is a graph illustrating how Figs.
14 8.050402AA-CJ are to be assembled. After such assembly, Figs.
15 8.050402AA-CJ provide a circuit drawing of a medium step generator
16 "dcr_medstepgen" included in the circuit of Figs. 8.0504AA-EE.

17 Fig. 8.050403 is a graph illustrating how Figs.
18 8.050403AA-BI are to be assembled. After such assembly, Figs.
19 8.050403AA-BI provide a circuit drawing of a medium fine step
20 generator "dcr_medfinestepgen" included in the circuit of
21 Figs. 8.0504AA-EE.

22 Fig. 8.050404 is a graph illustrating how Figs.
23 8.050404AA-BB are to be assembled. After such assembly, Figs.
24

1 8.050404AA-BB provide a circuit drawing of a fine step controller
2 "dcr_finestepctrl" included in the circuit of Figs. 8.0504AA-EE.

3 Fig. 8.050405 is a graph illustrating how Figs.
4 8.050405AA-EJ are to be assembled. After such assembly, Figs.
5 8.050405AA-EJ provide a circuit drawing of a fine step generator
6 "dcr_finestepgen" included in the circuit of Figs. 8.0504AA-EE.

7 Fig. 8.0505 is a graph illustrating how Figs.
8 8.0505AA-EF are to be assembled. After such assembly, Figs.
9 8.0505AA-EF provide a circuit drawing of a receiver VCO "dcr_vco"
10 included in the circuit of Figs. 8.05AA-DE.

11 Fig. 8.0506 is a graph illustrating how Figs.
12 8.0506AA-BB are to be assembled. After such assembly, Figs.
13 8.0506AA-BB provide a circuit drawing of an RX clock generator
14 "dcr_rxclkgen" included in the circuit of Figs. 8.05AA-DE.

15 Fig. 8.050601 is a circuit drawing of an RX
16 clock generator flip-flop "dcr_rxclkgenff" included in the circuit of
17 Figs. 8.0506AA-BB.

18 Fig. 8.0507 is a graph illustrating how Figs.
19 8.0507AA-AB are to be assembled. After such assembly, Figs.
20 8.0507AA-AB provide a circuit drawing of a PLL non-overlapping clock
21 generator "dcr_clkgen" included in the circuit of Figs. 8.05AA-DE.

22 Fig. 8.06 is a graph illustrating how Figs. 8.06AA-ED are
23 to be assembled. After such assembly, Figs. 8.06AA-ED provide a
24

1 circuit drawing of a BPSK/AM/Backscatter transmitter "tx" included in
2 the circuit of Figs. 8AA-CB.

3 Fig. 8.0601 is a graph illustrating how Figs.
4 8.0601AA-BB are to be assembled. After such assembly, Figs.
5 8.0601AA-BB provide a circuit drawing of a transmitter PLL "txpllfsyn"
6 included in the circuit of Figs. 8.06AA-ED.

7 Fig. 8.060101 is a graph illustrating how Figs.
8 8.060101AA-CC are to be assembled. After such assembly, Figs.
9 8.060101AA-CC provide a circuit drawing of a TX phase/frequency
10 detector "txpfdet" included in the circuit of Figs. 8.0601AA-BB.

11 Fig. 8.060102 is a graph illustrating how Figs.
12 8.060102AA-BB are to be assembled. After such assembly, Figs.
13 8.060102AA-BB provide a circuit drawing of a TX PLL charge pump
14 "txchgpump" included in the circuit of Figs. 8.0601AA-BB.

15 Fig. 8.060103 is a graph illustrating how Figs.
16 8.060103AA-CB are to be assembled. After such assembly, Figs.
17 8.060103AA-CB provide a circuit drawing of a TX PLL loop filter
18 "txloopfilter" included in the circuit of Figs. 8.0601AA-BB.

19 Fig. 8.060104 is a graph illustrating how Figs.
20 8.060104AA-DC are to be assembled. After such assembly, Figs.
21 8.060104AA-DC provide a circuit drawing of a TX VCO "txvco" included
22 in the circuit of Figs. 8.0601AA-BB.

23 Fig. 8.06010401 is a graph illustrating how
24 Figs. 8.06010401AA-BD are to be assembled. After such assembly, Figs.

1 8.06010401AA-BD provide a circuit drawing of a TX VCO stage
2 "txvcostage" included in the circuit of Figs. 8.060104AA-DC.

3 Fig. 8.0601040101 is a graph
4 illustrating how Figs. 8.0601040101AA-BC are to be assembled. After
5 such assembly, Figs. 8.0601040101AA-BC provide a layout plot showing
6 how the components of the VCO stage are laid out.

7 Fig. 8.060105 is a graph illustrating how Figs.
8 8.060105AA-DD are to be assembled. After such assembly, Figs.
9 8.060105AA-DD provide a circuit drawing of a divider "txdivider"
10 included in the circuit of Figs. 8.0601AA-BB.

11 Fig. 8.06010501 is a graph illustrating how
12 Figs. 8.06010501AA-AB are to be assembled. After such assembly, Figs.
13 8.06010501AA-AB provide a circuit drawing of a divider flip-flop
14 "txdivtff" included in the circuit of Figs. 8.060105AA-DD.

15 Fig. 8.0602 is a graph illustrating how Figs.
16 8.0602AA-AB are to be assembled. After such assembly, Figs.
17 8.0602AA-AB provide a circuit drawing of a test mode data selector
18 "txdatasel" included in the circuit of Figs. 8.06AA-ED.

19 Fig. 8.0603 is a graph illustrating how Figs.
20 8.0603AA-AB are to be assembled. After such assembly, Figs.
21 8.0603AA-AB provide a circuit drawing of a BPSK modulation driver
22 "txbpsk" included in the circuit of Figs. 8.06AA-ED.

23 Fig. 8.0604 is a graph illustrating how Figs.
24 8.0604AA-AB are to be assembled. After such assembly, Figs.

1 8.0604AA-AB provide a circuit drawing of a frequency doubler
2 "txdoubler" included in the circuit of Figs. 8.06AA-ED.

3 Fig. 8.060401 is a graph illustrating how Figs.
4 8.060401AA-FE are to be assembled. After such assembly, Figs.
5 8.060401AA-FE provide a circuit drawing of a frequency doubler core
6 "txfdbl" included in the circuit of Figs. 8.0604AA-ED.

7 Fig. 8.0605 is a graph illustrating how Figs.
8 8.0605AA-AB are to be assembled. After such assembly, Figs.
9 8.0605AA-AB provide a circuit drawing of a second frequency doubler
10 "txdoubler2" included in the circuit of Figs. 8.06AA-ED.

11 Fig. 8.060501 is a graph illustrating how Figs.
12 8.060501AA-CD are to be assembled. After such assembly, Figs.
13 8.060501AA-CD provide a circuit drawing of doubler driver amps
14 "txfdbldrv" included in the circuit of Figs. 8.0605AA-CD.

15 Fig. 8.060502 is a graph illustrating how Figs.
16 8.060502AA-CD are to be assembled. After such assembly, Figs.
17 8.060502AA-CD provide a circuit drawing of second doubler driver amps
18 "txfdbldrv2" included in the circuit of Figs. 8.0605AA-CD.

19 Fig. 8.060503 is a graph illustrating how Figs.
20 8.060503AA-FE are to be assembled. After such assembly, Figs.
21 8.060503AA-FE provide a circuit drawing of a frequency doubler core
22 "txfdbl2" included in the circuit of Figs. 8.0605AA-CD.

23 Fig. 8.0606 is a graph illustrating how Figs.
24 8.0606AA-IE are to be assembled. After such assembly, Figs.

1 8.0606AA-IE provide a circuit drawing of a transmitter power amp
2 "txpoweramp" included in the circuit of Figs. 8.06AA-ED.

3 Fig. 8.0607 is a graph illustrating how Figs.
4 8.0607AA-JJ are to be assembled. After such assembly, Figs.
5 8.0607AA-JJ provide a circuit drawing of a transmitter bias generator
6 "txbias" included in the circuit of Figs. 8.06AA-ED.

7 Fig. 8.0608 is a graph illustrating how Figs.
8 8.0608AA-BB are to be assembled. After such assembly, Figs.
9 8.0608AA-BB provide a circuit drawing of a modulated backscatter
10 transmitter "txmbs" included in the circuit of Figs. 8.06AA-ED.

11 Fig. 8.07 is a graph illustrating how Figs. 8.07AA-BB are to
12 be assembled. After such assembly, Figs. 8.07AA-BB provide a partial
13 circuit drawing of a 915 MHZ transmitter "tx915" included in the circuit
14 of Figs. 8AA-CB in place of the transmitter "tx" in an alternative
15 embodiment of the invention.

16 Fig. 8.0701 is a graph illustrating how Figs.
17 8.0701AA-CB are to be assembled. After such assembly, Figs.
18 8.0701AA-CB provide a circuit drawing of a TX VCO stage
19 "txvcostage915" for use with the 915 MHZ transmitter "tx915" of
20 Fig. 8.07 in place of the TX VCO "txvco" of Fig. 8.060104.

21 Fig. 9 is a graph illustrating how Figs. 9AA-CB are to be
22 assembled. After such assembly, Figs. 9AA-CB provide a circuit drawing
23 of an analog processor "anlgproc" included in the circuit of
24 Figs. 6AA-EK.

1 Fig. 9.01 is a graph illustrating how Figs. 9.01AA-DH are
2 to be assembled. After such assembly, Figs. 9.01AA-DH provide a
3 circuit drawing of an algorithmic A/D converter with databus interface
4 "ada_new" included in the circuit of Figs. 9AA-CB.

5 Fig. 9.0101 is a graph illustrating how Figs.
6 9.0101AA-CK are to be assembled. After such assembly, Figs.
7 9.0101AA-CK provide a circuit drawing of a differential I/O op-amp
8 "dopamp" included in the circuit of Figs. 9.01AA-DH.

9 Fig. 9.0102 provides a circuit drawing of an analog
10 divider (divide by two) "adaprescale" included in the circuit of
11 Figs. 9.01AA-DH.

12 Fig. 9.0103 is a graph illustrating how Figs.
13 9.0103AJ-FP are to be assembled. After such assembly, Figs.
14 9.0103AJ-FP provide a circuit drawing of a control PLA "adactl_new"
15 included in the circuit of Figs. 9.01AA-DH.

16 Fig. 9.010301 is a graph illustrating how Figs.
17 9.010301AA-CC are to be assembled. After such assembly, Figs.
18 9.010301AA-CC provide a circuit drawing of a clock generator
19 "adacgen_new" included in the circuit of Figs. 9.0103AJ-FP.

20 Fig. 9.010302 is a graph illustrating how Figs.
21 9.010302AA-AB are to be assembled. After such assembly, Figs.
22 9.010302AA-AB provide a circuit drawing of a control output driver
23 "adacdrv_new" included in the circuit of Figs. 9.0103AJ-FP.

1 Fig. 9.010303 is a graph illustrating how Figs.
2 9.010303AA-AB are to be assembled. After such assembly, Figs.
3 9.010303AA-AB provide a circuit drawing of a control output driver
4 "adacdrvn_new" included in the circuit of Figs. 9.0103AJ-FP.

5 Fig. 9.010304 is a graph illustrating how Figs.
6 9.010304AA-BB are to be assembled. After such assembly, Figs.
7 9.010304AA-BB provide a circuit drawing of a data latch "adadlat_new"
8 included in the circuit of Figs. 9.0103AJ-FP.

9 Fig. 9.0104 is a graph illustrating how Figs.
10 9.0104AA-DD are to be assembled. After such assembly, Figs.
11 9.0104AA-DD provide a circuit drawing of an analog bias circuit
12 "adabias_new" included in the circuit of Figs. 9.01AA-DH.

13 Fig. 9.02 is a graph illustrating how Figs. 9.02AA-DK are
14 to be assembled. After such assembly, Figs. 9.02AA-DK provide a
15 circuit drawing of a Vdd power up detector "pup" included in the
16 circuit of Figs. 9AA-CB.

17 Fig. 9.03 is a graph illustrating how Figs. 9.03AA-BB are to
18 be assembled. After such assembly, Figs. 9.03AA-BB provide a circuit
19 drawing of a master bias source "mbs" included in the circuit of
20 Figs. 9AA-CB.

21 Fig. 9.0301 is a graph illustrating how Figs.
22 9.0301AA-DJ are to be assembled. After such assembly, Figs.
23 9.0301AA-DJ provide a circuit drawing of a band gap reference
24 generator "mbs_bgr" included in the circuit of Figs. 9.03AA-BB.

1 Fig. 9.0302 is a graph illustrating how Figs.
2 9.0302AA-DI are to be assembled. After such assembly, Figs.
3 9.0302AA-DI provide a circuit drawing of a temperature compensated
4 current generator "mbs_cur" included in the circuit of Figs. 9.03AA-BB.

5 Fig. 9.0303 is a graph illustrating how Figs.
6 9.0303AA-CF are to be assembled. After such assembly, Figs.
7 9.0303AA-CF provide a circuit drawing of a reference current generator
8 "mbs_iref" included in the circuit of Figs. 9.03AA-BB.

9 Fig. 9.04 is a graph illustrating how Figs. 9.04AA-CE are
10 to be assembled. After such assembly, Figs. 9.04AA-CE provide a
11 circuit drawing of a voltage regulator "vrg" included in the circuit of
12 Figs. 9AA-CB.

13 Fig. 9.05 is a graph illustrating how Figs. 9.05AA-FE are to
14 be assembled. After such assembly, Figs. 9.05AA-FE provide a circuit
15 drawing of a voltage regulator "vrgtx" included in the circuit of
16 Figs. 9AA-CB.

17 Fig. 9.0501 is a graph illustrating how Figs.
18 9.0501AA-CD are to be assembled. After such assembly, Figs.
19 9.0501AA-CD provide a circuit drawing of an operational amplifier
20 without compensation "opampnc" included in the circuit of
21 Figs. 9.05AA-FE.

22 Fig. 9.06 is a graph illustrating how Figs. 9.06AA-DD are
23 to be assembled. After such assembly, Figs. 9.06AA-DD provide a
24

1 circuit drawing of a bias OK detector "biasok" included in the circuit
2 of Figs. 9AA-CB.

3 Fig. 9.07 is a graph illustrating how Figs. 9.07AA-EG are
4 to be assembled. After such assembly, Figs. 9.07AA-EG provide a
5 circuit drawing of an analog port current source "aportcs" included in
6 the circuit of Figs. 9AA-CB.

7 Fig. 9.08 is a graph illustrating how Figs. 9.08AA-CC are
8 to be assembled. After such assembly, Figs. 9.08AA-CC provide a
9 circuit drawing of an analog multiplexer decoder "asl" included in the
10 circuit of Figs. 9AA-CB.

11 Fig. 9.09 is a graph illustrating how Figs. 9.09AA-BB are to
12 be assembled. After such assembly, Figs. 9.09AA-BB provide a circuit
13 drawing of a random clock generator "rcg" included in the circuit of
14 Figs. 9AA-CB.

15 Fig. 9.0901 is a graph illustrating how Figs.
16 9.0901AA-CH are to be assembled. After such assembly, Figs.
17 9.0901AA-CH provide a circuit drawing of a linear feedback shift
18 register "rcg_sreg" included in the circuit of Figs. 9.09AA-CB.

19 Fig. 9.090101 is a graph illustrating how Figs.
20 9.090101AA-CC are to be assembled. After such assembly, Figs.
21 9.090101AA-CC provide a circuit drawing of a shift register bit
22 "rcg_sregbit0" included in the circuit of Figs. 9.0901AA-CH.

23 Fig. 9.090102 is a graph illustrating how Figs.
24 9.090102AA-BB are to be assembled. After such assembly, Figs.

1 9.090102AA-BB provide a circuit drawing of a shift register bit
2 "rcg_sregbit" included in the circuit of Figs. 9.0901AA-CH.

3 Fig. 9.0902 is a graph illustrating how Figs.
4 9.0902AA-FL are to be assembled. After such assembly, Figs.
5 9.0902AA-FL provide a circuit drawing of a low power oscillator and
6 bias generator "rcg_osc" included in the circuit of Figs. 9.09AA-CB.

7 Fig. 9.0903 is a graph illustrating how Figs.
8 9.0903AA-CC are to be assembled. After such assembly, Figs.
9 9.0903AA-CC provide a circuit drawing of a clock generator "rcg_clkgen"
10 included in the circuit of Figs. 9.09AA-CB.

11 Fig. 10 is a graph illustrating how Figs. 10AA-DD are to be
12 assembled. After such assembly, Figs. 10AA-DD provide a circuit
13 drawing of a pn processor "pnproc" included in the circuit of
14 Figs. 6AA-EK.

15 Fig. 10.01 is a graph illustrating how Figs. 10.01AA-DI are
16 to be assembled. After such assembly, Figs. 10.01AA-DI provide a
17 circuit drawing of a digital PN correlator "dcorr" included in the circuit
18 of Figs. 10AA-DI.

19 Fig. 10.0101 is a graph illustrating how Figs.
20 10.0101AA-BG are to be assembled. After such assembly, Figs.
21 10.0101AA-BG provide a circuit drawing of a PN correlator shift register
22 "dcorr_sreg" included in the circuit of Figs. 10.01AA-DI.

23 Fig. 10.010101 is a circuit drawing of a PN
24 correlator bit "dcorr_bit" included in the circuit of Figs. 10.0101AA-BG.

1 Fig. 10.01010101 is a circuit drawing of a
2 shift register cell "dcorr_sregbit" included in the circuit of
3 Figs. 10.010101.

4 Fig. 10.0102 is a graph illustrating how Figs.
5 10.0102AA-CN are to be assembled. After such assembly, Figs.
6 10.0102AA-CN provide a circuit drawing of a correlator bias generator
7 "dcorr_bias" included in the circuit of Figs. 10.01AA-DI.

8 Fig. 10.02 is a graph illustrating how Figs. 10.02AA-BE are
9 to be assembled. After such assembly, Figs. 10.02AA-BE provide a
10 circuit drawing of a PN lock detector "pnlockdet" included in the circuit
11 of Figs. 10AA-DD.

12 Fig. 10.0201 is a graph illustrating how Figs.
13 10.0201AA-AB are to be assembled. After such assembly, Figs.
14 10.0201AA-AB provide a circuit drawing of a counter bit "lockcounterbit"
15 included in the circuit of Figs. 10.02AA-BE.

16 Fig. 10.03 is a graph illustrating how Figs. 10.03AA-AB are
17 to be assembled. After such assembly, Figs. 10.03AA-AB provide a
18 circuit drawing of a PN generator clock "pngclk" included in the circuit
19 of Figs. 10AA-DD.

20 Fig. 10.04 is a graph illustrating how Figs. 10.04AA-CE are
21 to be assembled. After such assembly, Figs. 10.04AA-CE provide a
22 circuit drawing of a PN generator shift register "pngshr" included in the
23 circuit of Figs. 10 AA-DD.
24

1 Fig. 10.0401 is a circuit drawing of a PN generator
2 shift register cell "pngsreg" included in the circuit of Figs. 10.04AA-CE.

3 Fig. 10.0402 is a graph illustrating how Figs.
4 10.0402AA-CB are to be assembled. After such assembly, Figs.
5 10.0402AA-CB provide a circuit drawing of a PN generator shift register
6 summer "pngssum" included in the circuit of Figs. 10.04AA-CE.

7 Fig. 10.05 is a circuit drawing of a PN controller D type
8 flip-flop "pnddff" included in the circuit of Figs. 10AA-DD.

9 Fig. 10.06 is a graph illustrating how Figs. 10.06AA-DH are
10 to be assembled. After such assembly, Figs. 10.06AA-DH provide a
11 circuit drawing of differential and PN encoder "dpenc" included in the
12 circuit of Figs. 10AA-DD.

13 Fig. 10.07 is a graph illustrating how Figs. 10.07AA-CD are
14 to be assembled. After such assembly, Figs. 10.07AA-CD provide a
15 circuit drawing of a PSK/FSK generator "fskgen" included in the circuit
16 of Figs. 10AA-DD.

17 Fig. 10.0701 is a graph illustrating how Figs.
18 10.0701AA-AB are to be assembled. After such assembly, Figs.
19 10.0701AA-AB provide a circuit drawing of a FSK counter bit "fskcbt"
20 included in the circuit of Figs. 10AA-DD.

21 Fig. 11 is a graph illustrating how Figs. 11AA-AB are to be
22 assembled. After such assembly, Figs. 11AA-AB provide a circuit
23 drawing of a battery I/O buffer "batalg" included in the circuit of
24 Figs. 6AA-EK.

1 Fig. 12 is a graph illustrating how Figs. 12AA-AB are to be
2 assembled. After such assembly, Figs. 12AA-AB provide a circuit
3 drawing of a digital I/O pad buffer "paddig" included in the circuit of
4 Figs. 6AA-EK.

5 Fig. 13 is a circuit drawing of a digital input pad buffer
6 "paddigin" included in the circuit of Figs. 6AA-EK.

7 Fig. 13.5 is a circuit drawing of a digital input pad buffer
8 "paddigin2" included in the circuit of Figs. 6AA-EK.

9 Fig. 14 is a circuit drawing of an analog I/O pad buffer "padalg"
10 included in the circuit of Figs. 6AA-EK.

11 Fig. 15 is a graph illustrating how Figs. 15AA-BC are to be
12 assembled. After such assembly, Figs. 15AA-BC provide a circuit
13 drawing of return link configuration control logic "rlconfig" included in
14 the circuit of Figs. 6AA-EK.

15 Fig. 16 is a graph illustrating how Figs. 16AA-EH are to be
16 assembled. After such assembly, Figs. 16AA-EH provide a circuit
17 drawing of a temperature sensor "tsn" included in the circuit of
18 Figs. 6AA-EK.

19 Fig. 16.01 is a graph illustrating how Figs. 16.01AA-DI are
20 to be assembled. After such assembly, Figs. 16.01AA-DI provide a
21 circuit drawing of an operational amplifier "opamp" included in the
22 circuit of Figs. 16AA-EH.

23 Fig. 17 is a graph illustrating how Figs. 17AA-BB are to be
24 assembled. After such assembly, Figs. 17AA-BB provide a circuit

1 drawing of a magnetic field sensor "mag" (a sensor for sensing magnetic
2 fields) included in the circuit of Figs. 6AA-EK.

3 Fig. 18 is a graph illustrating how Figs. 18AA-AB are to be
4 assembled. After such assembly, Figs. 18AA-AB provide a circuit
5 drawing of a chip bypass capacitor "bypcap3" included in the circuit of
6 Figs. 6AA-EK.

7 Fig. 19 is a graph illustrating how Figs. 19AA-EK are to be
8 assembled. After such assembly, Figs. 19AA-EK provide a circuit
9 drawing of a monolithic semiconductor integrated circuit "LO3BT3F" in
10 accordance with an alternative embodiment of the invention. The
11 integrated circuit of Figs. 19AA-EK is similar to the integrated circuit
12 shown in Figs. 6AA-EK, like component names indicating like
13 components, except that the integrated circuit of Figs. 19AA-EK has no
14 ROM, and is adapted to be connected to external ROM "extrom". The
15 embodiment of Figs. 19AA-EK is particularly useful for test purposes.

16 Fig. 20 is a graph illustrating how Figs. 20AA-DF are to be
17 assembled. After such assembly, Figs. 20AA-DF provide a circuit
18 drawing of a data processor "dataproc_t3" to be used in the integrated
19 circuit of Fig. 19 in place of the data processor "dataproc" of Fig. 7.

20 Fig. 20.01 is a graph illustrating how Figs. 20.01AA-CB are
21 to be assembled. After such assembly, Figs. 20.01AA-CB provide a
22 circuit drawing of an external ROM "extrom" shown in Figs. 20AA-CB.

23 Fig. 20.0101 is a graph illustrating how Figs.
24 20.0101AA-BB are to be assembled. After such assembly, Figs.

1 20.0101AA-BB provide a circuit drawing of external ROM control logic
2 "extromctl" included in the circuit of Figs. 20.01AA-CB.

3 Fig. 20.0102 is a circuit drawing of an external ROM
4 address interface "extromad" included in the circuit of Figs. 20.01AA-CB.

5 Fig. 20.0103 is a graph illustrating how Figs.
6 20.0103AA-AC are to be assembled. After such assembly, Figs.
7 20.0103AA-AC provide a circuit drawing of a digital I/O pad buffer
8 "paddigt3" included in the circuit of Figs. 20.01AA-CB.

9 Fig. 20.0104 is a circuit drawing of an external ROM
10 databus interface "extromdb" included in the circuit of Figs. 20.01AA-CB.

11 Fig. 21 is a circuit schematic illustrating a transmitter switchable
12 between an active mode and a backscatter mode, and employing
13 separate antennas for the active mode and the backscatter mode.

14 Fig. 22 is a circuit schematic illustrating a transmitter switchable
15 between an active mode and a backscatter mode, and employing the
16 same antenna for both the active mode and the backscatter mode.

17 Fig. 23 is a circuit schematic illustrating low battery detection
18 circuitry.

19 Fig. 24 is a circuit schematic illustrating circuitry providing a low
20 power wake up timer.

21 Figs. 25-26 provide a flowchart illustrating logic employed for
22 switching between a low power sleep mode, and higher power modes.

23 Fig. 27 is a diagram of current versus time illustrating switching
24 between a low power sleep mode, and higher power modes.

1 Fig. 28 is a circuit schematic illustrating a Schottky diode detector.

2 Fig. 29 is a circuit schematic illustrating a Schottky diode detector
3 in accordance with one embodiment of the invention.

4 Fig. 30 is a circuit schematic illustrating a Schottky diode detector
5 in accordance with another embodiment of the invention.

6 Fig. 31 is a waveform diagram illustrating the effect of high
7 power radio frequency input levels on Schottky detectors.

8 Fig. 32 is a circuit schematic illustrating a high frequency voltage
9 controlled oscillator differential stage.

10 Fig. 33 is a waveform diagram illustrating the effect of errors in
11 frequency doubler circuits that necessitates correction, such as by using
12 an integrator and feedback.

13 Fig. 34 is a circuit schematic illustrating a frequency doubler
14 circuit that employs an integrator and feedback to solve the problem
15 illustrated in Fig. 33.

16 Fig. 35 is a waveform diagram illustrating input and output waves
17 created and employed by a frequency doubler circuit such as the one
18 shown in Fig. 34.

19 Fig. 36 is a circuit schematic illustrating a symmetric frequency
20 doubler circuit that does not require an integrator and feedback to
21 solve the problem illustrated in Fig. 33. The frequency doubler circuit
22 of Fig. 36 creates and employs waveforms such as those shown in
23 Fig. 35.

24

1 Fig. 37 is a circuit schematic of an inverter illustrating a power
2 saving technique employed in a pseudo random number generator
3 embodying one aspect of the invention.

4 Fig. 38 is a cross-sectional view illustrating a step of a process
5 of manufacturing a Schottky diode.

6 Fig. 39 is a cross-sectional view illustrating a step subsequent to
7 the step of Fig. 38.

8 Fig. 40 is a cross-sectional view illustrating a step subsequent to
9 the step of Fig. 39.

10 Fig. 41 is a cross-sectional view illustrating a step subsequent to
11 the step of Fig. 40.

12 Fig. 42 is a top view illustrating a step subsequent to the step
13 of Fig. 41 and showing parallel connection of some Schottky diodes of
14 a plurality of Schottky diodes.

15 Fig. 43 is a top view illustrating a step subsequent to the step
16 of Fig. 41 in accordance with an alternative embodiment of the
17 invention and showing parallel connection of all Schottky diodes of a
18 plurality of Schottky diodes.

19 Fig. 44 is a cross-sectional view illustrating a step of an
20 alternative process of manufacturing a Schottky diode.

21 Fig. 45 is a cross-sectional view illustrating a step subsequent to
22 the step of Fig. 44.

23 Fig. 46 is a cross-sectional view illustrating a step subsequent to
24 the step of Fig. 45.

1 Fig. 47 is a cross-sectional view illustrating a step subsequent to
2 the step of Fig. 46.

3 Fig. 48 is a simplified circuit schematic of a quick bias AC-
4 coupled video amplifier included in the integrated circuit.

5 Fig. 49 is a plot of voltage versus angular frequency illustrating
6 selection of components to realize a desired high pass roll off frequency
7 in the amplifier of Fig. 48.

8 Fig. 50 is a simplified circuit schematic illustrating sharing of a
9 single antenna by both a Schottky detector and an active transmitter.

10 Fig. 51 is a simplified circuit schematic illustrating circuitry
11 included in the active transmitter of Fig. 50 in accordance with one
12 aspect of the invention.

13 Fig. 52 is a simplified circuit schematic illustrating sharing of a
14 single antenna by both a Schottky detector and a backscatter
15 transmitter.

16 Fig. 53 is a simplified circuit schematic illustrating sharing of a
17 single antenna by both a Schottky detector and a backscatter transmitter
18 in accordance with an alternative embodiment of the invention.

19 Fig. 54 is a graph of voltage versus time illustrating a method of
20 determining when frequency lock has occurred.

21 Fig. 55 is a flowchart illustrating a top level of code stored in
22 ROM in the integrated circuit.

23 Figs. 56A and B define a flowchart illustrating a command
24 processing routine performed by the integrated circuit.

1 Figs. 57A and B define a flowchart illustrating steps performed
2 by the integrated circuit in response to an Identify command received
3 from the interrogator in which the interrogator requests, via radio
4 frequency command, identification of an integrated circuit.

5 Fig. 58 is a flowchart illustrating steps performed to initialize the
6 interrogator.

7 Fig. 59 is a flowchart illustrating steps performed when the
8 interrogator sends a command to the integrated circuit.

9 Fig. 60 is a flowchart illustrating steps performed by the
10 interrogator in issuing an Identify command.

11 Fig. 61 is a simplified circuit diagram of a digital clock recovery
12 loop including a start-up circuit including a counter, a voltage controlled
13 oscillator, a charge pump and loop filter, and a state machine. The
14 start-up circuit and counter determine when clock frequency is close to
15 a desired value.

16 Fig. 62 is a plot of frequency produced by a voltage controlled
17 oscillator versus control voltage applied to the voltage controlled
18 oscillator.

19 Fig. 63 is a timing diagram showing when the start-up circuit of
20 Fig. 61 issues pump up signals to increase the control voltage applied
21 to the voltage controlled oscillator.

22 Fig 64 is a state diagram illustrating the design of the state
23 machine of Fig. 61.

1 Figs. 65-70 illustrate steps used in designing a state machine that
2 implements the state diagram of Fig. 64. Fig. 65 illustrates flip-flops
3 having outputs representing in binary form the various states of the
4 state diagrams and having inputs representing next state values. Fig.
5 66 is a state table. Figs. 67 and 68 are Karnaugh maps used to
6 derive minimum logic circuitry needed to derive circuit output functions
7 and flip-flop input functions.

8 Fig. 71 is a simplified timing diagram illustrating operation of the
9 state machine.

10 Fig. 72 is a table illustrating step sizes produced by the start-up
11 circuit and the state machine.

12 SUMMARY OF THE INVENTION

13 The invention provides a radio frequency identification device
14 comprising an integrated circuit including a receiver, a transmitter, and
15 a microprocessor. The integrated circuit is preferably a monolithic
16 single die integrated circuit including the receiver, the transmitter, and
17 the microprocessor. Because the device includes an active transponder,
18 instead of a transponder which relies on magnetic coupling for power,
19 the device has a much greater range.
20

21 One aspect of the invention provides a radio frequency
22 identification device comprising a monolithic integrated circuit including
23 a receiver, a transmitter which can operate at frequencies above 400
24 MHz, and a microprocessor.

1 Another aspect of the invention provides a radio frequency
2 identification device comprising a monolithic integrated circuit including
3 a receiver, a transmitter which can operate at frequencies above 1 GHz,
4 and a microprocessor.

5 Another aspect of the invention provides a radio frequency
6 identification device comprising a monolithic integrated circuit including
7 a transmitter, a microprocessor, and a receiver which can receive and
8 interpret signals having frequencies above 400 MHz.

9 Another aspect of the invention provides a radio frequency
10 identification device comprising a monolithic integrated circuit including
11 a transmitter, a microprocessor, and a receiver which can receive and
12 interpret signals having frequencies above 1 Ghz.

13 Another aspect of the invention provides a radio frequency
14 identification device comprising a monolithic integrated circuit including
15 a receiver, a microwave transmitter, and a microprocessor.

16 Another aspect of the invention provides a radio frequency
17 identification device comprising a monolithic integrated circuit including
18 a microwave receiver, a transmitter, and a microprocessor.

19 Another aspect of the invention provides a radio frequency
20 identification device comprising a single die including a receiver, a
21 transmitter, and a microprocessor, the die having a size less than 90,000
22 mils². In accordance with a more preferred embodiment of the
23 invention, the die has a size less than 300 x 300 mils². In accordance
24 with a more preferred embodiment of the invention, the die has a size

1 less than 37,500 mils². In accordance with a more preferred
2 embodiment of the invention, the die has a size of 209 by 116 mils².

3 Another aspect of the invention provides a radio frequency
4 identification device comprising a single die integrated circuit including
5 a receiver, a transmitter, and a microprocessor.

6 Another aspect of the invention provides a radio frequency
7 identification device comprising a single die with a single metal layer
8 including a receiver, a transmitter, and a microprocessor.

9 Another aspect of the invention provides a radio frequency
10 identification device comprising a single die integrated circuit including
11 a receiver, a transmitter, and a microprocessor formed using a single
12 metal layer processing method.

13 Another aspect of the invention provides a radio frequency
14 identification system comprising an integrated circuit including a receiver,
15 and a transmitter; and an antenna coupled to the integrated circuit, the
16 integrated circuit being responsive to radio frequency signals of multiple
17 carrier frequencies.

18 Another aspect of the invention provides a radio frequency
19 identification device comprising transponder circuitry formed in a
20 monolithic integrated circuit comprising both transmitting and receiving
21 circuits of the transponder circuitry; a power supply operably associated
22 with the transponder circuitry; and an antenna operably associated with
23 the transponder circuitry.
24

1 Another aspect of the invention provides a radio frequency
2 identification device comprising a monolithic semiconductor integrated
3 circuit including a receiver and a transmitter; means for applying a
4 supply of power to the integrated circuit device from a battery; and
5 means for configuring the integrated circuit to receive and transmit
6 radio frequency signals.

7 Another aspect of the invention provides a method for producing
8 a radio frequency identification device, the method comprising the
9 following steps: providing a monolithic integrated circuit having a
10 receiver and a transmitter; and providing a package configured to carry
11 the integrated circuit.

12 Another aspect of the invention provides a method for adapting
13 a radio frequency data communication device for use at a desired
14 carrier frequency for use in a radio frequency identification (RFID)
15 device, the method comprising the following steps: providing an
16 integrated circuit having tunable circuitry, the integrated circuit
17 comprising a receiver and a transmitter; configuring the integrated circuit
18 for connection with a power supply to enable operation; configuring the
19 integrated circuit to receive and apply radio frequency signals via an
20 antenna, the antenna and the tunable circuitry cooperating in operation
21 there between; and tuning the tunable circuitry and the antenna to
22 realize a desired carrier frequency from a wide range of possible carrier
23 frequencies. A method for adapting a radio frequency data
24 communication device for use at a desired carrier frequency for use in

1 a radio frequency identification device, the method comprising the
2 following steps: providing an integrated circuit having tunable circuitry,
3 the integrated circuit comprising a receiver and a transmitter; configuring
4 the integrated circuit for connection with a power supply to enable
5 operation; configuring the integrated circuit to receive and apply radio
6 frequency signals via an antenna, the antenna and the tunable circuitry
7 cooperating in operation there between; and tuning the antenna to
8 realize a desired carrier frequency from a wide range of possible carrier
9 frequencies.

10 Another aspect of the invention provides a radio frequency
11 communications device comprising an integrated circuit including a
12 transmitter and a receiver, the integrated circuit including a clock
13 recovery circuit recovering a clock frequency from a signal received by
14 the receiver, the clock recovery circuit having a phase lock loop
15 including a voltage controlled oscillator, and a loop filter having a
16 capacitor storing a voltage indicative of a frequency at which the
17 voltage controlled oscillator is oscillating, the integrated circuit using the
18 voltage stored on the capacitor to generate a clock frequency for the
19 transmitter.

20 Another aspect of the invention provides a method of recovering
21 a clock frequency from a received radio frequency signal, storing the
22 clock frequency, and using the clock frequency for radio frequency
23 transmission by a transmitter, the method comprising: providing a clock
24 recovery circuit recovering a clock frequency from a signal received by

1 the receiver, the clock recovery circuit having a phase lock loop
2 including a voltage controlled oscillator, and a loop filter having a
3 capacitor; using the clock recovery circuit to recover a clock frequency
4 from a received radio frequency signal; storing on the capacitor a
5 voltage indicative of frequency at which the voltage controlled oscillator
6 is oscillating; using the voltage stored on the capacitor to generate a
7 clock frequency for use by the transmitter.

8 Another aspect of the invention provides a method of recovering
9 and storing a clock frequency from a received radio frequency signal in
10 a radio frequency identification device including a transmitter and a
11 receiver, the method comprising providing a clock recovery circuit
12 recovering a clock frequency from a signal received by the receiver, the
13 clock recovery circuit having a phase lock loop; using the clock recovery
14 circuit to recover a clock frequency from a received radio frequency
15 signal; storing in analog form a value indicative of frequency at which
16 the voltage controlled oscillator is oscillating; and using the analog value
17 to generate a clock frequency for use by the transmitter.

18 Another aspect of the invention provides a radio frequency
19 communications device comprising an integrated circuit including a
20 transmitter and a receiver, the transmitter being switchable between a
21 backscatter mode, wherein a carrier for the transmitter is derived from
22 a carrier received from an interrogator spaced apart from the radio
23 frequency communications device, and an active mode, wherein a carrier
24 for the transmitter is generated by the integrated circuit itself.

1 Another aspect of the invention provides a radio frequency
2 communications device comprising an integrated circuit including a
3 transmitter and a receiver, the transmitter selectively transmitting a
4 signal using a modulation scheme, the transmitter being switchable for
5 transmission using different modulation schemes.

6 Another aspect of the invention provides a method for adapting
7 modulation schemes of a radio frequency data communication device in
8 a radio frequency identification device, the method comprising the
9 following steps: providing an integrated circuit having switching circuitry,
10 a receiver, a transmitter, and a processor; the integrated circuit having
11 a plurality of transmitting circuits including a first transmitting circuit
12 configured to realize an active transmitter scheme and a second
13 transmitting circuit configured to realize a modulated backscatter scheme;
14 configuring the integrated circuit for connection with a power supply to
15 enable operation; configuring the integrated circuit to receive and apply
16 radio frequency signals via an antenna, the antenna and the tunable
17 circuitry cooperating in operation; and switching the switchable circuitry
18 with respect to the antenna to enable one of the transmitting circuits
19 to realize one of the modulation schemes.

20 Another aspect of the invention provides a method for adapting
21 modulation schemes of a radio frequency data communication device in
22 a radio frequency identification device, the method comprising the
23 following steps: providing an integrated circuit having switching circuitry,
24 a receiver, a transmitter, and a processor, the integrated circuit

1 including a plurality of transmitting circuits, the plurality of transmitting
2 circuits configured to selectively realize a plurality of modulated
3 backscatter schemes; configuring the integrated circuit for connection
4 with a power supply to enable operation; configuring the integrated
5 circuit to receive and apply radio frequency signals via an antenna, the
6 antenna and the tunable circuitry cooperating in operation; and switching
7 the transmitting circuits with respect to the antenna to enable one of
8 the transmitting circuits to realize one of the modulation schemes.

9 Another aspect of the invention provides a radio frequency
10 identification device comprising: an integrated circuit including a
11 transmitter and a receiver, the integrated circuit being adapted to be
12 connected to a battery, and further including a comparator comparing
13 the voltage of the battery with a predetermined voltage and generating
14 a low battery signal if the voltage of the battery is less than the
15 predetermined voltage.

16 Another aspect of the invention provides a method for detecting
17 a low battery condition in a radio frequency data communication device
18 for use in a radio frequency identification device, the method comprising
19 the following steps: providing an integrated circuit having switching
20 circuitry, a receiver, and a transmitter, the integrated circuit including
21 a comparator configured to compare the battery voltage with a
22 predetermined voltage and generate a low battery signal if the battery
23 voltage is less than the predetermined voltage; configuring the integrated
24 circuit for connection with the battery to enable operation; configuring

1 the integrated circuit to receive and apply radio frequency signals via
2 an antenna, the antenna and the tunable circuitry cooperating in
3 operation there between; determining a predetermined voltage for the
4 battery; comparing the voltage of the battery with the predetermined
5 voltage; and generating a low battery signal if the voltage of the battery
6 is less than the predetermined voltage.

7 Another aspect of the invention provides a radio frequency
8 communications device comprising an integrated circuit including a
9 transmitter and a receiver, the integrated circuit periodically checking if
10 a radio frequency signal is being received by the receiver, the integrated
11 circuit further including a timer setting a time period for the checking,
12 the timer having a frequency lock loop.

13 Another aspect of the invention provides a radio frequency
14 communications device comprising an integrated circuit including a
15 transmitter and a receiver, the integrated circuit being configured to
16 periodically check if a radio frequency signal is being received by the
17 receiver, the integrated circuit further including a timer setting a time
18 period for the checking, the timer having a phase lock loop.

19 Another aspect of the invention provides a method for calibrating
20 a clock in a radio frequency data communication device for use in a
21 radio frequency identification device, the method comprising the following
22 steps: providing an integrated circuit having a receiver and a
23 transmitter, the integrated circuit including a timer having a frequency
24 lock loop configured to set a time period for periodically checking if

1 a radio frequency signal is being received by the receiver; configuring
2 the integrated circuit for connection with a battery to enable operation;
3 configuring the integrated circuit to receive and apply radio frequency
4 signals via an antenna, the antenna and the integrated circuit
5 cooperating in operation therebetween; and periodically checking whether
6 a radio frequency signal is being received by the receiver.

7 Another aspect of the invention provides a radio frequency
8 identification device for receiving and responding to radio frequency
9 commands from an interrogator transmitting a radio frequency signal, the
10 device comprising an integrated circuit including a receiver, a
11 transmitter, and a connection pin, the integrated circuit being switchable
12 between a radio frequency receive mode wherein the receiver receives
13 commands via radio frequency, and a direct receive mode wherein
14 commands are received via the connection pin.

15 Another aspect of the invention provides a radio frequency
16 identification device for receiving and responding to radio frequency
17 commands from an interrogator transmitting a radio frequency signal, the
18 device comprising an integrated circuit including a receiver, a
19 transmitter, and a digital input pin, the integrated circuit being
20 switchable between a radio frequency receive mode wherein the receiver
21 receives commands via radio frequency, and a direct receive mode
22 wherein commands are received digitally via the digital input pin.
23 Another aspect of the invention provides a radio frequency identification
24 device for receiving and responding to radio frequency commands from

1 an interrogator transmitting a radio frequency signal, the device
2 comprising an integrated circuit including a receiver, a transmitter, and
3 a connection pin, the integrated circuit being switchable between a radio
4 frequency receive mode wherein the receiver receives commands via
5 radio frequency, and a direct receive mode wherein a modulation signal
6 without a carrier is received via the connection pin.

7 Another aspect of the invention provides a radio frequency
8 identification device for receiving and responding to radio frequency
9 commands from an interrogator transmitting a radio frequency signal, the
10 device comprising an integrated circuit including a receiver, a
11 transmitter, and a connection pin, the integrated circuit being switchable
12 between a radio frequency transmit mode wherein the receiver transmits
13 responses to the commands via radio frequency, and a direct transmit
14 mode wherein responses are transmitted via the connection pin.

15 Another aspect of the invention provides a radio frequency
16 identification device for receiving and responding to radio frequency
17 commands from an interrogator transmitting a radio frequency signal, the
18 device comprising an integrated circuit including a receiver, a
19 transmitter, and a digital output pin, the integrated circuit being
20 switchable between a radio frequency transmit mode wherein the receiver
21 transmits responses to the commands via radio frequency, and a direct
22 transmit mode wherein responses are transmitted digitally via the digital
23 output pin.
24

1 Another aspect of the invention provides a radio frequency
2 identification device for receiving and responding to radio frequency
3 commands from an interrogator transmitting a radio frequency signal, the
4 device comprising an integrated circuit including a receiver, a
5 transmitter, and a connection pin, the integrated circuit being switchable
6 between a radio frequency transmit mode wherein the receiver transmits
7 responses to the commands via radio frequency, and a direct transmit
8 mode wherein a modulation signal without a carrier is transmitted via
9 the connection pin.

10 Another aspect of the invention provides a method comprising the
11 following steps: providing an integrated circuit having a receiver, a
12 transmitter, and a connection pin, the integrated circuit including a
13 switchable circuit configured to switch between a radio frequency receive
14 mode wherein the receiver receives commands via radio frequency, and
15 a direct receive mode wherein commands are received via the
16 connection pin; configuring the integrated circuit for connection with a
17 battery; configuring the integrated circuit to receive and transmit radio
18 frequency signals via an antenna, the antenna and the integrated circuit
19 cooperating in operation; and switching to one of the radio frequency
20 receive mode and the direct receive mode to enable receipt of radio
21 frequency commands or commands received via the connection pin.

22 Another aspect of the invention provides a method comprising the
23 following steps: providing an integrated circuit having a receiver, a
24 transmitter, and a connection pin, the integrated circuit including a

1 switchable circuit configured to switch between a radio frequency
2 transmit mode wherein the transmitter transmits information via radio
3 frequency, and a direct transmit mode wherein data is transmitted via
4 the connection pin; configuring the integrated circuit for connection with
5 a battery; configuring the integrated circuit to receive and transmit radio
6 frequency signals via an antenna, the antenna and the integrated circuit
7 cooperating in operation; and switching to one of the radio frequency
8 transmit mode and the direct transmit mode to enable transmission of
9 information via radio frequency or via the connection pin.

10 Another aspect of the invention provides an integrated circuit
11 comprising a radio frequency receiver; a unique, non-alterable indicia
12 identifying the integrated circuit; and a radio frequency transmitter
13 configured to transmit a signal representative of the indicia in response
14 to a command received by the receiver.

15 Another aspect of the invention provides a radio frequency
16 identification device comprising an integrated circuit including a receiver
17 for receiving radio frequency commands from an interrogation device,
18 and a transmitter for transmitting a signal identifying the device to the
19 interrogator, the transmitter and receiver being formed on a die having
20 a lot number, wafer number, and die number, the integrated circuit
21 including non-alterable indicia identifying the lot number, wafer number,
22 and die number, the transmitter being configured to transmit the non-
23 alterable indicia in response to a manufacturer's command received by
24

1 the receiver, the transmitted non-alterable indicia being different from
2 the identifying signal.

3 Another aspect of the invention provides a method of tracing
4 manufacturing process problems by tracing the origin of a defective
5 radio frequency identification integrated circuit, the method comprising:
6 forming a non-alterable indicia on a die for the integrated circuit, the
7 indicia representing the wafer lot number, wafer number, and die
8 number on the wafer, the indicia being not readily ascertainable by a
9 user; and causing the integrated circuit to transmit the non-alterable
10 indicia via radio frequency in response to a manufacturer's command.

11 Another aspect of the invention provides a method of tracing
12 stolen property including a radio frequency identification integrated
13 circuit, the method comprising: forming a non-alterable indicia on a die
14 for the integrated circuit, the indicia representing the wafer lot number,
15 wafer number, and die number on the wafer, the indicia being not
16 readily ascertainable by a user; and causing the integrated circuit to
17 transmit the non-alterable indicia via radio frequency in response to a
18 manufacturer's command.

19 Another aspect of the invention provides a method of tracing
20 manufacturing process problems in the manufacture of a radio frequency
21 integrated circuit by tracing defect origin, the method comprising the
22 following steps: providing a detectable signature on the integrated
23 circuit, the signature indicative of one or more of the wafer lot number,
24 wafer number, and die number of a die for the integrated circuit; and

1 enabling the integrated circuit to transmit the signature via radio
2 frequency responsive to an inquiry command.

3 Another aspect of the invention provides a radio frequency
4 identification device comprising: an integrated circuit including a
5 microprocessor, a receiver receiving radio frequency commands from an
6 interrogation device, and a transmitter transmitting a signal identifying
7 the device to the interrogator, the integrated circuit switching between
8 a sleep mode, and a microprocessor on mode, in which more power is
9 consumed than in the sleep mode, if the microprocessor determines that
10 a signal received by the receiver is a radio frequency command from
11 an interrogation device.

12 Another aspect of the invention provides a method for conserving
13 power during operation of a radio frequency identification device, the
14 method comprising the following steps: providing a receiver, a
15 transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry
16 configured to selectively supply clock signals to the processor and thus
17 control power consumption of the processor; configuring the receiver
18 with an antenna to receive radio frequency signals from an interrogation
19 device; configuring the transmitter to transmit a signal identifying the
20 device to the interrogator; selectively enabling powered wake-up of the
21 receiver to periodically check for presence of radio frequency signals;
22 detecting whether a radio frequency signal is valid; and depending on
23 whether a radio frequency signal is valid, supplying clock signals to the
24 processor.

1 Another aspect of the invention provides a method for conserving
2 power during operation of a radio frequency identification device, the
3 method comprising the following steps: providing a receiver, a
4 transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry
5 configured to selectively supply power to the processor; configuring the
6 receiver with an antenna to receive radio frequency signals from an
7 interrogation device; configuring the transmitter to transmit a signal
8 identifying the device to the interrogator; selectively enabling powered
9 wake-up of the receiver to periodically check for presence of radio
10 frequency signals; detecting whether a radio frequency signal is valid;
11 and depending on whether a radio frequency signal is valid, supplying
12 power signals to the processor.

13 Another aspect of the invention provides a radio frequency
14 identification device comprising an integrated circuit including a
15 microprocessor, a transmitter, and a receiver, the integrated circuit being
16 switchable between a sleep mode, and a microprocessor on mode in
17 which more power is consumed than in the sleep mode, the integrated
18 circuit being switched from the sleep mode to the microprocessor on
19 mode in response to a direct sequence spread spectrum modulated radio
20 frequency signal, which has a predetermined number of transitions within
21 a certain period of time, being received by the receiver.

22 Another aspect of the invention provides a method for conserving
23 power in a radio frequency identification device, the method comprising
24 periodically switching from a sleep mode to a receiver on mode and

1 performing the following tests to determine whether to further switch
2 to a microprocessor on mode because a valid radio frequency signal is
3 present: (a) determining if any radio frequency signal is present and,
4 if so, proceeding to step (b); and, if not, returning to the sleep mode;
5 and (b) determining if the radio frequency signal has a predetermined
6 number of transitions per a predetermined time period of time and, if
7 so, switching to the microprocessor on mode; and, if not, returning to
8 the sleep mode.

9 Another aspect of the invention provides a radio frequency
10 identification device switchable between a sleep mode and a mode in
11 which more power is consumed than in the sleep mode, the radio
12 frequency identification device comprising a transponder including a
13 receiver and a transmitter; means for periodically checking whether any
14 radio frequency signal is being received by the receiver; and means for
15 determining if a radio frequency signal has a predetermined number of
16 transitions within a predetermined period of time.

17 Another aspect of the invention provides a method for conserving
18 power in a radio frequency identification device, the method comprising
19 periodically switching from a sleep mode to a receiver on mode and
20 performing the following tests to determine whether to further switch
21 to a microprocessor on mode because a valid radio frequency signal is
22 present: (a) determining if any radio frequency signal is present and,
23 if so, proceeding to step (b); and, if not, returning to the sleep mode;
24 (b) determining if the radio frequency signal is modulated and has a

1 predetermined number of transitions per a predetermined period of time
2 and, if so, proceeding to step (c); and, if not, returning to the sleep
3 mode; and © determining if the modulated radio frequency signal has
4 a predetermined number of transitions per a predetermined period of
5 time different from the predetermined time of step (b) and, if so,
6 switching to the microprocessor on mode; and, if not, returning to the
7 sleep mode.

8 Another aspect of the invention provides a method of forming an
9 integrated circuit including a Schottky diode, the method comprising:
10 providing a p-type substrate; defining an n-type region relative to the
11 substrate; forming an insulator over the n-type region; removing an area
12 of the insulator for definition of a contact hole, and removing an area
13 encircling the contact hole; forming n⁺regions in the n-type regions
14 encircling the contact hole; depositing a Schottky metal in the contact
15 hole; and annealing the metal to form a silicide interface to the n-type
16 region.

17 Another aspect of the invention provides a method of forming an
18 integrated circuit including a Schottky diode, the method comprising:
19 providing a substrate; defining a p-type region relative to the substrate;
20 forming an insulator over the p-type region; removing an area of the
21 insulator for definition of a contact hole, and removing an area
22 encircling the contact hole; forming p⁺regions in the p-type regions
23 encircling the contact hole; depositing a Schottky metal in the contact
24

1 hole; and annealing the Schottky metal to form a silicide interface to
2 the p-type region.

3 Another aspect of the invention provides a method of forming an
4 integrated circuit including a Schottky diode, the method comprising:
5 providing a p-type substrate; defining an n-well region relative to the
6 substrate; forming a BPSG insulator over the n-well region; etching away
7 an area of the BPSG for definition of a contact hole, and etching an
8 area encircling the contact hole; forming n+regions in the n-well regions
9 encircling the contact hole; depositing titanium in the contact hole; and
10 annealing the titanium to form a silicide interface to the n-well region.

11 Another aspect of the invention provides a method of forming an
12 integrated circuit including a Schottky diode, the method comprising:
13 providing an n-type substrate; defining a p-well region relative to the
14 substrate; forming a BPSG insulator over the p-well region; etching away
15 an area of the BPSG for definition of a contact hole, and etching an
16 area encircling the contact hole;
17 forming p+regions in the p-well regions encircling the contact hole;
18 depositing titanium in the contact hole; and annealing the titanium to
19 form a silicide interface to the p-well region.

20 Another aspect of the invention provides a radio frequency
21 communications system comprising an antenna; an integrated circuit
22 including a receiver having a Schottky diode detector including a
23 Schottky diode coupled to the antenna; and a current source connected
24 to drive current through the antenna and the Schottky diode.

1 Another aspect of the invention provides an integrated circuit for
2 radio frequency communications comprising an inductorless radio
3 frequency detector.

4 Another aspect of the invention provides a system comprising an
5 antenna; a transponder including a receiver having a Schottky diode
6 detector including a Schottky diode having a first terminal coupled to
7 the antenna and having a second terminal; and means for driving
8 current through both the antenna and the Schottky diode in a direction
9 from the first terminal to the second terminal.

10 Another aspect of the invention provides a system comprising an
11 antenna;

12 a transponder including a receiver having a Schottky diode detector
13 including a Schottky diode having a first terminal coupled to the
14 antenna and having a second terminal; and means for driving current
15 through both the antenna and the Schottky diode in a direction from
16 the second terminal to the first terminal. Another aspect of the
17 invention provides a system comprising an antenna;

18 a transponder including a receiver having a Schottky diode detector
19 including a Schottky diode having an anode coupled to the antenna and
20 having a cathode; and means for driving current through both the
21 antenna and the Schottky diode in a direction from the anode to the
22 cathode.

23 Another aspect of the invention provides a radio frequency
24 communications system comprising: an antenna; an integrated circuit

1 including a receiver having a Schottky diode detector including a
2 Schottky diode having an anode coupled to the antenna and having a
3 cathode, the Schottky diode detector further including a capacitor
4 connected between the cathode and ground, and including a capacitor
5 having a first contact connected to the cathode and having a second
6 contact defining an output of the Schottky diode detector; a current
7 source connected to the cathode to drive current through the antenna
8 and the Schottky diode in a direction from the anode to the cathode.

9 Another aspect of the invention provides a radio frequency
10 communications system comprising an antenna; an integrated circuit
11 including a receiver having a Schottky diode detector including a
12 Schottky diode having a cathode coupled to the antenna and having an
13 anode, the Schottky diode detector further including a capacitor
14 connected between the anode and ground, and including a capacitor
15 having a first contact connected to the anode and having a second
16 contact defining an output of the Schottky diode detector; and
17 a current source connected to the anode to drive current through the
18 antenna and the Schottky diode in a direction from the anode to the
19 cathode.

20 Another aspect of the invention provides a system comprising an
21 antenna; a transponder including a receiver having a Schottky diode
22 detector including a Schottky diode having a cathode coupled to the
23 antenna and having an anode; and means for driving current through
24

1 both the antenna and the Schottky diode in a direction from the anode
2 to the cathode.

3 Another aspect of the invention provides a method for realizing
4 an improved radio frequency detector for use in a radio frequency
5 identification device, the method comprising the following steps:
6 providing an integrated circuit and an antenna, the integrated circuit
7 having a receiver and a transmitter, the integrated circuit further having
8 a Schottky diode and a current source, with the Schottky diode in
9 operation being coupled to the antenna and the current source, the
10 Schottky diode and antenna cooperating there between to form an
11 inductorless radio frequency detector; applying a supply of power to the
12 integrated circuit device from a battery; and applying a desired current
13 across the Schottky diode to impart a desired impedance there across
14 relative to the impedance of the antenna.

15 Another aspect of the invention provides a frequency lock loop
16 comprising a current controlled oscillator including a plurality of
17 selectively engageable current mirrors, the frequency of oscillation of the
18 frequency lock loop varying in response to selection of the current
19 mirrors, the current mirrors including transistors operating in a
20 subthreshold mode.

21 Another aspect of the invention provides an integrated circuit
22 comprising a receiver, a transmitter, and a frequency lock loop including
23 a current source having a thermal voltage generator, a current
24 controlled oscillator having a plurality of selectively engageable current

1 mirrors multiplying up the current of the current source, the frequency
2 of oscillation of the frequency lock loop varying in response to selection
3 of the current mirrors, the current mirrors including transistors operating
4 in a subthreshold mode.

5 Another aspect of the invention provides a timing oscillator that
6 consumes less than one milliAmp.

7 Another aspect of the invention provides a method of constructing
8 a frequency lock loop including a current controlled oscillator having a
9 plurality of selectively engageable current mirrors, the frequency of
10 oscillation of the frequency lock loop varying in response to selection
11 of the current mirrors, the method comprising selecting current mirrors
12 to vary frequency of operation, and operating transistors in the current
13 mirrors in subthreshold mode.

14 Another aspect of the invention provides a method of operating
15 an integrated circuit including a receiver, a transmitter, and a frequency
16 lock loop including a current source having a thermal voltage generator,
17 a current controlled oscillator having a plurality of selectively engageable
18 current mirrors multiplying up the current of the current source, the
19 frequency of oscillation of the frequency lock loop varying in response
20 to selection of the current mirrors, the method comprising engaging
21 selected current mirrors and operating transistors in the current mirrors
22 in a subthreshold mode.

23 Another aspect of the invention provides an amplifier powered by
24 a selectively engageable voltage source, the amplifier comprising first and

1 second electrodes for receiving an input signal to be amplified, the
2 input electrodes being adapted to be respectively connected to coupling
3 capacitors; a differential amplifier having inputs respectively connected
4 to the first and second electrodes, and having an output; selectively
5 engageable resistances between the voltage source and respective inputs
6 of the differential amplifier and defining, with the coupling capacitors,
7 the high pass characteristics of the circuit; and second selectively
8 engageable resistances between the voltage source and respective inputs
9 of the differential amplifier, the second resistances respectively having
10 smaller values than the first mentioned resistances, the second resistances
11 being engaged then disengaged in response to the voltage source being
12 engaged.

13 Another aspect of the invention provides a radio frequency
14 identification device comprising an integrated circuit including a
15 microprocessor, a receiver receiving radio frequency commands from an
16 interrogation device, and a transmitter transmitting a signal identifying
17 the device to the interrogator, the integrated circuit switching between
18 a sleep mode, and a microprocessor on mode, in which more power is
19 consumed than in the sleep mode, if the microprocessor determines that
20 a signal received by the receiver is a radio frequency command from
21 an interrogation device, the integrated circuit further including an
22 amplifier powered by a selectively engageable voltage source engaged in
23 the microprocessor on mode but not in the sleep mode, the amplifier
24 including first and second electrodes for receiving an input signal to be

1 amplified, the input electrodes being adapted to be respectively
2 connected to coupling capacitors, a differential amplifier having inputs
3 respectively connected to the first and second electrodes, and having an
4 output, selectively engageable resistances between the voltage source and
5 respective inputs of the differential amplifier, second selectively
6 engageable resistances between the voltage source and respective inputs
7 of the differential amplifier, the second resistances respectively having
8 smaller values than the first mentioned resistances, the second resistances
9 being engaged then disengaged in response to the integrated circuit
10 switching from the sleep mode to the microprocessor on mode.
11 Another aspect of the invention provides a method of speeding power
12 up of an amplifier stage powered by a selectively voltage source and
13 including first and second electrodes for receiving an input signal to be
14 amplified, the input electrodes being adapted to be respectively
15 connected to coupling capacitors; a differential amplifier having inputs
16 respectively connected to the first and second electrodes, and having an
17 output; and selectively engageable resistances between the voltage source
18 and respective inputs of the differential amplifier, the method
19 comprising: shorting around the selectively engageable resistances for
20 a predetermined amount of time in response to the voltage source being
21 engaged.

22 Another aspect of the invention provides a radio frequency
23 communications system comprising an antenna; an integrated circuit
24 including a receiver having a Schottky diode detector including a

1 Schottky diode having an anode coupled to the antenna and having a
2 cathode, the Schottky diode detector further including a capacitor
3 connected between the cathode and ground, and including a capacitor
4 having a first contact connected to the cathode and having a second
5 contact defining an output of the Schottky diode detector, the integrated
6 circuit further including a clock recovery circuit recovering a clock from
7 rising edges only of a signal at the output of the Schottky diode
8 detector; and a current source connected to drive current through the
9 antenna and the Schottky diode in a direction from the anode to the
10 cathode.

11 Another aspect of the invention provides a radio frequency
12 communications system comprising an antenna; an integrated circuit
13 including a receiver having a Schottky diode detector including a
14 Schottky diode having a cathode coupled to the antenna and having an
15 anode, the Schottky diode detector further including a capacitor
16 connected between the anode and ground, and including a capacitor
17 having a first contact connected to the anode and having a second
18 contact defining an output of the Schottky diode detector, the integrated
19 circuit further including a clock recovery circuit recovering a clock from
20 falling edges only of a signal at the output of the Schottky diode
21 detector; and a current source connected to drive current through the
22 antenna and the Schottky diode in a direction from the anode to the
23 cathode.
24

1 Another aspect of the invention provides a method of recovering
2 a clock in a radio frequency communications system, the method
3 comprising: providing an antenna; providing a receiver having a
4 Schottky diode detector including a Schottky diode having an anode
5 coupled to the antenna and having a cathode, the Schottky diode
6 detector further including a capacitor connected between the cathode
7 and ground, and including a capacitor having a first contact connected
8 to the cathode and having a second contact defining an output of the
9 Schottky diode detector; driving current through the antenna and the
10 Schottky diode in a direction from the anode to the cathode; and
11 recovering a clock from rising edges only of a signal at the output of
12 the Schottky diode detector.

13 Another aspect of the invention provides a method of recovering
14 a clock in a radio frequency communications system, the method
15 comprising: providing an antenna; providing a receiver having a
16 Schottky diode detector including a Schottky diode having a cathode
17 coupled to the antenna and having an anode, the Schottky diode
18 detector further including a capacitor connected between the anode and
19 ground, and including a capacitor having a first contact connected to
20 the anode and having a second contact defining an output of the
21 Schottky diode detector; driving current through the antenna and the
22 Schottky diode in a direction from the anode to the cathode; and
23 recovering a clock from falling edges only of a signal at the output of
24 the Schottky diode detector.

1 Another aspect of the invention provides a stage for a voltage
2 controlled oscillator, the stage comprising a first transistor having a
3 control electrode defining a first input, and having first and second
4 power electrodes, the first power electrode defining a first node; a
5 second transistor having a control electrode defining a second input, and
6 having first and second power electrodes, the first power electrode of
7 the second transistor defining a second node; a current source connected
8 to the second power electrodes of the first and second transistors and
9 directing current away from the second power electrodes of the first
10 and second transistors; and means defining a variable resistance
11 connecting the first and second nodes to a supply voltage.

12 Another aspect of the invention provides a stage for a voltage
13 controlled oscillator, the stage comprising a first p-channel transistor
14 having a gate defining a control node, having a source adapted to be
15 connected to a supply voltage, and having a drain; a second p-channel
16 transistor having a gate connected to the control node, having a source
17 connected to the supply voltage, and having a drain; a first n-channel
18 transistor having a gate defining a first input, having a drain connected
19 to the drain of the first p-channel transistor and defining a first node,
20 and having a source; a second n-channel transistor having a gate
21 defining a second input, having a drain connected to the drain of the
22 second p-channel transistor and defining a second node, and having a
23 source; a current source connected to the sources of the first and
24 second n-channel transistors directing current from the sources of the

1 first and second n-channel transistors; a first resistor connected between
2 the supply voltage and the drain of the first n-type transistor; a second
3 resistor connected between the supply voltage and drain of the second
4 n-type transistor; a first source follower having an input connected to
5 the first node and having an output defining a first output of the stage;
6 and a second source follower having an input connected to the second
7 node and having an output defining a second output of the stage.

8 Another aspect of the invention provides a transmitter including
9 a ring oscillator having a chain of stages, each stage comprising a first
10 p-channel transistor having a gate defining a control node, having a
11 source adapted to be connected to a supply voltage, and having a
12 drain; a second p-channel transistor having a gate connected to the
13 control node, having a source connected to the supply voltage, and
14 having a drain; a first n-channel transistor having a gate defining a first
15 input, having a drain connected to the drain of the first p-channel
16 transistor and defining a first node, and having a source; a second
17 n-channel transistor having a gate defining a second input, having a
18 drain connected to the drain of the second p-channel transistor and
19 defining a second node, and having a source; a current source
20 connected to the sources of the first and second n-channel transistors
21 directing current from the sources of the first and second n-channel
22 transistors; a first resistor connected between the supply voltage and the
23 drain of the first n-type transistor; a second resistor connected between
24 the supply voltage and drain of the second n-type transistor; a first

1 source follower having an input connected to the first node and having
2 an output defining a first output of the stage; and a second source
3 follower having an input connected to the second node and having an
4 output defining a second output of the stage.

5 Another aspect of the invention provides a method of varying
6 frequency in a stage of a voltage controlled oscillator having two input
7 transistors having gates defining input nodes and having drain to source
8 paths adapted to be connected between a supply voltage and a current
9 source, the method comprising providing an impedance between the
10 input transistors and the supply voltage, and varying the impedance.

11 Another aspect of the invention provides a frequency doubler
12 comprising a first Gilbert cell; a second Gilbert cell coupled to the first
13 Gilbert cell; a frequency generator configured to apply a first sinusoidal
14 wave to the first Gilbert cell; and a phase shifter applying a sinusoidal
15 wave shifted from the first sinusoidal wave to the second Gilbert cell.

16 Another aspect of the invention provides a frequency doubler
17 comprising a first Gilbert cell including a first pair of transistors having
18 sources that are connected together, a second pair of transistors having
19 sources that are connected together, a first one of the transistors of the
20 first pair having a gate defining a first input node and a first one of
21 the transistors of the second pair having a gate connected to the first
22 input node, a second one of the transistors of the first pair having a
23 gate defining a second input node and a second one of the transistors
24 of the second pair having a gate connected to the second input node,

1 the first transistor of the first pair having a drain, and the second
2 transistor of the second pair having a drain connected to the drain of
3 the first transistor of the first pair, the second transistor of the first
4 pair having a drain, and the first transistor of the second pair having
5 a drain connected to the drain of the second transistor of the first
6 pair, a third pair including first and second transistors having sources
7 coupled together, the first transistor of the third pair having a drain
8 connected to the source of the second transistor of the first pair, the
9 second transistor of the third pair having a drain connected to the
10 source of the second transistor of the second pair, and a current source
11 connected to the sources of the third pair and forward biasing the third
12 pair, the second transistor of the third pair having a gate defining a
13 third input node, and the first transistor of the third pair having a gate
14 defining a fourth input node; and a second Gilbert cell including a first
15 pair of transistors having sources that are connected together, a second
16 pair of transistors having sources that are connected together, a first
17 one of the transistors of the first pair of the second cell having a gate
18 defining a first input node and a first one of the transistors of the
19 second pair of the second cell having a gate connected to the first
20 input node of the second cell, a second one of the transistors of the
21 first pair of the second cell having a gate defining a second input node
22 of the second cell and a second one of the transistors of the second
23 pair of the second cell having a gate connected to the second input
24 node of the second cell, the first transistor of the first pair of the

1 second cell having a drain, and the second transistor of the second pair
2 of the second cell having a drain connected to the drain of the first
3 transistor of the first pair of the second cell, the second transistor of
4 the first pair of the second cell having a drain, and the first transistor
5 of the second pair of the second cell having a drain connected to the
6 drain of the second transistor of the first pair of the second cell, a
7 third pair including first and second transistors having sources coupled
8 together, the first transistor of the third pair of the second cell having
9 a drain connected to the source of the second transistor of the first
10 pair of the second cell, the second transistor of the third pair of the
11 second cell having a drain connected to the source of the second
12 transistor of the second pair of the second cell, and a current source
13 connected to the sources of the third pair of the second cell and
14 forward biasing the third pair of the second cell, the second transistor
15 of the third pair of the second cell having a gate defining a third input
16 node of the second cell, and the first transistor of the third pair of the
17 second cell having a gate defining a fourth input node of the second
18 cell; the drain of the second transistor of the first pair of the second
19 cell being connected to the drain of the second transistor of the first
20 pair of the first cell, the drain of the second transistor of the second
21 pair of the second cell being connected to the drain of the second
22 transistor of the second pair of the second cell, the first input node of
23 the second cell being connected to the fourth input node of the first
24 cell, the third input node of the second cell being connected to the

1 second input node of the first cell, and the fourth input node of the
2 second cell being connected to the first input node of the first cell.

3 Another aspect of the invention provides a method of doubling
4 frequency without using a feedback loop, the method comprising:
5 providing a first Gilbert cell; providing a second Gilbert cell coupled to
6 the first Gilbert cell; applying a first sinusoidal wave to the first Gilbert
7 cell; and applying a sinusoidal wave shifted from the first sinusoidal
8 wave to the second Gilbert cell.

9 Another aspect of the invention provides a pseudo random number
10 generator comprising a linear feedback shift register switchably operable
11 in a first mode, and in a second mode wherein the shift register
12 consumes more power than in the first mode.

13 Another aspect of the invention provides a method of generating
14 a pseudo random number, the method comprising providing a linear
15 feedback shift register; providing an oscillator which generates clock
16 signals used by the linear feedback shift register for shifting; and
17 providing a first power level to the oscillator when a pseudo random
18 number is required, and providing a second power level, lower than the
19 first power level, to the oscillator at other times. Another aspect of
20 the invention provides a method of generating a pseudo random
21 number, the method comprising: providing a linear feedback shift
22 register; providing an oscillator which generates clock signals used by
23 the linear feedback shift register for shifting; and operating the
24 oscillator at a first frequency in response to a request for a pseudo

1 random number, and operating the oscillator at a second frequency
2 lower than the first frequency after the pseudo random number is
3 generated.

4 Another aspect of the invention provides a system comprising a
5 microprocessor operating at a frequency; a linear feedback shift register
6 operable in a low power mode, wherein the shift register operates at
7 a frequency below the frequency of the microprocessor, and a high
8 power mode wherein the shift register consumes more power than in
9 the low power mode, operates at the frequency of the microprocessor,
10 and shifts data into the microprocessor.

11 Another aspect of the invention provides a radio frequency
12 identification device comprising an integrated circuit including a receiver,
13 a transmitter, a thermal voltage generator, a microprocessor operating
14 at a frequency, a linear feedback shift register operable in a low power
15 mode, wherein the shift register operates at a frequency below the
16 frequency of the microprocessor, and a high power mode wherein the
17 shift register consumes more power than in the low power mode,
18 operates at the frequency of the microprocessor, and shifts data into the
19 microprocessor, an oscillator supplying clock signals to the shift register,
20 and current mirrors supplying current to each stage of the shift register,
21 the current mirrors being referenced to the thermal voltage generator
22 when the shift register is in the low power mode, and, when the shift
23 register is in the high power mode, connected to a supply voltage
24

1 potential greater than the potential provided by the thermal voltage
2 generator.

3 Another aspect of the invention provides a method of generating
4 a pseudo random number, the method comprising: providing a thermal
5 voltage generator, a linear feedback shift register, an oscillator supplying
6 clock signals to the shift register, and current mirrors supplying current
7 to each stage of the shift register; referencing the current mirrors to
8 the thermal voltage generator when no pseudo random number is
9 required; and connecting the current mirrors to a supply voltage
10 potential greater than the potential provided by the thermal voltage
11 generator when a pseudo random number is required.

12 Another aspect of the invention provides an integrated circuit
13 comprising a receiver and a transmitter sharing a common antenna.

14 Another aspect of the invention provides a method of using an
15 integrated circuit including a receiver and a transmitter, the method
16 comprising connecting the receiver and transmitter to a common
17 antenna.

18 Another aspect of the invention provides an integrated circuit
19 comprising:

20 a die including a transmitter having an antenna output and a detector
21 having an antenna input; a package housing the die; a first contact
22 connected to the antenna output and accessible from outside the
23 package; a second contact connected to the antenna input and accessible
24

1 from outside the package; and a short electrically connecting the first
2 contact to the second contact outside the package.

3 Another aspect of the invention provides a method of using an
4 integrated circuit including a die having a transmitter including an
5 antenna output and a detector including an antenna output, the
6 integrated circuit further including a package housing the die, a first
7 contact connected to the antenna output and accessible from outside the
8 package, and a second contact connected to the antenna input and
9 accessible from outside the package, the method comprising: electrically
10 shorting the first contact to the second contact outside the package.

11 Another aspect of the invention provides a transceiver comprising
12 an antenna having a first end connected to a bias voltage, and having
13 a second end; a detector including a Schottky diode having an anode
14 connected to the second end of the antenna; and a transmitter having
15 an output connected to the second end of the antenna.

16 Another aspect of the invention provides a radio frequency
17 identification device comprising an integrated circuit including both a
18 receiver and a transmitter; a first antenna connected to the receiver;
19 and a second antenna connected to the transmitter.

20 Another aspect of the invention provides a transceiver comprising
21 a loop antenna having a first end connected to a bias voltage, and
22 having a second end; a second antenna; a detector including a Schottky
23 diode having an anode connected to the second end of the antenna;
24 and a transmitter having an output connected to the second antenna.

1 Another aspect of the invention provides a transceiver comprising
2 an antenna having a first end connected to a bias voltage, and having
3 a second end; a detector including a Schottky diode having an anode
4 connected to the second end of the antenna; and an active transmitter
5 having an output connected to the second end of the antenna.

6 Another aspect of the invention provides a transceiver comprising
7 an antenna having a first end, and having a second end; a detector
8 including a Schottky diode having a cathode connected to the second
9 end of the antenna and defining a potential at the second end of the
10 antenna, the first end of the antenna being connected to a potential
11 lower than the potential of the second end of the antenna; and a
12 backscatter transmitter including a transistor having a first power
13 electrode connected to the first end of the antenna, a second power
14 electrode connected to the second end of the antenna, and a control
15 electrode adapted to have a modulation signal applied thereto.

16 Another aspect of the invention provides a transceiver in
17 accordance with claim and further comprising a current source directing
18 current in the direction from the anode to the cathode.

19 Another aspect of the invention provides a transceiver comprising
20 a loop antenna having a first end connected to a bias voltage, and
21 having a second end; a detector including a Schottky diode having an
22 anode connected to the second end of the antenna; a backscatter
23 transmitter having a first output and having a second output; a
24 capacitor connected between the first output and the first end of the

1 antenna; and a capacitor connected between the second output and the
2 second end of the antenna.

3 Another aspect of the invention provides a method of configuring
4 a transceiver including a backscatter transmitter having first and second
5 outputs, and a detector having a Schottky diode including an anode, the
6 method comprising: applying a bias voltage to a first end of an
7 antenna; connecting a second end of the antenna to the anode;
8 connecting a capacitor between the first output and the first end of the
9 antenna; and connecting a capacitor between the second output and the
10 second end of the antenna.

11 Another aspect of the invention provides a method of arranging
12 a transceiver including a backscatter transmitter and a detector having
13 a Schottky diode including a cathode, the method comprising:
14 connecting a first end of an antenna to a ground potential; connecting
15 a second end of the antenna to the cathode; and connecting a first
16 power electrode of a transistor to the first end of the antenna;
17 connecting a second power electrode connected to the second end of
18 the antenna; and connecting a control electrode of the transistor to a
19 modulation signal.

20 Another aspect of the invention provides a method of determining
21 when a phase lock loop achieves frequency lock relative to a desired
22 frequency, the phase lock loop including a voltage controlled oscillator
23 having a control node and oscillating at a frequency responsive to the
24 voltage applied to the control node, the method comprising: crossing

1 the voltage that would result in the phase lock loop tracking the
2 desired frequency in a first direction; crossing the voltage that would
3 result in the phase lock loop tracking the desired frequency in a second
4 direction opposite the first direction; and indicating that frequency lock
5 has been achieved.

6 Another aspect of the invention provides a method of determining
7 when frequency lock occurs relative to a desired frequency, the method
8 comprising:

9 providing a phase lock loop including a voltage controlled oscillator that
10 oscillates at a frequency responsive to voltage applied to the voltage
11 controlled oscillator; applying a voltage to the voltage controlled
12 oscillator to produce a frequency of oscillation less than the desired
13 frequency; increasing the voltage applied to the voltage controlled
14 oscillator using one or more steps of a first size; increasing the voltage
15 applied to the voltage controlled oscillator using one or more steps of
16 a second size smaller than the first size; decreasing the voltage applied
17 to the voltage controlled oscillator using one or more steps of a third
18 size smaller than the second size; increasing the voltage applied to the
19 voltage controlled oscillator using a step of the third size; and indicating
20 that lock has occurred in response to the increase of the step of the
21 third size.

22 Another aspect of the invention provides a method of determining
23 when a phase lock loop achieves frequency lock relative to a desired
24 frequency, the phase lock loop including a voltage controlled oscillator

1 having a control node and oscillating at a frequency responsive to the
2 voltage applied to the control node, the method comprising: increasing
3 the voltage applied to the control node to a voltage above the voltage
4 that would result in the phase lock loop tracking the desired frequency;
5 decreasing the voltage applied to the control node to a voltage below
6 the voltage that would result in the phase lock loop tracking the
7 desired frequency; and increasing the voltage applied to the control
8 node and indicating that frequency lock has been achieved.

9 Another aspect of the invention provides a radio frequency
10 identification device comprising an integrated circuit including a
11 microprocessor, a transmitter, and a receiver, the integrated circuit
12 periodically switching between a sleep mode, and a receiver-on mode in
13 which more power is consumed than in the sleep mode, and further
14 including a selectively engageable timer preventing switching from the
15 sleep mode to the receiver-on mode for a predetermined amount of
16 time.

17 Another aspect of the invention provides a radio frequency
18 identification device comprising an integrated circuit including a
19 microprocessor, a transmitter, and a receiver, the integrated circuit
20 periodically switching between a sleep mode, and a receiver-on mode in
21 which more power is consumed than in the sleep mode, and further
22 including means for selectively preventing switching from the sleep mode
23 to the receiver-on mode for a predetermined amount of time.
24

1 Another aspect of the invention provides a radio frequency
2 identification device comprising an integrated circuit including a
3 microprocessor, a transmitter, and a receiver, the integrated circuit being
4 switchable between a sleep mode, and a mode in which more power is
5 consumed than in the sleep mode, the integrated circuit being switched
6 from the sleep mode to the mode in which more power is consumed
7 in response to a direct sequence spread spectrum modulated radio
8 frequency signal being received by the receiver which has a
9 predetermined number of transitions within a certain period of time, the
10 integrated circuit further including a selectively engageable timer which
11 prevents switching from the sleep mode for a period of time regardless
12 of whether a signal is subsequently received by the receiver which has
13 the predetermined number of transitions within a certain period of time.

14 Another aspect of the invention provides a method for conserving
15 power in a radio frequency identification device, the method comprising:
16 periodically switching from a sleep mode to a receiver on mode and
17 performing tests to determine whether to further switch to a
18 microprocessor on mode because a valid radio frequency signal is
19 present; and selectively disabling the periodic switching from the sleep
20 mode for a predetermined amount of time.

21
22 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

1 This disclosure of the invention is submitted in furtherance of the
2 constitutional purposes of the U.S. Patent Laws "to promote the
3 progress of science and useful arts" (Article 1, Section 8).

4 5 Overview of Device

6 Fig. 1 illustrates a radio frequency data communication device 12
7 embodying the invention. The radio frequency data communication
8 device 12 includes an integrated circuit 16, a power source 18 connected
9 to the integrated circuit 16 to supply power to the integrated circuit 16,
10 and at least one antenna 14 connected to the integrated circuit 16 for
11 radio frequency transmission and reception by the integrated circuit 16.
12 For purposes of this disclosure, including the appended claims, the term
13 "integrated circuit" shall be defined as a combination of interconnected
14 circuit elements inseparably associated on or within a continuous
15 substrate. For purposes of this disclosure, including the appended
16 claims, the term "semiconductive substrate" is defined to mean any
17 construction comprising semiconductive material, including, but not limited
18 to, bulk semiconductive materials such as a semiconductive wafer (either
19 alone or in assemblies comprising other materials thereon), and
20 semiconductive material layers (either alone or in assemblies comprising
21 other materials). For purposes of this disclosure, including the
22 appended claims, the term "substrate" refers to any supporting structure,
23 including, but not limited to, the semiconductive substrates described
24 above. In the illustrated embodiment, the integrated circuit 16 is a

1 monolithic integrated circuit. For purposes of this disclosure, including
2 the appended claims, the term "monolithic integrated circuit" shall be
3 defined as an integrated circuit wherein all circuit components are
4 manufactured into or on top of a single chip of silicon. The integrated
5 circuit 16 will be described in greater detail below. The power
6 source 18 is a battery or other suitable power source.

8 Housing

9 The radio frequency data communication device 12 can be
10 included in any appropriate housing or packaging.

11 Fig. 2 shows but one example in the form of an employee
12 identification badge 10 including the radio frequency data communication
13 device 12, and a card 11 made of plastic or other suitable material.
14 In one embodiment, the radio frequency data communication device 12
15 is laminated to the back face of the plastic card 11, and the card
16 forms the visible portion of the badge. In another embodiment, the
17 radio frequency data communication device 12 is bonded to the back
18 face of the card by embedding it within a thin bond line of epoxy-
19 based material. Alternatively, the radio frequency data communication
20 device 12 is embedded into the plastic card 11. In one embodiment,
21 the front face of the badge 10 has visual identification features
22 including an employee photograph as well as identifying text.

23 Fig. 3 illustrates but one alternative housing supporting the
24 device 12. More particularly, Fig. 3 shows a miniature housing 20

1 encasing the device 12 to define a tag which can be supported by an
2 object (e.g., hung from an object, affixed to an object, etc.). The
3 housing 20 preferably has the general shape and size, in plan view, of
4 a postage stamp. The embodiment of Fig. 3 also includes a card 21
5 supporting the device 12 in the housing 20. The card 21 is formed of
6 plastic or other suitable material having a thickness of about 0.040
7 inches, a width of about 1.25 inches, and a height of about 1.25 inches.
8 In one embodiment, the device 12 is bonded to a back face of the
9 card 21 with a thin layer of non-conductive epoxy material that
10 cooperates with the card to define the housing 20.

11 Although two particular types of housings have been disclosed, the
12 device 12 can be included in any appropriate housing. The device 12
13 is of a small size that lends itself to applications employing small
14 housings, such as cards, miniature tags, etc. Larger housings can also
15 be employed. The device 12, housed in any appropriate housing, can
16 be supported from or attached to an object in any desired manner; for
17 example using double sided tape, glue, lanyards, leash, nails, staples,
18 rivets, or any other fastener. The housing can be sewn on to an
19 object, hung from an object, implanted in an object (hidden), etc.

20 21 Antenna

22 Various configurations are possible for the antenna 14. The
23 integrated circuit 16 includes a receiver 30 and a transmitter 32
24 (Fig. 5). In one embodiment, separate antennas 44 and 46 are

1 provided for receiver and transmitter of the integrated circuit 16. In
2 another embodiment (Fig. 1), a single antenna is shared by the receiver
3 and transmitter sections. In one embodiment, the antenna is defined
4 by conductive epoxy screened onto a card or housing. In the illustrated
5 embodiment, the antenna is conductively bonded to the integrated circuit
6 via bonding pads.

7 In an embodiment where a single antenna is employed, that single
8 antenna preferably comprises a folded dipole antenna defining a
9 continuous conductive path, or loop, of microstrip. Alternatively, the
10 antenna can be constructed as a continuous loop antenna.

11 Battery

12 If the power source 18 is a battery, the battery can take any
13 suitable form. Preferably, the battery type will be selected depending
14 on weight, size, and life requirements for a particular application. In
15 one embodiment, the battery 18 is a thin profile button-type cell
16 forming a small, thin energy cell more commonly utilized in watches and
17 small electronic devices requiring a thin profile. A conventional button-
18 type cell has a pair of electrodes, an anode formed by one face and
19 a cathode formed by an opposite face. Exemplary button-type cells are
20 disclosed in several pending U.S. patent applications including U.S.
21 Patent Application Serial No. 08/205,957, "Button-Type Battery Having
22 Bendable Construction and Angled Button-Type Battery," listing Mark E.
23 Tuttle and Peter M. Blonsky as inventors; U.S. Patent Application Serial
24

1 No. 08/321,251, "Button-Type Batteries and Method of Forming Button-
2 Type Batteries," listing Mark E. Tuttle as inventor; and U.S. Patent
3 Application Serial No. 08/348,543, "Method of Forming Button-Type
4 Batteries and a Button-Type Battery Insulating and Sealing Gasket,"
5 listing Mark E. Tuttle as inventor. These patent applications and
6 resulting patents are hereby incorporated by reference. In an
7 alternative embodiment, the battery 18 comprises a series connected pair
8 of button type cells. Instead of using a battery, any suitable power
9 source can be employed.

10 11 Overview of Communication System

12 Fig. 4 illustrates a radio frequency communication system 24
13 including the device 12 and a radio frequency interrogator unit
14 (hereinafter "interrogator") 26. The device 12 transmits and receives
15 radio frequency communications to and from the interrogator 26.
16 Preferably, the interrogator unit 26 includes an antenna 28, as well as
17 dedicated transmitting and receiving circuitry, similar to that implemented
18 on the integrated circuit 16. The system 24 further includes a host
19 computer 48 in communication with the interrogator 26. The host
20 computer 48 acts as a master in a master-slave relationship with the
21 interrogator 26. The host computer 48 includes an applications program
22 for controlling the interrogator 26 and interpreting responses, and a
23 library ("MRL") of radio frequency identification device applications or
24 functions. Most of the functions communicate with the interrogator 26.

1 These functions effect radio frequency communication between the
2 interrogator 26 and the device 12. These functions are described below
3 in a section titled "Protocol."

4 One example of an interrogator implemented in combination with
5 a transponder unit is disclosed in U.S. Patent No. 4,857,893, hereby
6 incorporated by reference. Generally, the interrogator 26 includes an
7 antenna 28, and transmits an interrogation signal or command 27
8 ("forward link") via the antenna 28. The device 12 receives the
9 incoming interrogation signal via its antenna 14. Upon receiving the
10 signal 27, the device 12 responds by generating and transmitting a
11 responsive signal or reply 29 ("return link"). Preferably, the responsive
12 signal 29 is encoded with information that uniquely identifies, or labels
13 the particular device 12 that is transmitting, so as to identify any object
14 or person with which the device 12 is associated.

15 In the illustrated embodiment in Fig. 4, there is no communication
16 between devices 12. Instead, the devices 12 communicate with the
17 interrogator 26. Fig. 4 illustrates the device 12 as being in the
18 housing 20 of Fig. 3. The system 24 would operate in a similar
19 manner if the device 12 is provided in a housing such as the
20 housing 10 of Fig. 2, or any other appropriate housing. Multiple
21 devices 12 can be used in the same field of an interrogator 26 (i.e.,
22 within communications range of an interrogator 26). Similarly, multiple
23 interrogators 26 can be in proximity to one or more of the devices 12.

1 Various U.S. patent applications, which are incorporated herein by
2 reference, disclose features that are employed in various alternative
3 embodiments of the invention: 08/092,147, filed July 15, 1993, "Wake
4 Up Device for a Communications System" and continuation application
5 08/424,827, filed April 19, 1995, "Wake Up Device for a
6 Communications System"; 08/281,384, filed July 27, 1994, "Communication
7 System Having Transmitter Frequency Control"; 07/990,918, filed
8 December 15, 1992, now U.S. Patent No. 5,365,551, "Data
9 Communication Transceiver Using Identification Protocol"; 07/899,777,
10 filed June 17, 1992, "Radio Frequency Identification Device (RFID) and
11 Method of Manufacture, Including an Electrical Operating System and
12 Method," now abandoned; 07/921,037, filed July 24, 1992, "Anti-Theft
13 Method for Detecting The Unauthorized Opening of Containers and
14 Baggage," now abandoned; 07/928,899, filed August 12, 1992, "Electrically
15 Powered Postage Stamp or Mailing or Shipping Label Operative with
16 Radio Frequency (RF) Communications," now abandoned; and 08/032,384,
17 filed on March 17, 1993, "Modulated Spread Spectrum in RF
18 Identification Systems Method," now allowed.

19 The above described system 24 is advantageous over prior art
20 devices that utilize magnetic field effect systems because, with the
21 system 24, a greater range can be achieved, and more information can
22 be obtained (instead of just an identification number).

23 As a result, such a system 24 can be used, for example, to
24 monitor large warehouse inventories having many unique products

1 needing individual discrimination to determine the presence of particular
2 items within a large lot of tagged products. The system can also be
3 used to counteract terrorism to monitor luggage entering a plane to
4 ensure that each item of luggage that enters the plane is owned by a
5 passenger who actually boards the plane. Such a technique assumes
6 that a terrorist will not board a plane that he or she is planning to
7 bomb. The system 24 is useful whenever RF transmission over a large
8 range is desirable, such as for inventory control. In one embodiment,
9 the sensitivity of the devices 12 is adjustable so that only devices within
10 a certain range of the interrogator 26 will respond. In another
11 embodiment, the power of the interrogator 26 is adjustable so that only
12 devices within a certain range of the interrogator 26 will respond.

13 However, a power conservation problem is posed by such
14 implementations where batteries are used to supply power to the
15 integrated circuits 16. If the integrated circuit 16 operates continuously
16 at full power, battery life will be short, and device 12 will have to be
17 frequently replaced. If the battery 18 is permanently sealed in a
18 housing, replacement of the battery will be difficult or impossible. For
19 example, one reason for sealing the battery with the integrated circuit
20 16 and antenna 14 in a housing is to simplify the design and
21 construction, to reduce the cost of production, and protect the electrical
22 interconnections between devices. Another reason is protection of the
23 battery and integrated circuit 16 from moisture and contaminants. A
24 third reason is to enhance the cosmetic appeal of the device 12 by

1 eliminating the need for an access port or door otherwise necessary to
2 insert and remove the battery. When the battery is discharged, the
3 entire badge or stamp is then discarded. It is therefore desirable in
4 this and other applications to incorporate power conservation techniques
5 into the integrated circuit 16 in order to extend useful life.

6 In one embodiment, the devices 12 switch between a "sleep" mode
7 of operation, and higher power modes to conserve energy and extend
8 battery life during periods of time where no interrogation signal 27 is
9 received by the device 12. These power conservation techniques are
10 described in greater detail below.

11 In one embodiment of the invention, in order to further extend
12 the life of the battery 18, the receiver sensitivity of the device 12 is
13 tuned over a range of tuned and detuned states in order to modify the
14 ability of the device to detect signal 27, and therefore adjust the
15 tendency for the device to wake up. One way to adjust the receiver
16 sensitivity is by adjusting the sensitivity, or impedance of the antenna.
17 Another way is by controlling the gain of amplifiers included in the
18 receiver. Another way is to adjust or switch in different circuit
19 elements in the device 12, thereby realizing different circuit
20 configurations. Additionally, the transmitting sensitivity for the device 12
21 can be adjusted. For example, transmitting range can be adjusted by
22 controlling interrogator continuous wave power if the transmitter is
23 operating in backscatter mode, and by controlling output power if the
24 transmitter is in active mode.

Overview of Integrated Circuit

Fig. 5 is a high level circuit schematic of the integrated circuit 16 utilized in the devices of Figs. 1-4. In the embodiment shown in Fig. 5, the integrated circuit 16 is a monolithic integrated circuit. More particularly, in the illustrated embodiment, the integrated circuit 16 comprises a single die, having a size of 209 x 116 mils², including the receiver 30, the transmitter 32, a micro controller or microprocessor 34, a wake up timer and logic circuit 36, a clock recovery and data recovery circuit 38, and a bias voltage and current generator 42.

In one embodiment, a spread spectrum processing circuit 40 is also included in the integrated circuit 16 and formed relative to the single die. In this embodiment, signals received by the receiver 30 are modulated spread spectrum signals. Spread spectrum modulation is described below. In the illustrated embodiment, the modulation scheme for replies sent by the transmitter 32 is selectable. One of the available selections for replies sent by the transmitter 32 is modulated spread spectrum.

Spread Spectrum Modulation

Many modulation techniques minimize required transmission bandwidth. However, the spread spectrum modulation technique employed in the illustrated embodiment requires a transmission bandwidth that is up to several orders of magnitude greater than the minimum required signal bandwidth. Although spread spectrum

1 modulation techniques are bandwidth inefficient in single user
2 applications, they are advantageous where there are multiple users, as
3 is the case with the instant radio frequency identification system 24.
4 The spread spectrum modulation technique of the illustrated embodiment
5 is advantageous because the interrogator signal can be distinguished from
6 other signals (e.g., radar, microwave ovens, etc.) operating at the same
7 frequency. The spread spectrum signals transmitted by the device 12
8 and by the interrogator 26 (Fig. 4) are pseudo random and have
9 noise-like properties when compared with the digital command or reply.
10 The spreading waveform is controlled by a pseudo-noise or pseudo
11 random number (PN) sequence or code (described below). The PN
12 code is a binary sequence that appears random but can be reproduced
13 in a predetermined manner by the device 12. More particularly,
14 incoming spread spectrum signals are demodulated by the device 12
15 through cross correlation with a version of the pseudo random carrier
16 that is generated by the device 12 itself. Cross correlation with the
17 correct PN sequence unspreads the spread spectrum signal and restores
18 the modulated message in the same narrow band as the original data.

19 A pseudo-noise or pseudo random sequence (PN sequence) is a
20 binary sequence with an autocorrelation that resembles, over a period,
21 the autocorrelation of a random binary sequence. The autocorrelation
22 of a pseudo-noise sequence also roughly resembles the autocorrelation
23 of band-limited white noise. A pseudo-noise sequence has many
24 characteristics that are similar to those of random binary sequences.

1 For example, a pseudo-noise sequence has a nearly equal number of
2 zeros and ones, very low correlation between shifted versions of the
3 sequence, and very low cross correlation between any two sequences.
4 A pseudo-noise sequence is usually generated using sequential logic
5 circuits. For example, a pseudo-noise sequence can be generated using
6 a feedback shift register.

7 A feedback shift register comprises consecutive stages of two state
8 memory devices, and feedback logic. Binary sequences are shifted
9 through the shift registers in response to clock pulses, and the output
10 of the various stages are logically combined and fed back as the input
11 to the first stage. The initial contents of the memory stages and the
12 feedback logic circuit determine the successive contents of the memory.

13 The illustrated embodiment employs direct sequence spread
14 spectrum modulation. A direct sequence spread spectrum (DSSS) system
15 spreads the baseband data by directly multiplying the baseband data
16 pulses with a pseudo-noise sequence that is produced by a pseudo-noise
17 generator. A single pulse or symbol of the PN waveform is called a
18 "chip." Synchronized data symbols, which may be information bits or
19 binary channel code symbols, are added in modulo-2 fashion to the
20 chips before being modulated. The receiver performs demodulation.
21 For example, in one embodiment the data is phase modulated, and the
22 receiver performs coherent or differentially coherent phase-shift keying
23 (PSK) demodulation. In another embodiment, the data is amplitude
24 modulated. Assuming that code synchronization has been achieved at

1 the receiver, the received signal passes through a wideband filter and
2 is multiplied by a local replica of the PN code sequence. This
3 multiplication yields the unspread signal.

4 A pseudo-noise sequence is usually an odd number of chips long.
5 In the illustrated embodiment, one bit of data is represented by a
6 thirty-one chip sequence. A zero bit of data is represented by inverting
7 the pseudo-noise sequence.

8 Spread spectrum techniques are also disclosed in the following
9 patent applications and patent, which are incorporated herein by
10 reference: U.S. Patent Application Serial No. 08/092,147; U.S. Patent
11 Application Serial No. 08/424,827, filed April 19, 1995; and U.S. Patent
12 No. 5,121,407 to Partyka et al. They are also disclosed, for example,
13 in "Spread Spectrum Systems," by R.C. Dixon, published by John Wiley
14 and Sons, Inc.

15 The system disclosed in U.S. Patent Application Serial No.
16 08/092,147 includes two receivers, a low power receiver for detecting a
17 wake up signal from an interrogator, and a high power receiver for
18 receiving commands from an interrogator. On the other hand, the
19 integrated circuit 16 of the illustrated embodiment employs a single
20 receiver for both wake up and receiving commands from an interrogator.
21 Another difference is that in the system 12 of the illustrated
22 embodiment the receiver, not the interrogator, controls wake up. In the
23 system 24 of the illustrated embodiment, the integrated circuit 16
24

1 includes a timer that causes the receiver and support circuitry to be
2 powered on periodically. This is described in greater detail elsewhere.

3 4 Backscatter and Frequency Hopping

5 The interrogator sends out a command that is spread around a
6 certain center frequency (e.g, 2.44 GHz). After the interrogator
7 transmits the command, and is expecting a response, the interrogator
8 switches to a CW mode (continuous wave mode). In the continuous
9 wave mode, the interrogator does not transmit any information.
10 Instead, the interrogator just transmits 2.44 GHz radiation. In other
11 words, the signal transmitted by the interrogator is not modulated.
12 After the device 12 receives the command from the interrogator, the
13 device 12 processes the command. If the device 12 is in a backscatter
14 mode it alternately reflects or does not reflect the signal from the
15 interrogator to send its reply. For example, in the illustrated
16 embodiment, two halves of a dipole antenna are either shorted together
17 or isolated from each other, as described below in greater detail. In
18 the illustrated embodiment, frequency hopping does not occur when the
19 interrogator transmits a command, but occurs when the interrogator is
20 in the continuous wave mode. The interrogator, in the continuous wave
21 mode, hops between various frequencies close to the 2.44 GHz
22 frequency. These various frequencies are sufficiently close to the 2.44
23 GHz frequency that backscatter antenna reflection characteristics of the
24 device 12 are not appreciably altered. Because the interrogator is

1 hopping between frequencies, the interrogator knows what frequency
2 backscatter reflections to expect back from the device 12. By hopping
3 between various frequencies, the amount of time the interrogator
4 continuously uses a single frequency is reduced. This is advantageous
5 in view of FCC regulatory requirements.

6 In the illustrated embodiment, no attempt is made to frequency
7 hop at the interrogator to a pseudo-random sequence and then correlate
8 to that at the receiver. However, in alternative embodiments, such
9 correlation takes place.

10 11 CMOS Process

12 The integrated circuit 16 is formed according to semiconductor
13 wafer processing steps, such as CMOS semiconductor wafer processing
14 steps used to form static random access memories. In the preferred
15 embodiment, the integrated circuit 16 is a single metal integrated circuit.
16 In other words, the integrated circuit 16 is formed using a single metal
17 layer processing method. More particularly, only one layer of metal
18 (e.g., aluminum) is employed. This is advantageous in that it results
19 in a lower cost of production.

20 In this processing method, a p-type wafer is employed. The
21 processing method employed provides n-well areas used to define
22 p-channel transistors; an active area which is used to define p+ and n+
23 diffused regions inside the p-type wafer or inside the n-well areas.
24 Next, a layer is provided that helps prevent leakage between adjacent

1 devices. Then, transistor are defined by forming n-type and p-type
2 polysilicon. Then, a contact layer is defined for connecting desired
3 intersections of polysilicon with metal (aluminum) that is subsequently
4 formed. The contact layer is also used, in some instances, for
5 connecting desired intersections of the metal that is subsequently formed
6 with active area. Then the metal layer is formed. The contact layer
7 provides a means for connecting metal with layers below the metal.
8 Then, a passivation step is performed. Passivation means that the die
9 is covered with a protective layer and holes are cut around the edge
10 of the die so that electrical connection can be made to the bond pads.

11 In some processing, after the metal layer is formed, an insulating
12 layer is provided, and another layer of aluminum is formed above the
13 insulating layer. Holes are provided at selected locations to
14 interconnect the top layer of aluminum with lower layers. An
15 advantage of using multiple layers of metal is that it provides greater
16 flexibility in how functional blocks are laid out and in how power is
17 bused to various areas. However, multiple metal layers add processing
18 steps. This results in added cost and complexity.

19 The process of the preferred embodiment employs only one layer
20 of metal, and is therefore a relatively simple, inexpensive process.

21 The following U.S. patents, which are incorporated herein by
22 reference, disclose CMOS processing techniques that are employed in
23 various alternative embodiments of the invention: 5,489,546 to Ahmad
24 et al.; 5,272,367 to Dennison et al.; and 5,134,085 to Gilgen et al.

1 Various other processing methods can be employed in alternative
2 embodiments.

3 4 Transmitter and Receiver

5 The receiver 30 is a radio frequency receiver included in the
6 integrated circuit 16, and the transmitter 32 is a radio frequency
7 transmitter included in the integrated circuit 16. In one embodiment,
8 the receiver 30 includes a Schottky diode detector. Various forms of
9 Schottky diode detectors are described in a paper titled "Designing
10 Detectors for RF/ID Tags," by Raymond W. Waugh of Hewlett-Packard
11 Company, submitted for presentation at the RF Expo, San Diego,
12 February 1, 1995, and incorporated herein by reference.

13 The receiver 30 of the illustrated embodiment makes use of the
14 rate or frequency of data included in incoming signals, but does not
15 make use of the carrier frequency of the incoming signal. In other
16 words, operation of the receiver 30 is independent of the frequency of
17 the carrier of the incoming signal over a wide range of carrier
18 frequencies.

19 Therefore, the device 12 can operate over a wide range of carrier
20 frequencies. For example, the device 12 can operate with carriers of
21 915-5800 MHZ. In a more particular embodiment, the device 12 can
22 operate with carrier frequencies in the 915, 2450, or 5800 MHZ bands.
23 In the illustrated embodiment, the antennas are half wave antennas, and
24 frequency selectivity of the device 12 is achieved based on selection of

1 the antenna external to the integrated circuit 16. Capacitors employed
2 in the Schottky diode detector are also selected based on the carrier
3 frequency that will be employed.

4 In one embodiment, the transmitter 32 is switchable between
5 operating in a modulated backscatter transmitter mode, and operating
6 in an active mode. The transmitter 32 switches between the backscatter
7 mode and the active mode in response to a radio frequency command,
8 instructing the transmitter to switch, sent by the interrogator 26 and
9 received by the receiver 30. In the active mode, a carrier for the
10 transmitter is extracted from a signal received by the receiver 30.

11 Active transmitters are known in the art. See, for example, U.S.
12 Patent Application Serial No. 08/281,384. U.S. Patent Application Serial
13 No. 08/281,384 also discloses how transmit frequency for the transmitter
14 32 is recovered from a message received via radio frequency from the
15 interrogator 26. The device 12 differs from the device disclosed in U.S.
16 Patent Application Serial No. 08/281,384 in that a VCO control voltage
17 is stored as an analog voltage level on a capacitor instead of as a
18 digital number in a register. Further, in the illustrated embodiment, the
19 recovered frequency is also used by the integrated circuit 16 to generate
20 a DPSK subcarrier for modulated backscatter transmission.

21 The transmitter is capable of transmitting using different
22 modulation schemes, and the modulation scheme is selectable by the
23 interrogator. More particularly, if it is desired to change the
24 modulation scheme, the interrogator sends an appropriate command via

1 radio frequency. The transmitter can switch between multiple available
2 modulation schemes such as Binary Phase Shift Keying (BPSK), Direct
3 Sequence Spread Spectrum, On-Off Keying (OOK), and Modulated
4 Backscatter (MBS).

6 Wake Up Timer and Logic Circuit

7 The integrated circuit 16 includes the wake up timer and logic
8 circuit 36 for conserving battery power. More particularly, the
9 integrated circuit 16 normally operates in a sleep mode wherein most
10 circuitry is inactive and there is a very low current draw on the
11 battery 18. One circuit that is active during the sleep mode is a timer
12 for waking up the integrated circuit at predetermined intervals. In the
13 illustrated embodiment, the interval is 16 milliseconds; however, various
14 other intervals can be selected by radio frequency by sending a message
15 from the interrogator 26 to the device 12. For example, in the
16 illustrated embodiment, the interval is selectable as being 0.5, 16, 64 or
17 256 milliseconds.

18 Assuming the selected interval is 16 milliseconds, after every sleep
19 period of 16 milliseconds the wake up timer and logic
20 circuit 36 activates the receiver 30, the clock recovery and data recovery
21 circuit 38, and all the bias currents and voltages associated with the
22 receiver 30. This is a receiver on mode, illustrated by a vertical line
23 marked WAKEUP RX ON in Fig. 27. Such bias currents and voltages

1 are generated by the bias voltage and current generator 42. The
2 receiver 30 then determines if there is a radio frequency signal present.

3 If there is no radio frequency signal present, the wake up timer
4 and logic circuit 36 deactivates the receiver 30 and clock recovery and
5 data recovery circuit 38. The receiver then goes back to sleep in the
6 low current mode until another 16 milliseconds pass (or whatever sleep
7 period is selected).

8 If there is a radio frequency signal present, the receiver will
9 unspread the spread spectrum signal for processing. It is possible that
10 while the receiver is on, it may detect a radio frequency signal from
11 a source other than the interrogator 26. For example, other radio
12 frequency transmitting devices may be operating in the area. In the
13 illustrated embodiment, the receiver is set to receive microwave
14 frequency signals, so that a small antenna can be used. Therefore, the
15 wake up timer and logic circuit 36 performs tests to determine if a
16 radio frequency signal received on wake up is valid. This is a wake
17 up abort test mode, illustrated by a vertical line marked WAKEUP
18 ABORT TESTS in Fig. 27. If the wake up timer and logic circuit 36
19 determines that the incoming signal is not valid, the integrated
20 circuit 16 returns to the sleep mode. The illustrated integrated
21 circuit 16 consumes approximately one micro amp in the sleep mode,
22 and the battery 18 is expected to last up to 10 years with a current
23 drain of that order, depending on how often radio frequency signals are
24 present and on the capacity of the battery.

1 If a radio frequency signal is detected upon wake up, the wake
2 up timer and logic compares the incoming signal to known
3 characteristics of expected spread spectrum encoded data. In the
4 illustrated embodiment, a valid incoming radio frequency signal will be
5 a spread spectrum signal having a thirty-one chip code representing a
6 single data bit. To represent a digital one ("1") the thirty-one chip
7 code is sent as is. To represent a digital zero ("0") the thirty-one chip
8 code is inverted. The wake up timer and logic circuit 36 knows how
9 many transitions there are in a valid thirty-one chip sequence, and
10 knows the time period within which all those transitions are expected
11 (or the frequency of the transitions). After the incoming radio
12 frequency signal is amplified and converted to baseband, it is tested
13 against known characteristics of a valid signal.

14 If the incoming signal does not pass these tests, the integrated
15 circuit 16 returns to the sleep mode. If the incoming signal does pass
16 these tests, then the wake up timer and logic circuit determines whether
17 the clock recovery and data recovery circuit 38 locks on to the clock
18 frequency contained in the chip rate of the incoming signal within a
19 predetermined time period. If frequency lock is obtained, the
20 microprocessor is turned on for processing of the received command.
21 this is a processor on mode illustrated by a vertical line marked
22 "PROCESSOR ON" in Fig. 27.

23 If frequency lock is not obtained within the predetermined time,
24 the integrated circuit 16 returns to the sleep mode.

1 Other appropriate tests can be performed in embodiments where
2 spread spectrum is not employed. In these embodiments, knowing how
3 valid data is encoded, the wake up timer and logic still compares the
4 number of transitions received in a given amount of time with an
5 expected number of transitions for a valid signal.

6 In summary, various tests are performed, and the order in which
7 they are performed is preferably selected to most quickly identify invalid
8 signals. U.S. Patent Application Serial No. 08/424,827, filed April 19,
9 1995 and U.S. Patent Application Serial No. 08/092,147, which are
10 incorporated herein by reference, disclose tests that could be employed
11 in various alternative embodiments of the invention.

12 After the wake up timer and logic circuit 36 determines that a
13 received signal is valid, the integrated circuit 16 then performs clock
14 recovery. To save space and cost, the preferred device 12 does not
15 include a crystal timing element (clock). Instead, all timing for the
16 device 12 is extracted from valid incoming signals received by the
17 receiver 30.

18 In one embodiment, a valid incoming radio frequency signal is
19 digital, and starts with a preamble, which is followed by a start code
20 (or Barker code), which is followed by data (e.g., a command). For
21 example, in the illustrated embodiment, the preamble is a long (e.g.,
22 eighteen milliseconds) string of zeros; i.e., the thirty-one chip sequence
23 is inverted, and sent repeatedly for approximately 18 milliseconds. In
24

1 the illustrated embodiment the data or command after the Barker code
2 is shorter than the preamble, and is approximately 4 milliseconds long.

3 4 Clock Recovery and Data Recovery Circuit

5 The clock for the entire integrated circuit 16 is extracted from
6 the incoming message itself. In one embodiment, the transmitter 32 is
7 selectable as being operable in an active transmission mode, or a
8 backscatter mode. If the transmitter 32 is operating in an active mode,
9 the extracted clock is multiplied up to the carrier frequency of the
10 transmitter 32. For example, in one embodiment, the transmitter carrier
11 frequency is 2.44 GHz. The choice of chip rate is a function of the
12 carrier frequency and the carrier frequency has to be divisible by a
13 power of two to give the chip rate on the input.

14 If the transmitter 32 is operating in a backscatter mode, the clock
15 that has been recovered from the incoming signal received by the
16 receiver 30 is divided to make it slower and is then used for frequency
17 shift key or phase shift key modulated backscatter.

18 In summary, a clock is recovered from the incoming message, and
19 used for timing for the micro controller 34 and all the other clock
20 circuitry on the chip, and also for deriving the transmitter carrier or
21 the subcarrier, depending on whether the transmitter is operating in
22 active mode or backscatter mode.

23 Note that there are disadvantages to generating a transmit
24 frequency in this fashion. In an alternative embodiment (not shown),

1 a crystal is employed to generate a clock. A crystal provides a more
2 stable, reliable clock to generate the transmit frequency, but also
3 increases cost and size of the device 12.

4 In addition to recovering a clock, the clock recovery and data
5 recovery circuit 38 also performs data recovery on valid incoming
6 signals. The valid spread spectrum incoming signal is passed through
7 the spread spectrum processing circuit 40, and the spread spectrum
8 processing circuit 40 extracts the actual ones and zeros of data from
9 the incoming signal. More particularly, the spread spectrum processing
10 circuit 40 takes the chips from the spread spectrum signal, and reduces
11 each thirty-one chip section down to a bit of one or zero, which is
12 passed to the micro controller 34.

13 14 Micro controller

15 The micro controller 34 includes a serial processor, or I/O facility
16 that received the bits from the spread spectrum processing circuit 40.
17 The micro controller 34 performs further error correction. More
18 particularly, a modified hamming code is employed, where each eight
19 bits of data is accompanied by five check bits used by the micro
20 controller 34 for error correction. The micro controller 34 further
21 includes a memory, and after performing the data correction, the micro
22 controller 34 stores bytes of the data bits in memory. These bytes
23 contain a command sent by the interrogator 26. The micro
24 controller 34 responds to the command.

1 For example, the interrogator 26 may send a command requesting
2 that any device 12 in the field respond with the device's identification
3 number. Status information is also returned to the interrogator 26 from
4 the device 12 when the device 12 responds.

6 Unalterable Identification

7 In one embodiment, the integrated circuit 16 includes unalterable
8 indicia (a signature), different from the device's identification number
9 discussed above. The unalterable indicia is burned into programmable
10 read only memory or formed using a laser operating on fusible links.
11 The unalterable indicia is indicative of the history of the particular die
12 used to manufacture the integrated circuit 16. For example, in the
13 illustrated embodiment, the unalterable indicia includes a lot number,
14 wafer number, and die number of the die used to manufacture the
15 integrated circuit 16. This information is transmitted by the transmitter
16 in response to a manufacturer's command received by the receiver. In
17 one embodiment, the manufacturer's command is a controlled access, or
18 secret command that is not readily ascertainable by the public or
19 purchaser/user of the device. This unalterable indicia can be used to

1 trace manufacturing problems in defective devices 12, or to locate stolen
2 products carrying a device 12.

3 4 Arbitration

5 If the interrogator 26 sends out a command requesting that all
6 devices 12 within range identify themselves, and gets a large number of
7 simultaneous replies, the interrogator 26 may not be able to interpret any
8 of these replies. Further, there may be multiple interrogators in an
9 area trying to interrogate the same device 12.

10 Therefore, arbitration schemes are provided. With the more
11 common scenario of multiple devices 12 trying to respond to an
12 interrogator, the interrogator 26 sends a command causing each
13 device 12 of a potentially large number of responding devices 12 to
14 select a random number from a known range and use it as that
15 device's arbitration number. By transmitting requests for identification
16 to various subsets of the full range of arbitration numbers, and checking
17 for an error-free response, the interrogator 26 determines the arbitration
18 number of every responder station capable of communicating at the
19 same time. Therefore, the interrogator 26 is able to conduct
20 subsequent uninterrupted communication with devices 12, one at a time,
21 by addressing only one device 12.

22 If the interrogator 26 has prior knowledge of the identification
23 number of a device 12 which the interrogator 26 is looking for, it can
24

1 specify that a response is requested only from the device 12 with that
2 identification number.

3 Arbitration schemes are discussed below, in greater detail, in
4 connection with protocols.

5 U.S. Patent No. 5,365,551 to Snodgrass et al., which is
6 incorporated by reference, discloses arbitration schemes that could be
7 employed in various alternative embodiments of the invention.

8 9 Reply

10 After the micro controller processes a command from the
11 interrogator 26, the micro controller formats the reply as specified in
12 the protocol and the formatted reply leaves the micro controller via a
13 serial data port of the micro controller. If desired, the formatted reply
14 is spread spectrum encoded by the spread spectrum processing
15 circuit 40. The reply is then modulated by the transmitter 32. The
16 transmitter 32 is capable of transmitting using different modulation
17 schemes, and the modulation scheme is selectable by the interrogator 26.
18 More particularly, if it is desired to change the modulation scheme, the
19 interrogator 26 sends an appropriate command via radio frequency.

20 The transmitted replies have a format similar to the format of
21 incoming messages. More particularly, a reply starts with a preamble
22 (e.g., all zeros in active mode, or alternating double zeros and double
23 ones in backscatter mode), followed by a Barker or start code which
24 is thirteen bits long, followed by actual data.

1 No stop bits are included in the incoming message or reply, in
2 the preferred embodiment. Instead, part of the incoming message
3 describes how many bytes are included, so the integrated circuit 16
4 knows how much information is included. Similarly, part of the
5 outgoing reply describes how many bytes are included, so the
6 interrogator 12 knows how much information is included. The incoming
7 message and outgoing reply preferably also include a check sum or
8 redundancy code so that the integrated circuit 16 or the interrogator 12
9 can confirm receipt of the entire message or reply.

10 After the reply is sent, the integrated circuit 16 returns to the
11 sleep mode, and the wake up timer and logic circuit 36 starts timing
12 again for the next wake up (e.g., in 16 milliseconds, or whatever period
13 is selected).

14 15 Detailed Circuit Schematics

16 Fig. 6 is a graph illustrating how Figs. 6AA-EK are to be
17 assembled.

18 Figs. 6AA-EK include circuitry partitioned in blocks in a manner
19 that is somewhat different from the way the blocks are partitioned in
20 Fig. 5. In some ways Figs. 6AA-EK shows less detail than in Fig. 5,
21 and in some ways they show more detail.

22 The integrated circuit 16 is shown as including an analog
23 processor "anlgproc," an RF processor "rfproc," a PN (pseudo random
24

1 number) processor "pnproc," a data processor "dataproc," and return
2 link configuration logic "rlconfig."

3 The data processor "dataproc" shown in Figs. 6AA-EK is the
4 micro controller or microprocessor 34 of Fig. 5. The data processor
5 "dataproc" is shown in greater detail in Fig. 7. In the illustrated
6 embodiment, the data processor "dataproc" is an eight bit processor, and
7 includes a ROM "rom," a RAM "ram," a serial I/O block "sio," an eight
8 bit ALU (arithmetic logic unit) "alu," an instruction decoder
9 programmable logic array "insdec," and address decoder "adrdec," a clock
10 generator "clk," a conditional qualifier decoder "cqualdec," a databus
11 latch/precharge circuit "dblatch," a timed lockout divider "tld," a data
12 interleaver (which interleaves two thirteen bit words) "dil," a
13 convolutional encoder and preamble generator "conv," a digital port
14 output controller "doutport," a shift register input data multiplexer
15 "shdel" and a series of registers. In the illustrated embodiment, the
16 registers include a timed lockout register "tloreg," a plurality of status
17 registers "sreg," a plurality of read/write control registers "oreg," and an
18 instruction register "insreg."

19 The registers are used to drive control lines to various different
20 circuits to allow the data processor to have control over those circuits.
21 The "sio" block (described below) is the data path for data received
22 and for the data to be transmitted.

23 Fig. 6.01 is a layout diagram illustrating the physical layout of
24 various components on an integrated circuit die, in accordance with one

embodiment of the invention. The physical locations and sizes of components relative to other components are shown. Boundaries between various blocks may be approximate in the sense that portions of certain blocks may extend into other blocks. The layout diagram illustrates that separate analog and digital ground returns are provided. In the illustrated embodiment, the ground return for the receiver and transmitter is spaced apart from the receiver and transmitter. However, in an alternative embodiment, locating the ground return for the receiver and transmitter proximate the receiver and transmitter may provide improved results. In the preferred embodiment, the transmitter and receiver circuitry is physically located on the die close to an edge, proximate to the bond pads. More particularly, the microwave outputs of the transmitter 32 are arranged on the die so as to be next to (in close physical proximity to) the appropriate bond pads. Also shown in Fig. 6.01 are small squares adjacent the receiver and active transmitter pads, respectively. These are ground pads for microwave probing, in the exemplary embodiment. In an alternative embodiment, these microwave probing ground pads can be employed as functional ground pads instead of using the illustrated common analog ground pad.

Fig. 7.01AA-BB provide a circuit drawing of a processor clock generator "clk." The processor clock generator provides clock circuitry that generates all the various clocks that are used by the processor.

Figs. 7.0101AA-BB provide a circuit drawing of a processor clock controller "clkctl." The clock controller "clkctl" determines when the

1 clocks are running. As described elsewhere, the processor is not always
2 on. The clock controller uses enabling signals from wake up so that
3 it knows when to turn on. Thus, some of the inputs to the clock
4 controller are power wake up, receive wake up, timer wake up. The
5 clock controller also synchronizes shut down of the clocks when the
6 processor has completed its task.

7 Figs. 7.0102AE-DJ provide a circuit drawing of a processor phase
8 generator "clkph." The processor phase generator "clkph" generates
9 master clocks - phase one "PH1" and phase two "PH2" - which are
10 non-overlapping clocks.

11 Figs. 7.0103AA-BD provide a circuit drawing of a clock state
12 generator "clkst." The clock state generator "clkst" generates some
13 derivative clocks. Processor instruction cycles are divided. There are
14 cycles and there are states. Within each cycle, which is a certain time
15 period, there are four states - S1 through S4. The states are all non-
16 overlapping, and each state has a high time that is one quarter of the
17 cycle time. As a processor instruction executes, the instruction is taken
18 from the rom "rom," and loaded into the instruction register. The
19 instruction can be, for example, a 1, 2 or 3 cycle instruction, depending
20 on how complex the function is that is performed by that instruction.
21 These are micro instructions for running the processor on chip. They
22 should not be confused with the commands that are sent by radio
23 frequency, which are a much higher level commands. The commands
24 sent by radio frequency require many of these micro instructions for the

processor to carry them out. During clock cycle one, line C1 in Figs. 7.0103AA-BD is high, during clock cycle two, line C2 is high, etc. Within each one of those clock cycles, state one is high for a certain time period and then goes low, and state two goes high for a certain time period then goes low, and so on up through state four. Within each of these states, there is one phase one high time, and one phase two high time.

Figs. 7.02AA-BF provide a circuit drawing of an address decoder "adrdec." In executing instructions, the processor has the need to move bytes of data between registers and ram "ram" and possibly to the serial IO controller "sio." The address decoder "adrdec" generates enable lines to those various different blocks (the registers, ram, and sio, as appropriate) when their address appears on the address bus. The primary input to the address decoder is the address bus. This decoder decides which circuit block is being addressed and issues an enable for either a write or a read, whichever is appropriate, to that particular block.

Figs. 7.03AA-EH provide a circuit drawing of random access memory "ram." The ram has 512 bytes of storage available. 256 of those bytes are available to the user of the device 12, and the other 256 bites are used to do calculations required by the processor. Most of the drawing is taken up by blocks of RAM arrays "ram8x4."

Figs. 7.0301AA-BB provide a circuit drawing of a ram control circuit "ramctl." The ram control circuit issues word line select enable

1 signals, a read command, a write command, and some precharge signals.
2 The ram control circuit generates the signals to control access to and
3 from the random access memory "ram."

4 Figs. 7.0302AA-AC provide a circuit drawing of a RAM array
5 "ram 8x4." Each RAM array is made up of four rows and eight
6 columns of RAM cells.

7 Fig. 7.030201 provides a circuit drawing of a single RAM cell.
8 In the illustrated embodiment, the RAM cell is a six transistor RAM
9 cell. Four transistor RAM cells are employed in alternative
10 embodiments.

11 Figs. 7.0303AA-AD provide a circuit drawing of a RAM precharge
12 circuit "rampch." Figs. 7.0304AA-AD provide a circuit drawing of a
13 RAM precharge circuit "ramdch." In the illustrated embodiment, this
14 circuit has been disabled as is shown in the figure. The RAM
15 precharge circuits provides precharge signals to speed up writing to and
16 reading from RAM cells.

17 Fig. 7.0305 provides a circuit drawing of a RAM address buffer
18 "ramadb." The RAM address buffer isolates the capacitive load
19 presented by the RAM circuits from the address bus.

20 Figs. 7.0306AA-BA provide a circuit drawing of a RAM word line
21 driver "ramwdr." The RAM wordline driver is a predecoder. It takes
22 two address inputs and generates four possible select lines "P0-P3"
23 which are used in a row decoder (discussed below) for the RAM.
24

1 Figs. 7.0307AA-BB provide a circuit drawing of a RAM word line
2 decoder "ramwdec." The RAM word line decoder receives the select
3 lines from the RAM wordline driver in conjunction with four other
4 addresses "AD0-AD3" to select a unique word line. A word line is a
5 row of RAM cells within the RAM.

6 Figs. 7.0308AA-BB provide a circuit drawing of a RAM column
7 select decode circuit "ramcdec." The RAM column select decode circuit
8 uses three address lines "AD5-AD7" to generate eight select lines
9 "CSEL0-CSEL7."

10 Figs. 7.0309AA-BG provide a circuit drawing of a RAM column
11 selector multiplexor "ramcsel." The RAM column selector multiplexor
12 uses the output select lines "CSEL0-CSEL7" from the RAM column
13 select decode circuit "ramcdec" to connect one pair of bit or column
14 lines out of eight pairs "BIT0N/P"- "BIT7N/P" onto a bus. The bus
15 goes to a sense amp or to a write driver, depending on whether a
16 RAM cell is being read or written. There are eight of these RAM
17 column selectors side by side, functioning in the same manner. With
18 any one selection, one of eight pairs are selected on Figs.
19 7.0309AA-BG, but there are seven more similar selections taking place
20 so an entire byte of RAM is selected at one time.

21 Figs. 7.0310AA-BB provide a circuit drawing of a RAM databus
22 interface "ramdb." The RAM databus interface includes a sense amp
23 and write driver for the RAM. The RAM databus interface receives
24

1 the output/input lines "BIT0N/P"-"BIT7N/P" from the RAM column
2 selector "ramcsel." Selected RAM cells can either be sensed or written.

3 Figs. 7.04AA-HJ provide a circuit drawing of a ROM "rom." The
4 ROM has 4096 bytes of contact programmable memory. ROMs of
5 multiple integrated circuits 16 are simultaneously mass programmed. In
6 the third to the last mask step, each particular cell of ROM is
7 programmed with a zero or a one. The ROM does not include the
8 information about the lot number, wafer number and die number
9 discussed elsewhere herein. The ROM is programmed at the time of
10 manufacture, whereas the information about the lot number and wafer
11 number and die location is stored after the manufacture of the wafer
12 using an electrically programmable or laser fuse programmable, or
13 electrical fuse programmable structure.

14 Figs. 7.0401AA-BB provide a circuit drawing of a ROM control
15 logic circuit "romctl." The ROM control logic circuit provides signals
16 to allow the contents of eight memory cells of the ROM, one byte to
17 be read out at a time.

18 Figs. 7.0402AA-AB provide a circuit drawing of a ROM bit line
19 precharge circuit "ROMPCH." The ROM bit line precharge circuit
20 precharges bit lines of the ROM. Bit lines are the vertical lines in the
21 array of ROM cells on which the voltage that is sensed appears after
22 selected ROM cells are accessed.

23 Figs. 7.0403AA-BB provide a circuit drawing of a ROM word line
24 driver "romwdr." The ROM word line driver (or row driver) takes

1 address inputs "A7-A9" and generates enable signals "WDR0-WDR7" to
2 select row lines of the ROM.

3 Figs. 7.0404AA-DC provide a circuit drawing of a ROM word
4 block decoder "romwdec_rev." The ROM word block decoder has as
5 inputs the enable signals "WDR0-WDR7" from the ROM word line
6 driver "romwdr" plus other addresses to generate actual word line
7 signals themselves. A word line signal selects a row of ROM cells.

8 Figs. 7.0405AA-BA provide a circuit drawing of a ROM bit line
9 address driver "rombladr." The ROM bit line address driver buffers
10 some of the addresses so they are capable of driving a large decoder
11 structure "rombldec" (described below).

12 Figs. 7.0406AA-CK provide a circuit drawing of a ROM bit line
13 decoder "rombldec." The ROM bit line decoder provides a decoder
14 structure for selecting a particular ROM bit line out of thirty-two bit
15 lines. There are eight such "rombldec" circuits, allowing simultaneous
16 selection of eight bit lines.

17 Figs. 7.0407AA-AB provide a circuit drawing of a ROM sense
18 amplifier "romsns." The ROM sense amplifier is the sense amp used
19 for determining the state of a particular ROM bit being accessed.
20 Eight ROM bit sense amplifiers are used.

21 Figs. 7.05AA-CB provide a circuit drawing of an instruction
22 register "insreg." The code or program that controls the operation of
23 the processor is stored in the ROM. The instructions stored in the
24 ROM are transferred one at a time to this instruction register "insreg"

1 so that they can be interpreted and the processor can carry out the
2 operations required by that instruction. After the integrated circuit
3 wakes up, its operation is controlled by the wake up and clock recovery
4 circuits. After the integrated circuit locks on to the clock and a valid
5 start (Barker) code is received, the processor turns on and the program
6 stored in the ROM takes over from that point. The program performs
7 functions such as determining if the integrated circuit 16 is in a power
8 up cycle. If the device 12 is in a power up cycle, the processor
9 performs various tasks relevant to power up. If the integrated circuit
10 16 is receiving a command from an interrogator, the program will
11 determine which command and then go through a sequence of required
12 steps in order to respond appropriately to that command. Then the
13 program allows the integrated circuit 16 to go back to sleep.

14 Figs. 7.0501AA-BB provide a circuit drawing of an instruction
15 register "insrcel" included in the instruction register "insreg."

16 Figs. 7.06AA-CN provide a circuit drawing of an instruction
17 decoder PLA "insdec." The instruction decoder PLA interprets what is
18 in the instruction register "insreg" and issues all the enable signals
19 necessary to effect performance of the functions called for in that
20 instruction. Details of the instruction decoder PLA are shown in Figs.
21 7.0601AA-HI; 7.0602AA-JH; 7.0603AA-JI; and 7.0604AA-JI.

22 Figs. 7.0601AA-HI provide a circuit drawing of an instruction
23 decoder (first section) "insdec1."

1 Figs. 7.0602AA-JH provide a circuit drawing of an instruction
2 decoder (second section) "insdec2."

3 Figs. 7.0603AA-JI provide a circuit drawing of an instruction
4 decoder (third section) "insdec3."

5 Figs. 7.0604AA-JI provide a circuit drawing of an instruction
6 decoder (fourth section) "insdec4." Fig. 7.060401 provides a circuit
7 drawing of an instruction decoder ROM amp "insramp" included in the
8 circuit of Figs. 7.0604AA-JI, 7.0601AA-HI, 7.0602AA-JH, and 7.0603AA-
9 JI. Fig. 7.060402 is a circuit drawing of an instruction decoder PLA
10 amp "inspamp" included in the circuit of Figs. 7.0604AA-JI, 7.0601AA-
11 HI, 7.0602AA-JH, and 7.0603AA-JI. Fig. 7.060403 is a circuit drawing
12 of an instruction decoder PLA latch "insplat" included in the circuit of
13 Figs. 7.0604AA-JI, 7.0601AA-HI, 7.0602AA-JH, and 7.0603AA-JI.

14 Figs. 7.07AA-BB provide a circuit drawing of a conditional
15 qualifier decoder "cqualdec." Certain instructions behave differently
16 depending on certain conditions (e.g., whether a carry bit is set), and
17 the conditional qualifier decoder looks for these conditions.

18 Figs. 7.08AA-CA provide a circuit drawing of a databus latch and
19 precharge circuit "dblatch." Data is bused around in eight bit bytes,
20 and the databus latch and precharge circuit drives the databus. The
21 data bus is in a precharge high state when the data bus is not being
22 used. Whichever source of data is selected to put its information on
23 the bus will then drive selected bits low if appropriate.
24

1 Figs. 7.09AA-BF provide a circuit drawing of an arithmetic logic
2 unit "alu." The arithmetic logic unit "alu" is a basic arithmetic logic
3 unit that provides enough flexibility to perform the functions that are
4 needed for the RFID task. Details of the arithmetic logic unit are
5 provided in drawings below.

6 Figs. 7.0901AA-CE provide a circuit drawing of an ALU low byte
7 "alubyt1". There are eight bits within the ALU low byte that are all
8 processed simultaneously.

9 Figs. 7.090101AA-AD provide a circuit drawing of a ALU bit
10 "alubit1" included in the ALU low byte "alubyt1." Figs. 7.090101AA-AD
11 show the registers contained within each bit of the ALU. The registers
12 include an A cell "aluacell" and a B cell "alubcell" which are the
13 primary registers. The data on which arithmetic or logical operations
14 are to be performed reside typically in the A cell "aluacell" or the B
15 cell "alubcell." The registers further include a program counter "alu pc,"
16 a stack pointer "alurcell," a data pointer "alurcell," and a memory
17 address register "alumar" that provides for indirect addressing. The
18 ALU bit "alubit1" further includes an adder "aluadd" and a slave
19 register "aluslave" to the adder.

20 Fig. 7.09010101 is a circuit drawing showing details of construction
21 of an ALU bit decoder cell "alubdec" included in the ALU bit.

22 Fig. 7.09010102 is a circuit drawing showing details of construction
23 of the ALU B register cell "alubcell" included in the ALU bit.
24

1 Fig. 7.09010103 is a circuit drawing showing details of construction
2 of the ALU A register cell "alubacell" included in the ALU bit.

3 Fig. 7.09010104 is a circuit drawing showing details of construction
4 of the ALU program counter "alupc" included in the ALU bit.

5 Fig. 7.09010105 is a circuit drawing showing details of construction
6 of the ALU register cell "alurcell." Such cells are used for a stack
7 pointer, data pointer, etc.

8 Fig. 7.09010106 is a circuit drawing showing details of construction
9 of the ALU memory address register "alumar" included in the ALU bit.

10 Fig. 7.09010107 is a circuit drawing showing details of construction
11 of the ALU slave cell "aluslave" for the ALU adder "aluadd."

12 Fig. 7.09010108 is a circuit drawing showing details of construction
13 of the ALU adder "aluadd" included in the ALU bit.

14 Figs. 7.0902AA-BD provide a circuit drawing for an ALU high
15 byte "alubyth" which functions similarly to the ALU low byte "alubyt1."
16 Two ALU bytes are provided so that sixteen bit commands can be
17 processed.

18 Figs. 7.090201AA-AC provide a circuit drawing of a bit "alubith"
19 included in the ALU high byte "alubyth."

20 21 Details of Low Power Dormant Mode

22 It is sometimes desirable to prevent the integrated circuit 16 from
23 responding to commands from an interrogator. For example, after
24 communication with a particular device 12, it is sometimes desirable to

1 prevent that particular device 12 from responding to a subsequent
2 interrogation that is intended for a different device 12. If, for example,
3 the device 12 is used in connection with an access gate, after an
4 interrogator has read a badge containing the device 12 as a controlled
5 access point is passed, the interrogator no longer has a need to
6 communicate with that badge. The interrogator instead would want to
7 pick up subsequent badges passing through the access gate. In addition,
8 when the interrogator no longer has a need to communicate with a
9 particular device 12, it is desirable that the device 12 stay in the sleep
10 mode to conserve battery power.

11 In one embodiment, the device 12 is put into an unresponsive
12 state by using a counter which is set to a desired time via a radio
13 frequency command. The device will then not respond to Identify
14 commands (described below in greater detail) used by an interrogator
15 to request information from a device 12. In this embodiment, the
16 unresponsive state can be cancelled by a radio frequency command.
17 However, this embodiment is disadvantageous in that the device must
18 wake up to process incoming commands and abort if the command is
19 an Identify command. This consumes battery capacity.

20 In a preferred embodiment, the device 12 can be placed in a
21 dormant mode via a radio frequency command. The dormant mode
22 cannot be cancelled. When in the dormant mode, the device 12 does
23 not wake up to look for incoming commands.
24

1 Figs. 7.10AA-CC provide a circuit drawing of a timed lock out
2 divider "tld." The timed lock out divider takes as an input the low
3 power clock which is the same clock that sets the wake up interval for
4 the integrated circuit 16. The timed lock out divider provides two
5 functions. The timed lockout divider provides an alarm timer function,
6 and provides a timed lockout function which is used for the dormant
7 mode function and for the timed lockout of Identify commands.

8 The alarm timer is set to go off in intervals, such as about every
9 one minute. As an alarm timer, the timed lock out divider causes the
10 integrated circuit 16 to wake up and check for threshold violations in
11 alarm mode. Such threshold violations would be triggered by analog
12 sensors such as temperature sensors, magnetic sensors, etc.

13 The timed lock out divider also allows, by RF command from an
14 interrogator, a user to disable a device 12 to make it not respond for
15 a prescribed period of time (i.e., allows the user to place the device
16 12 in the dormant mode). The prescribed period of time can be set
17 in various increments. For example, in the illustrated embodiment, the
18 increments are one second increments from one up to 255 seconds.

19 When in the dormant mode, the device 12 does not periodically
20 switch to the receiver on mode to check for the presence of radio
21 frequency commands. Therefore, power is conserved.

22 This dormant mode function is useful for the same reasons that
23 the cancellable timed disabling is useful. If, for example, the device
24 12 is used in connection with an access gate, after an interrogator has

1 read a badge containing the device 12 as a controlled access point is
2 passed, the interrogator no longer has a need to communicate with that
3 badge. The interrogator instead would want to pick up subsequent
4 badges. Therefore, the interrogator can instruct the device 12 to not
5 respond for a certain time, so as to prevent an unwanted response of
6 a device 12, after having communicated with that device 12, but with
7 increased power savings over the cancellable timed disabling. Because
8 wake ups are disabled, current consumed by the device 12 is very low;
9 e.g., 1 μ A.

10 Fig. 7.1001 provides a circuit drawing showing details of
11 construction of a timed lock out divider cell "tldcel" included in the
12 timed lockout divider "tld."

13 Figs. 7.11AA-AB provide a circuit drawing of a timed lock out
14 register "tloregr." This register acts as a down counter and is selectively
15 set with the desired lockout time, from 1 to 255 seconds.

16 Figs. 7.1101AA-AC provide a circuit drawing of a timed lock out
17 register cell "tlorcel" included in the timed lockout register.

18 Figs. 7.12AA-AC provide a circuit drawing of an read/write control
19 register or output register "oreg." There are a number of these output
20 registers. The output registers allow the processor to send control
21 signals out to various peripheral circuits to cause them to function when
22 required.

23 Fig. 7.1201 provides construction details of a control register cell
24 "regcell" included in the output register "oreg."

1 Figs. 7.13AA-BA provide a circuit drawing of a status register
2 "sreg." The processor uses the status register to monitor the status of
3 lines supplied from various blocks of circuitry.

4 Figs. 7.1301AA-AB provide a circuit drawing of a status register
5 cell "sregcel" included in the status register.

6 Figs. 7.14AA-AB provide a circuit drawing of a serial input output
7 block "sio." The serial input output circuitry is the data path for data
8 received and for the data to be transmitted. This circuit controls the
9 transfer of the serial stream of data received from the receiver into the
10 processor. The circuit also controls the transfer of the transmit serial
11 data stream from the processor out to the transmitter. The serial input
12 output circuitry comprises two blocks: a block "siodata" that processes
13 data, and a controller "sioctl" that runs the block that processes data.

14 Figs. 7.1401AA-AB provide a circuit drawing of a serial input
15 output data path "siodata." When the integrated circuit 16 is in a
16 transmit mode, data enters the bit registers "sioreg" from the top of
17 the figure, and the data is transferred down to the registers "siobdlat"
18 and "siobdlat_inv" which are the row of blocks second up from the
19 bottom of the figure. The intermediate stages "sioxor" are all exclusive
20 or gates that are used to generate check bits according to the
21 previously mentioned modified Hamming code. The extra five bits "P0-
22 P4" appended to the eight data bits "D0-D7" are generated by the
23 exclusive-or gates, and then all thirteen bits are transferred to the
24 registers "sioshr" which are the row of blocks at the bottom of the

1 figure. The thirteen bits are serially shifted out to the right of the
2 figure.

3 When the integrated circuit 16 is in a receive mode, a reverse
4 sequence takes place. Data is shifted into the thirteen bit registers
5 "sioshr" shown on the bottom of the figure, then transferred up to the
6 registers "siodblat" immediately above the shift registers "sioshr" in the
7 figure. Then the exclusive or circuitry "sioxor" uses the data and the
8 check bits to determine whether there are any errors. If there are any
9 correctable errors, they are corrected at that point. The serial input
10 output data path "siodata" can also detect double bit errors which are
11 not correctable. If a double bit error is detected, a signal is provided
12 at the upper left of the figure to the processor that an uncorrectable
13 error has occurred. Assuming that there is no uncorrectable error, the
14 eight corrected bits are now present as inputs to the top row of
15 registers "sioreg." The eight corrected bits are then transferred in to
16 the top row of registers. From the top row of registers "sioreg," the
17 corrected bits are transferred in parallel to the processor.

18 Figs. 7.140101AA-AB provide construction details of the serial
19 input output register cell "sioreg" included in the serial input output
20 data path "siodata."

21 Figs. 7.140102AA-GF provide construction details of the serial
22 input output exclusive or circuit "sioxor" included in the serial input
23 output data path "siodata."

1 Figs. 7.140103AA-AB provide construction details of the
2 bidirectional latch "siobdlat_inv" included in the serial input output data
3 path "siodata."

4 Figs. 7.140104AA-BB provide construction details of the shift
5 register "sioshr" included in the serial input output data path "siodata."

6 Figs. 7.140105AA-AB provide construction details of the
7 bidirectional latch "siobdlat" included in the serial input output data
8 path "siodata."

9 Figs. 7.1402BA-EI provide a circuit drawing of the previously
10 mentioned control logic "sioctl." The control logic "sioctl" generates all
11 the clocking and the signals that control when data is transferred from
12 register to register.

13 Figs. 7.140201AA-BB provide a circuit drawing showing construction
14 details of the counter bit "siocbit" included in the control logic "sioctl."

15 Figs. 7.15AA-EC provide a circuit drawing of a data interleaver
16 "dil." In a number of modulation schemes used or selectively used by
17 the integrated circuit 16, differential encoding is employed. Use of
18 differential encoding in the integrated circuit 16 makes possible a
19 simpler receiver in the interrogator. However, if an error occurs in the
20 process of differential encoding, it necessarily corrupts two adjacent bits.
21 The modified Hamming code cannot correct errors where two adjacent
22 bits are in error. This problem is solved by interleaving two bytes.
23 Bit by bit, the first bit of one byte is shuffled next to the first bit of
24 another byte and so on through all thirteen bits. This way, when

1 differential encoding is performed, which may possibly create two
2 adjacent errors, the two bytes are deinterleaved and separated at the
3 receiver so that the bytes are in separate error corrective words. The
4 errors can then be fixed.

5 The data interleaver works by shifting data in from a data input
6 "SIOTXD" (on the upper left of Figs. 7.15AA-EC). Twenty-six bits are
7 shifted into the registers "dil_sreg" shown along the top of Figs.
8 7.15AA-EC, then all twenty-six bits are simultaneously shifted to the
9 lower registers "dil_plsreg" and scrambled in order simultaneously by
10 wiring interconnections between the registers "dil_sreg" and the registers
11 "dil_plsreg" shown in Figs. 7.15AA-CC. Thus, a new interleave order
12 is generated on transfer from the registers "dil_sreg" to the registers
13 "dil_plsreg." Then, the contents of the registers "dil_plsreg" are shifted
14 out (to the right in the view of Figs. 7.15AA-EC) in a serial, bit by
15 bit fashion, through line "DILTXD."

16 Figs. 7.1501AA-CA provide a circuit drawing showing construction
17 details of the shift register "dil_sreg" included in the data interleaver
18 "dil."

19 Figs. 7.1502AA-CA provide a circuit drawing showing construction
20 details of the parallel load shift register "dil_plsreg" included in the
21 data interleaver "dil."

22 Fig. 7.150201 provides a circuit drawing showing construction
23 details of a shift register bit "dil_sregbit" included in the parallel load
24 shift register "dil_sregbit" and in the shift register "dil_sreg."

1 Figs. 7.16AA-CD provide a circuit drawing of a convolutional
2 encoder "conv." In the illustrated embodiment, convolutional encoding
3 is disabled. However, in one embodiment, convolution encoding is
4 provided. The circuitry of Figs. 7.16AA-CD performs more functions
5 than just convolutional encoding. The circuitry of Figs. 7.16AA-CD also
6 includes a preamble generator. In one embodiment, a series of zeros
7 are generated as a preamble. However, in the illustrated embodiment,
8 a pattern of alternating zeros and ones (0101) is generated for DPSK
9 backscatter. The circuitry of Figs. 7.16AA-CD also includes a clock for
10 the SIO "sio."

11 Fig. 7.1601 provides a circuit drawing showing construction details
12 of a shift register cell "convshr" included in the convolutional encoder
13 "conv."

14 Fig. 7.1602 provides a circuit drawing showing construction details
15 of a summer "convsum" included in the convolutional encoder "conv."

16 Figs. 7.17AA-BB provide a circuit drawing of a shift register data
17 multiplexor "shdcel." The shift register data multiplexor provides a port
18 into the processor. It does a selection among eight sources on the
19 integrated circuit 16, and connects only one of them for shifting of data
20 for transfer into the A register.

21 Figs. 7.18AA-CC provide a circuit drawing of a digital port output
22 controller "doutport." The device selectively reads data via a digital
23 port in response to a radio frequency command, instead of by radio
24 frequency reception, and the device selectively writes data via a digital

1 port in response to a radio frequency command, instead of by radio
2 frequency. The digital port output controller circuit controls these
3 functions. The digital port output controller circuit also includes a
4 clock in order to synchronize the transfer of the data in either direction
5 (input or output).

6 The RF processor "rfproc" shown in Figs. 6AA-EK contains the
7 receiver 30, the transmitter 32, the clock recovery and data recovery
8 circuit 38, and the wake up timer and logic circuit 36. The RF
9 processor "rfproc" is shown in greater detail in Figs. 8AA-CB.

10 Figs. 8AA-CB provide a circuit drawing of a RF processor
11 "rfproc." The RF processor "rfproc" includes a receiver "rx" (which is
12 the receiver 30 of Figs. 6AA-EK), a transmitter "tx" (which is the
13 transmitter 32 of Figs. 6AA-EK), a low power frequency locked loop
14 "lpfl," a counter bit "lpfl_cbit," a receiver wake up controller "rxwu"
15 (which is the wake up timer and logic circuit 36 of Figs. 6AA-EK), and
16 a digital clock and data recovery circuit "dcr" (which is the clock and
17 data recovery circuit 38 of Figs. 6AA-EK). Thus, RF processor "rfproc"
18 includes the clock that sets the wake up interval, as well as logic that
19 performs tests on the incoming signal to see whether the incoming
20 signal is a valid signal such that the integrated circuit 16 should stay
21 awake.

22 Figs. 8.01AA-DE provide a circuit drawing of the receiver "rx"
23 included in the RF processor. In the illustrated embodiment, the
24 receiver "rx" includes a Schottky diode detector "diodedet." In the

1 illustrated embodiment, the Schottky diode detector "diodet" is an
2 inductorless Schottky diode detector. Instead of employing inductors
3 in the diode detector to supply bias current to the diode, the diode
4 detector includes a current source which drives current through both an
5 antenna and a Schottky diode included in the detector. The
6 inductorless Schottky diode detector is described in more detail below.
7 Figs. 8.01AA-DE also illustrate a CMOS detector "cmosdet" that is used
8 in accordance with an alternative embodiment, but which is not used in
9 the illustrated embodiment. The output of the Schottky diode detector
10 is applied through a series of AC coupled amplifiers. More particularly,
11 in the illustrated embodiment, the Schottky diode detector is applied
12 through amplifiers "videoamp1," "videoamp2" replicated four times, and
13 then into a comparator. The function of the comparator is to put out
14 a full digital signal. The output of the comparator is a base band
15 digital representation of the command that was sent by the interrogator.

16 A base band signal is a signal without a carrier frequency present.
17 The output of the comparator is a signal that is the equivalent of the
18 signal that was used to modulate the carrier back at the interrogator.

19 The receiver "rx" includes a RF detect circuit "rxdetect." The
20 RF detect circuit determines when a modulated radio frequency signal
21 is present at the receiver and the output of the receiver is switching
22 between high and low states. The receiver "rx" includes a bias block
23 "rxbias" that provides currents to the various amplifiers "videoamp1,"
24 "videoamp2," etc. The receiver "rx" further includes logic that bypasses

1 the receiver when a user selects not to use RF for an input, but rather
2 to provide a base band input signal directly in digital form. The user
3 may make the selection to bypass the receiver, for example, for testing
4 or exercising the integrated circuit 16. The user may also make the
5 selection in applications where the receiver portion of the chip is not
6 required, but the integrated circuit 16 is used to transmit information
7 (e.g., for periodic transmissions).

8 9 Schottky Diode RFID Detector

10 Overview

11 For purposes of realizing a cost effective and low power radio
12 frequency receiver on an RFID tag, a simple Schottky diode receiver
13 is utilized. The receiver is formed from a Schottky diode detector, an
14 amplifier, and the receiving antenna "rxantenna". With the
15 implementation of a single integrated circuit 16 RFID tag, an easy and
16 low cost technique for configuring the frequency of operation on a tag
17 is needed. Receiver frequency characteristics can be tailored by
18 selecting an appropriately sized antenna to be coupled to the integrated
19 circuit 16 that supports the Schottky diode detector. Furthermore,
20 adjustment of bias current across the Schottky diode can be used to
21 realize a desired resistance there across, enabling tuning or detuning of
22 the receiver.

1 For purposes of enabling simplified representation, Fig. 29
2 illustrates a simplified circuit schematic for one embodiment of a
3 receiver 80 having a Schottky diode detector 84 and antenna 44.

4 The detector 84 includes a Schottky diode 86 having an anode
5 connected to the antenna 44 and having a cathode.

6 The exemplary antenna 44 is formed from a loop or folded dipole
7 construction. The antenna 44 performs band pass filtering.

8 The detector 84 further includes an ideal current source 88
9 connected to the cathode of the Schottky diode 86 and driving current
10 through the antenna and Schottky diode 86 in the direction from the
11 anode to the cathode. The current source 88 is an ideal current source,
12 and is configured to forward bias the Schottky diode 86, realizing a
13 desired resistance (or impedance) in the process.

14 The detector 84 further includes a capacitor 90 connected between
15 the cathode of the Schottky diode 86 and ground. The capacitor 90
16 provides a radio frequency short to ground so that all radio frequency
17 voltage appears across the Schottky diode 86. This maximizes a base
18 band signal produced by the Schottky diode 86.

19 The detector 84 further includes a capacitor 92 having a first
20 terminal connected to the cathode and having a second terminal defining
21 an output of the detector 84. The capacitor 92 provides an AC short
22 to video frequency, and defines the output of the detector 84. The
23 capacitor 92 allows different bias levels in the detector and at the input
24 of a video amplifier connected to the output of the detector 84.

1 Details of the actual circuit implementation on integrated circuit 16 (of
2 Fig. 5) will be discussed below with reference to Figs. 5, 8AA-CB,
3 8.01AA-DE, 8.0101AA-CB, 28, 29, and 30.

4 5 Antenna Implementation

6 Preferably, the antenna "rxantenna" is constructed and arranged to
7 form a folded dipole antenna, consisting of a continuous conductive
8 path, or loop of microstrip. The terminal ends of the antenna 44 loop
9 each form a conductive lead that electrically interconnects with the
10 integrated circuit 16 of Fig. 5. According to the actual circuit layout
11 of Fig. 6, antenna "rxantenna" is connected to the integrated circuit 16
12 via the exposed conductive bonding pad labeled "rxantenna - Pad D".
13 Alternatively, the antenna can be constructed as a continuous loop
14 antenna. In this case, the antenna is constructed from a continuous
15 piece of conductive microstrip configured in the shape of a square or
16 circle to form a loop antenna.

17 In assembly, antenna 44 (as well as antenna 46) is depicted in
18 electrically conductive and bonded relationship with "rxantenna - Pad D,"
19 shown on the integrated circuit 16 of Fig. 6. Similarly, antenna 46 is
20 bonded to "txantenna - Pad AA". The preferred assembly technique,
21 discussed below, involves a flip-chip epoxy bonding technique wherein
22 the antennas 44 and 46 of Fig. 5 are actually printed onto the back
23 face of the plastic card or carrier (e.g. card 11 of Fig. 2 and stamp 20
24

1 of Fig. 3), after which the integrated circuit 16 is bonded to the
2 antenna, as well as to the battery, using a conductive epoxy.

3 Preferably, the antennas 44 and 46 are printed onto the back side
4 of the card or stamp, forming each microstrip loop antenna thereon.
5 For example, the antenna can be silk screened onto the card with a
6 conductive polymer thick film. Alternatively, a conductive silver filled
7 epoxy can be used. Alternatively, the antenna can be formed from a
8 separate piece of conductive material, for example, from a piece of wire
9 or conductive ribbon that is glued to the back of the card.

10 One exemplary technique for assembling the postage stamp 20 of
11 Fig. 4 is provided here below. The same technique can be used to
12 assemble the badge 10 of Fig. 2, or any other similarly constructed tag
13 having a rigid support or substrate similar to plastic cards 11 and 21.
14 First, antennas 44 and 46 (of Fig. 5) are mounted to a back face of
15 the card. Preferably, the above elements are simultaneously printed
16 onto the back of a large sheet of plastic with a conductive silver
17 printed thick film, after which the cards are individually separated, or
18 cut from the sheet. Pads on the integrated circuit 16 form enlarged
19 connection points for electrically bonding each antenna 44 and 46 to
20 "rxantenna - Pad D" and "txantenna - Pad AA" of Fig. 6 and for
21 connections to a power supply. Next, the card is positioned front face
22 down onto a rigid support plate. Then integrated circuit 16 (of Fig.
23 4) is mounted to the pads with conductive beads of epoxy. Finally, the
24 battery 18 is bonded along its bottom face with a bead of conductive

1 epoxy, after which conductive epoxy is used to electrically connect the
2 opposite terminal or top of the battery with a corresponding conductive
3 die pad.

4 Subsequently, a metal dam sized to conform generally to the outer
5 peripheral shape of the card 20 is placed over the back of the card.
6 The dam functions as an outer template while a thin layer of non-
7 conductive epoxy (not shown) is applied to the back of the card 20,
8 preferably hermetically sealing in the integrated circuit 16, antenna and
9 battery. Preferably, the thin coat of epoxy consists of a coating, barely
10 thick enough to cover over the components forming the device. One
11 benefit provided by this construction technique is the elimination of any
12 visible bumps in the tag which can result when constructing the tag by
13 heat sealing two or more pieces of plastic card together to trap the
14 device 12 therein. However, a lesser preferred construction of this
15 invention envisions forming the tag, e.g. badge 10, stamp 20, or some
16 other tag, with such a heat sealed sandwich of plastic cards.

17 Preferably, the above technique for mounting integrated circuit 16
18 to card 20 (of Fig. 4) consists of a flip-chip mounting technique. One
19 example of a flip-chip mounting technique is disclosed in pending U.S.
20 Patent Application Serial No. 08/166,747, "Process of Manufacturing an
21 Electrical Bonding Interconnect Having a Metal Bond Pad Portion and
22 Having a Conductive Epoxy Portion Comprising an Oxide Reducing
23 Agent," listing Rick Lake and Mark E. Tuttle as inventors, and
24 incorporated herein by reference.

Integrated Circuit Implementation

According to Fig. 8, the Schottky diode detector "diodet" is configured within receiver "rx" to receive radio frequency signals via receiving antenna "rxantenna". One exemplary receiving antenna configuration is depicted in Figure 5, denoted generally by reference numeral 44. In operation, the Schottky diode detector and the receiving antenna cooperate to form a tunable receiving circuit. Signals detected by the Schottky diode detector are input to a five stage amplifier, then a comparator, for further signal conditioning. The output of the comparator is a digital representation of the received baseband signal.

As shown in Fig. 8, receiver "rx" is an Amplitude Shift Keying (ASK) receiver. This is also known as an AM receiver. The illustrated embodiment employs On Off keying (OOK) wherein a digital one ("1") is represented by the presence of the RF carrier, and wherein a digital zero ("0") is represented by the absence of the carrier.

Figs. 8.01AA-DE illustrate in greater detail the circuit implementation of receiver "rx". According to this embodiment, Schottky diode detector "diodedet" receives input signals via an input "rxantenna," and bias voltages for the current source via a pair of inputs "bias1" and "bias2". A pair of output signals "OUTN" and "OUTP" leave "diodedet" for input to a serially connected chain of amplifiers, and a comparator. The array of amplifiers comprise five video amplifiers, labeled "videoamp1" and "videoamp2". Bias voltages are applied to

1 "bias1" and "bias2" via "rxbias," a bias circuit which generates all bias
2 voltages required by the receiver.

3 A circuit "rxdet" shown in Figs. 8.01AA-DE receives the output
4 signal from the comparator, via combinational logic, with "digrxdata" and
5 "digrx". The output signal "RFDET" is driven high if there is a signal
6 at the output of the comparator. The resulting signal input into "rxdet"
7 is received via "dataIn." Additional inputs to "rxdet" include "lowrate,"
8 "Vref," "Vbias1," "Vbias2," "Vreg," and "enable." Further details of
9 "rxdet" are disclosed below with reference to Figs. 8.0106AA-CD, entitled
10 "RF Detect".

11 Figs. 8.0101AA-CB illustrate one embodiment for realizing the
12 Schottky diode detector "diodedet" of Figs. 8.01AA-DE. Namely, a
13 Schottky diode is forward biased from receiving antenna, coupled at
14 "ANT," to a detector output "OUTP." A second Schottky diode is
15 forward biased from Vdd to a detector output "OUTN." Two current
16 sources are formed by four transistors, and are driven by bias voltages
17 at "bias1" and "bias2." A capacitor is coupled to Vss, between each
18 Schottky diode and associated output, "OUTP" and "OUTN," respectively.
19 Furthermore, an array of parallel capacitors are provided in series
20 between each Schottky diode and associated output, "OUTP" and
21 "OUTN," respectively. The array of parallel capacitors acts as a single
22 capacitor. Each Schottky diode is formed from an array of Schottky
23 diodes. In order to use standard contact hole sizes, each Schottky
24

1 diode is formed from an array of Schottky diodes connected together
2 in parallel to act as a single Schottky diode.

3 According to Figs. 8.01AA-DE, "OUTP" and "OUTN" are input
4 into a multiple (e.g., five) stage amplifier and into a comparator. In
5 order to avoid amplification of substrate noise, a differential amplifier
6 is employed for each stage of the multiple stage amplifier. Noise
7 appears equally on both inputs of each differential amplifier, and, the
8 common mode rejection of the differential amplifiers impedes
9 transmission of substrate noise. The differential amplifiers amplify a
10 received baseband signal up to a digital level. A dummy Schottky
11 diode (the lower Schottky diode in the figures) is connected to the
12 second input of the first differential amplifier.

13 14 Details of Realization of Wide Carrier Frequency Bandwidth

15 In order to meet the wide range of intended applications, it is
16 desirable to construct the integrated circuit for an RFID tag to realize
17 operation of a wide range of carrier frequencies. For example, several
18 desirable carrier frequencies for the device disclosed in Figs. 5 and 6
19 are 915, 2450, and 5800 MegaHertz bands. Frequency selectivity is
20 realized in the device of Figs. 5 and 6 by appropriately configuring
21 external antennas and internal circuit components of the integrated
22 circuit. For the case of a single integrated circuit with an active on-
23 board transmitter, it is necessary to design circuit components into the
24 integrated circuitry prior to mounting and encapsulation of the integrated

1 circuit with an antenna inside of a package. Hence, the circuit
2 components needed to facilitate tailoring of the carrier frequency must
3 be "designed in" the integrated circuit. In the case of a backscatter
4 transmitter, components included in the integrated circuit can be selected
5 so as to allow operation over a wide range of carrier frequencies, the
6 selection being made by choice of antenna.

7 According to Figs. 8.01AA-DE, the number of amplifiers that need
8 to be implemented via "videoamp1" and "videoamp2" is determined based
9 upon the magnitude of the minimum detected signal and the required
10 signal to noise (S/N) ratio. Amplification is sufficient to produce full
11 digital levels at the output of the comparator.

12 The capacitor configured to ground in the video receiver circuit
13 of Fig. 29 (and Figs. 8.0101AA-CB) is used to separate the radio
14 frequency (RF) from the "VIDEO AMP" side of the video receiver
15 circuit. The capacitor is sized to impart an effective short circuit to
16 ground at radio frequency, thereby ensuring that all of the radio
17 frequency (RF) voltage appears across the Schottky diode terminals.
18 Additionally, the capacitor should be sized small enough at video
19 frequencies, so that the capacitor does not load down the video amp
20 circuit.

21 The capacitor configured in series in the video receiver circuit of
22 Fig. 29 (and Figs. 8.0101AA-CB) is used to block out the DC
23 component of a voltage to "VIDEO AMP" while retaining the AC
24

1 component. In this manner, the series capacitor forms a "blocking"
2 capacitor or "coupling" capacitor.

3 4 Details of Inductorless RF Detector

5 A second desirable feature for the integrated circuit of an RFID
6 tag is to eliminate the need to use inductors when constructing the
7 Schottky diode detector. One technique for providing a bias current to
8 a Schottky diode is disclosed in Fig. 28. Fig. 28 illustrates a
9 receiver 60 including an antenna 62 and a Schottky diode detector 64.
10 The receiver 60 includes inductors 68 and 70 used to provide the bias
11 current via voltage source 74 with this implementation. A capacitor 76
12 is shunted to ground, and a second capacitor 78 is placed in series,
13 providing AC coupling to the video amplifier. Several variations of
14 such inductor-based bias current implementations are described in a
15 paper entitled "Designing Detectors for RF/ID Tags," by Raymond W.
16 Waugh of Hewlett-Packard Company, submitted for presentation at the
17 RF Expo, San Diego, February 1, 1995, and which is already
18 incorporated by reference. Inductors are required in all of these
19 constructions, but their implementation on an integrated circuit proves
20 difficult because of problems inherent in forming inductors in an
21 integrated circuit. The circuit in Fig. 29 eliminates the inductors by
22 biasing the Schottky diode with a high impedance current source. A
23 current sink is provided by connecting the far end of the antenna to
24 Vdd.

Details of Elimination of Overdrive Problem

The Schottky diode detector circuit implementation of Figs. 8.0101AA-CB realizes a technique for negating the effect of high power radio frequency (RF) input levels on the Schottky diode detector. More particularly, when high level radio frequency (RF) power is present at the antenna "rxantenna," e.g. when the RFID tag antenna is close to the transmitting antenna of an interrogator, the signal present on node "A" of Fig. 29 becomes large. For example, the signal on node "A" could be several hundreds of millivolts. The rising and falling edges of the detected signal are controlled by two separate time constants which are very different, as shown in Fig. 31. As shown by the high power signal of Fig. 31, the high power signal has a rising edge which is fast, or has a very steep, nearly vertical slope. The nearly vertical slope of the rising edge results because the rising edge is controlled by the effective resistance of the Schottky diode (about 1 kOhm) multiplied by the capacitance of capacitor 90 (Crf) (about 1-10pF). Hence, the resulting time constant is about 1 to 10 nanoseconds.

In contrast, the falling edge of the detected signal in Fig. 31 is controlled by the current source 88 as it discharges capacitor 90 (Crf), which takes approximately 100 nanoseconds. As a result, the voltage waveform at node "A" is distorted. According to the amplified digital version of the signal, shown in Fig. 31, the signal in the high power case is distorted by the unequal rise and fall times. The onset of each fall for the digital version is triggered at the cross-over point, which

1 deviates substantially from that of the low power signal. Such a
2 distortion poses a serious problem for implementing clock recovery
3 schemes, which rely on accurate edge-to-edge timing.

4 To overcome the above-mentioned problem, the integrated
5 circuit 16 of Fig. 6 uses only rising edges for clock recovery. Hence,
6 the distorted falling edges are avoided altogether. As becomes apparent
7 from viewing the amplified digital signal of Fig. 31, rising edge to rising
8 edge timing is not affected by the slow falling edges. Therefore, the
9 clock can be accurately recovered.

10 Fig. 30 illustrates a circuit 93 including a Schottky diode
11 detector 94, and an antenna 44 connected to the Schottky diode
12 detector 94. More particularly, in the illustrated embodiment, the
13 Schottky diode detector 94 includes a Schottky diode 96 having a
14 cathode connected to the antenna 44 and an anode. The Schottky
15 diode detector 94 further includes a current source 98 driving current
16 in the direction from the anode to the cathode of the Schottky
17 diode 96 and through the antenna 44. The Schottky diode detector 94
18 further includes a capacitor 100 connected between the anode of the
19 Schottky diode 96 and ground; and a capacitor 102 connected between
20 the anode of the Schottky diode 96 and an output of the diode
21 detector 94 which is connected to an amplification circuit. The same
22 technique used with respect to Fig. 29 can also be implemented for the
23 Schottky diode detector circuit of Fig. 30. However, for this case, only
24 the rising edges are significantly distorted, since the Schottky diode is

1 reversed in direction. Therefore, only the falling edges are used in
2 clock recovery.

3 4 Details of Method of Forming an IC Schottky Structure

5 A method of forming a Schottky structure that can be employed
6 to manufacture the Schottky diode detector will now be described. A
7 Schottky diode is a diode in which a metal and a semiconductor form
8 a pn junction. Electrons injected into the metal have a higher energy
9 level than the charge carriers in a semiconductor, and energy storage
10 at the junction is low because current flow is not accompanied by hole
11 movement.

12 One embodiment of the invention comprises a Schottky diode 220
13 including an n+ region 222 generally encircling or surrounding an n-well
14 region 224 (Fig. 41). In the illustrated embodiment, the n+ region 222
15 is heavily doped; e.g., 1×10^{18} atoms/cm³ or greater of n-type material,
16 and the n-well region 224 is lightly doped; e.g., 1×10^{17} atoms/cm³ or
17 lower of n-type material. The n-well region 224 defines a contact area
18 226, and the n+ region 222 provides a low resistance interconnect to
19 the Schottky diode 220. The n+ region 222 has a diffused edge 228,
20 and the n-well region has a contact edge 230. The distance from the
21 n+ region diffused edge 228 to the n-well region contact edge 230 is
22 minimized. In one embodiment, the distance from the n+ region
23 diffused edge 228 to the n-well region contact edge 230 is less than
24 twenty micrometers. In a more preferred embodiment, the distance

1 from the n+ region diffused edge 228 to the n-well region contact
2 edge 230 is about two micrometers.

3 More particularly, the integrated circuit 16 includes a grid pattern
4 of n+ regions 222. Each region 222 generally encircles or surrounds
5 isolated n-well regions 224 of a large common n-well region 232 under
6 the n+ regions 222 (Figs. 41 and 42). This provides for parallel
7 connection of a selectable number of Schottky diodes 220. As described
8 elsewhere, the parallel connection of Schottky diodes 220 acts a single
9 Schottky diode, and allows use of standard sized contact holes. The
10 number of Schottky diodes 220 connected together is selectable to tailor
11 resistance, parasitic capacitance, and electrostatic discharge sensitivity for
12 a specific application.

13 To form the grid of Schottky diodes 220, the following process
14 steps are performed.

15 First, a p- substrate 234 is provided (Fig. 38). Next, n-well
16 region 232 is defined relative the substrate 234. Next, an insulator 236
17 is formed over the n-well region. In one embodiment, the insulator 236
18 is borophosphosilicate glass (BPSG).

19 Next, a removal or etching step is performed to remove areas of
20 the insulator 236 for definition of contact holes 238, and areas 240
21 generally encircling or surrounding the contact holes 238 (Fig. 39). The
22 contact holes 238 are not necessarily circular in cross-section; any cross-
23 sectional shape is possible. Similarly, any cross-sectional shape is
24 possible for the areas 240 surrounding the contact holes 238. In a

1 preferred embodiment, the contact holes 238 all have the same diameter
2 (or peripheral extent) to facilitate subsequent filling of the contact
3 holes 238 (described below in greater detail). In an alternative
4 embodiment, different contact holes 238 have different sizes. In the
5 process of the illustrated embodiment, the contact holes 238 do not
6 need to be completely filled with a conductor, and all contact holes
7 therefore do not need to be the same size.

8 In the illustrated embodiment, the n+ regions 222 are formed in
9 the n-well region 232 by diffusion after the etching has been performed,
10 via the openings 240 surrounding the contact holes 238. The n+
11 regions 222 can be formed by other processes or in other sequences.
12 For example, the n+ regions 222 can be formed before the
13 insulator 236 is formed over the n-well region 232.

14 Next, a Schottky forming metal 242 such as titanium is formed in
15 the contact hole openings. In the illustrated embodiment, the Schottky
16 forming metal is deposited on the surface of n-well regions 224 via the
17 contact hole openings 238. In one embodiment, the thickness of the
18 deposited metal is about 200 Å. The metal is annealed to form a
19 stable silicide interface to the n-well silicon.

20 If it is desired to fill the contact holes, a material such as
21 tungsten 246 may be deposited into the contact holes (Fig. 40). The
22 tungsten is then planarized to form final contact structures (Fig. 41).

23 Then, an interconnect metallization step is performed (Fig. 42).
24 For example, copper doped aluminum 248 is deposited (e.g. sputtered)

1 over the wafer, then the wafer is masked and etched to remove
2 unwanted areas. The mask defines a pattern to interconnect the
3 contacts as desired.

4 A variable number of Schottky diodes may be connected in
5 parallel by simply changing the metal masks and interconnecting only
6 the number of Schottky diodes required by a particular circuit
7 application. In one illustrated embodiment, an array of twelve by
8 twelve Schottky diodes (144 total Schottky diodes) is provided (Fig. 43).
9 In another embodiment (Fig. 42), less than all available Schottky diodes
10 are connected together. In one embodiment, only a six by six array
11 (36 Schottky diodes) is connected together in parallel.

12 In one alternative embodiment, aluminum is employed instead of
13 tungsten and silicide. In another alternative embodiment, tungsten is
14 employed instead of aluminum to interconnect contacts, and the step of
15 forming tungsten plugs is omitted.

16 In an alternative embodiment (Fig. 47), each Schottky diode
17 includes a p+ region 252 encircling a "p-" p-well region 254 and is
18 formed by a method substantially identical to the method described
19 above except with p-type material substituted for n-type material and
20 vice versa. More particularly, in this alternative embodiment, the
21 following steps are performed.

22 First, an n-type substrate 256 is provided (Fig. 44). Next, a
23 common p-well region 258 is defined relative the substrate 256. The
24 common p-well region 258 defines the p-well regions 254 for each of

1 the Schottky diodes. Next, an insulator 260 such as borophosphosilicate
2 glass (BPSG) is formed over the p-well region 258. Next, an etching
3 step is performed to etch away regions of the insulator for definition
4 of contact holes, and areas 264 generally encircling or surrounding the
5 contact holes (Fig. 45). In a preferred embodiment, the contact
6 holes 262 all have the same diameter (or peripheral extent) to facilitate
7 subsequent filling of the contact holes 262 with Tungsten or another
8 conductor. In an alternative embodiment, different contact holes 262
9 have different diameters. In the process of the illustrated embodiment,
10 the contact holes do not need to be completely filled, and all contact
11 holes therefore do not need to be the same size.

12 In the illustrated embodiment, the p+regions 252 are formed in
13 the p-well regions by diffusion after the etching has been performed,
14 via the openings 264 encircling the contact holes. The p+regions 252
15 can be formed by other processes or at other times. For example, the
16 p+regions 252 can be formed before the insulator is formed over the
17 p-well region 258.

18 Next, a Schottky forming metal 266 such as Titanium is formed
19 in the contact hole openings 262. In the illustrated embodiment, the
20 Schottky forming metal 266 is deposited on the surface of the p-well
21 region 258 via the contact hole openings 262. In one embodiment, the
22 thickness of the deposited metal is about 200 Å. The metal 266 is
23 annealed to form a stable silicide interface 268 to the p-well region
24 258.

1 If it is desired to fill the contact holes 262, a metal such as
2 tungsten 270 is deposited into the contact holes (Fig. 46). The
3 tungsten 270 is then planarized to form final contact structures.

4 Then, an interconnect metallization step is performed (Fig. 47).
5 For example, copper doped aluminum 272 is deposited (e.g. sputtered)
6 over the wafer, then the wafer is masked and etched to remove
7 unwanted areas. The mask defines a pattern to interconnect the
8 contacts as desired.

9 The above described processes for forming a Schottky diode are
10 preferred over a process wherein, after the contact holes are etched, ion
11 implantation of phosphorus into the holes is performed. In such a
12 process, the implant would be a two step process, with a low energy
13 implant (e.g., 35 keV of 4×10^{12} ions/cm²) followed by a high energy
14 implant (e.g., 120 keV of 4×10^{12} ions/cm²). Such implants cause a high
15 doping level at the bottom of the contact hole, which prevents
16 formation of a low leakage Schottky diode. The preferred processes
17 described above eliminates these two contact implants, and allows for
18 formation of a good quality Schottky diode.

19 Figs. 8.0101AA-CB provide a circuit drawing of the Schottky diode
20 detector "diodedet." Figs. 8.0101AA-CB actually show two Schottky
21 diode detectors. The lower Schottky diode detector shown in Figs.
22 8.0101AA-CB is a replicated or dummy detector which generates a
23 signal for the complement side of the differential amplifier "videoamp1."
24 The structure of the dummy Schottky diode detector is similar to the

1 real Schottky diode detector so that any noise coupled through ground
2 or possibly through Vdd is replicated on both sides of the differential
3 amplifier "videoamp1" and so that the common mode rejection of the
4 amplifier will result in little noise making it through the amplifier chain.
5 Bias current to the Schottky diode detector is provided by the current
6 source transistors having gates connected to "BIAS1" and "BIAS2"
7 respectively. A path for that current is through the antenna. Thus,
8 the antenna is biased to a high potential Vdd. The array of
9 capacitors in Figs. 8.0101AA-CB is a series capacitance that couples the
10 output of the Schottky detector to the input of the video amp
11 "videoamp1" and allows an independent bias level to be set at the
12 input of the video amp "videoamp1." The value of that capacitor in
13 conjunction with the effective resistance seen looking into the amplifier
14 "videoamp1" determines the high pass response of the amplifier
15 "videoamp1." The values of the capacitor and effective resistance
16 determine the lowest frequency at which the amplifiers can respond, and
17 that frequency is selected to be low enough so that none of the
18 information contained in the base band signal is lost.

19 Figs. 8.0102AA-BD provide a circuit drawing of the CMOS
20 detector "cmosdet" which is employed in an alternative embodiment.

21 22 Details of Quick Bias AC-Coupled Video Amplifier

23 Fig. 48 provides a simplified circuit schematic of a quick bias AC-
24 coupled video amplifier 270. The video amplifier goes from a power

1 down (unbiased) state to a fully biased state quickly despite a large
2 value effective resistance and capacitor used to bias and couple the
3 amplifier.

4 The video amplifier 270 has an input adapted to be connected to
5 V_{in} and includes coupling capacitors 292 and 294 at the input.

6 The video amplifier includes a voltage divider 276 including two
7 resistors 278 and 280 in series, and four transistors 282, 284, 286,
8 and 288 shown to the right of a voltage divider in Fig. 48.
9 Transistors 286 and 288, the rightmost two of the four transistors, are
10 long L (length), narrow W (width) p-channel devices operated in linear
11 mode to provide very high effective resistance R_{EFF} . Transistors 286
12 and 288 are used instead of resistors because it is hard to provide high
13 resistances using resistors without generating undesirable parasitic
14 capacitance and without taking up more space on an integrated circuit
15 die. The video amplifier 270 includes a differential amplifier 290. The
16 voltage divider 276 sets a bias voltage at the inputs of the differential
17 amplifier 290. The effective resistance R_{EFF} , in conjunction with the
18 value of coupling capacitor 292 or 294, sets the angular high pass roll
19 off frequency for the amplifier according to a relationship of
20 $\omega_{HP} = 1/((R_{EFF} + R1 || R2)C1)$ where ω is angular frequency (2π times
21 frequency), R1 and R2 are the values of the resistors 278 and 280
22 included in the voltage divider 276, and C1 is the value of one of the
23 coupling capacitors. The values of R_{EFF} , and the coupling capacitors
24 are adjusted to achieve the desired high pass roll off frequency ω_{HP} as

1 illustrated in Fig. 49. The high pass roll off frequency determines what
2 frequencies will be amplified or attenuated. The high pass roll off
3 frequency is set low enough so that important data is not excluded.

4 In many applications, the values of these components are high.
5 For example, in the integrated circuit 16, R_{EFF} is approximately two
6 MegaOhms, and the capacitance of each of the coupling capacitors 292
7 and 294 is approximately one picoFarad, which gives an angular high
8 pass frequency of approximately $1/((2\text{MegaOhms})(1\text{pF}))=500$
9 kiloradians/second, or a high pass frequency of $500/2\pi=79.6$ kHz.

10 In a powered down state, input V_{reg} is zero. Upon power up,
11 there is a delay before the inputs reach the desired bias voltage,
12 according to a relationship $V_{BIAS}=R1/(R1+R2)V_{reg}$. The time constant
13 equals $R_{EFF}C1$ which is approximately equal to two microseconds.

14 If it is decided to wait five time constants, this requires about ten
15 microseconds.

16 In accordance with the invention, transistors 282 and 284 are
17 added (the two leftmost transistors of the four). These are short L
18 (length) wide W (width) devices which allow the bias voltage to be
19 established in much less time by shorting around the high resistance of
20 the right two transistors 286 and 288. The time constant is thereby
21 reduced. This shorting occurs when an input RXEN is low. Before
22 using the circuit as an amplifier, RXEN is taken high (after bias
23 voltage is achieved). This restores the desired frequency behavior.

1 Figs. 8.0103AA-CF provide a circuit drawing of the video amp
2 "videoamp1." The video amp "videoamp1" is a differential amplifier
3 with a cascode device isolating a resistor load from differential
4 transistors of the amplifier. This lowers capacitance and improves the
5 frequency response of the amplifier. Bias is provided by a resistor
6 divider shown on the upper left of Figs. 8.0103AA-CF, which resistor
7 divider provides a potential to two p-channel transistors found almost
8 in the center of the Figs. 8.0103AA-CF. Each of these p-channel
9 transistors defines a very large resistance, effectively on the order of
10 one to two megaOhms connecting to the nodes of the amplifier to
11 provide the bias. The remaining p-channel devices shown left of center
12 in Figs. 8.0103AA-CF are shorting devices which short out the two
13 p-channel transistors during the period when the receiver is being
14 powered on out of the sleep mode. The function of these remaining
15 p-channel devices is to cause the inputs to the receiver to come up to
16 the bias level as quickly as possible. They are then shut off in order
17 to leave the circuit with only the high resistance p-channel devices
18 providing the bias. This is necessary from a frequency response
19 standpoint.

20 Figs. 8.0104AA-BC provide a circuit drawing of the video amp
21 "videoamp2." The video amp "videoamp2" operates in a manner similar
22 to operation of the video amp "videoamp1." The video amp
23 "videoamp1" has a higher bias current than the video amp "videoamp2."
24 The reason for this is to minimize the noise generated in the amplifier.

1 Figs. 8.0105AA-EE provide a circuit drawing of the comparator
2 "comparator." The comparator has biasing considerations similar to the
3 biasing considerations for the video amps, and has a biasing network
4 shown at the left in Figs. 8.0105AA-EE, at the inputs, which is similar
5 to the biasing networks in the video amps. The function of the
6 comparator "comparator" is to ensure an output at a full digital level.

7 Figs. 8.0106AA-CD provide a circuit drawing of an RF detect
8 circuit "rxdet." This circuit generates an RF detect signal. The circuit
9 includes an input switch that is either high or low, and a capacitor.
10 If the input switch is high for a sufficient percentage of the time, the
11 input switch will charge up the capacitor. The capacitor has a
12 continual discharge leakage current. As long as the input switch is high
13 sufficiently frequently, the input switch will overcome the capacitor
14 leakage current, and the circuit "rxdet" will put out an RF detect
15 signal.

16 Figs. 8.0107AA-GN provide a circuit drawing showing construction
17 details of the receiver bias generator "rxbias." The receiver bias
18 generator includes a series of current mirrors to produce bias currents
19 for various stages of the receiver.

20 Figs. 8.0108AA-AC provide a circuit drawing showing construction
21 details of a data transition detector "datatx." The data transition
22 detector has an input connected to the digital level output of the
23 comparator "comparator" of the receiver "rx" in Figs. 8.01AA-DE. The
24 data transition detector generates a high going pulse every time there

1 is a transition from high to low or from low to high in the data
2 output by the comparator "comparator." These transitions are tested
3 by other circuitry, described below, to determine whether or not a valid
4 signal is being received.

5 6 Details of Low Power Frequency Locked Loop

7 As previously discussed, the integrated circuit 16 periodically
8 checks if a radio frequency signal is being received by the receiver.
9 The integrated circuit 16 includes a timer setting the period for the
10 checking, the timer comprising a frequency locked loop "lpfll."

11 The low power frequency locked loop "lpfll" is shown in greater
12 detail in Figs. 8.02AA-BC. This is also shown in a simplified schematic
13 in Fig. 24. In the embodiment shown in Fig. 24, the device 12
14 includes a frequency locked loop (or phase locked loop) 54, a
15 divider 55 coupled to the input of the loop 54, and a divider 56
16 coupled to the output of the loop 54. A clock (e.g. 9.54 MHz) that
17 is recovered from an incoming radio frequency command from the
18 interrogator 26 is supplied to the frequency locked loop (or phase
19 locked loop) 54 after being passed through the divider 55. The terms
20 "phase locked loop" or "frequency locked loop" as used herein are
21 meant to describe physical structure, not a state of operation. The
22 term "locked" does not imply that the circuitry is operating, or
23 functioning in a locked condition. Thus, as used herein, "locked" is a
24 term for assisting definition of a particular circuit configuration and is

1 not meant to imply a required state of operation for the circuit. To
2 avoid ambiguity, the appended claims use the terms "phase lock loop"
3 or "frequency lock loop" instead of "phase locked loop" or "frequency
4 locked loop" to indicate that state of operation is not being claimed.

5 Phase locked loops and frequency locked loops are similar to one
6 another, except that a phase locked loop tracks phase as well as
7 frequency. A phase locked loop includes a phase detector having a
8 first input receiving the incoming message, having a second input, and
9 having an output; a loop filter having an input coupled to the output
10 of the phase detector and having an output; a voltage controlled
11 oscillator having an input coupled to the output of the loop filter, and
12 having an output defining an output of the phase locked loop; and a
13 divider having an input coupled to the output of the voltage controlled
14 oscillator and having an output connected to the second input of the
15 phase detector. The phase detector produces an output voltage
16 proportional to the phase difference of two input signals. The loop
17 filter is used to control the dynamics of the phase locked loop. The
18 voltage controlled oscillator produces an AC output having a frequency
19 proportional to input control voltage. The divider produces an output
20 signal having a frequency that is an integer division of the input signal.
21 The loop filter includes a capacitor on a control node of the voltage
22 controlled oscillator.

23 The frequency locked loop 54 includes a frequency comparator 57
24 receiving the divided recovered clock, an up/down counter 58 connected

1 to the output of the frequency comparator, and a current controlled
2 oscillator 59 connected to the output of the up/down counter. The
3 output of the current controlled oscillator 59 is fed back to the
4 frequency comparator 57, and to the divider 56. The divider 56 is
5 programmable (in response to a radio frequency command from the
6 interrogator 26) in one embodiment of the invention. To conserve
7 power, the loop 54 is enabled only during processing of a command
8 from the interrogator 26, during which time a recovered clock reference
9 signal is available. In the illustrated embodiment, the current controlled
10 oscillator 59 is a low power current controlled oscillator "lpcco" shown
11 in Figs. 8.0204AA-EJ.

12 Figs. 8.02AA-BC provide a circuit drawing of the low power
13 frequency locked loop "lpfl." This circuit generates a clock which is
14 used in multiple places to time the interval between wake ups. The
15 clock is used as a reference for the timed lock out function, and for
16 the alarm timer wake up function. In a preferred embodiment, the low
17 power frequency locked loop "lpfl" generates a 8 kHz clock. The low
18 power frequency locked loop includes a current controlled oscillator
19 "lpcco" that consumes very little current and that runs continuously from
20 the time power is first supplied to the integrated circuit 16 ("power
21 up") until power is removed from the integrated circuit 16. During
22 power up, the low power frequency locked loop "lpfl" attempts to
23 synchronize to the main clock recovery oscillator "dcr" (described below).
24 However, that oscillator is not calibrated to anything yet because it has

1 just been powered on. Still, an initial frequency is set for the low
2 power frequency locked loop "lpfll." On the first successful
3 communication with an interrogator, the low power frequency locked
4 loop "lpfll" is actually calibrated to a known clock frequency and set
5 to a desired frequency (8 kHz in the illustrated embodiment).

6 The low power frequency locked loop includes a divider shown at
7 the top of Figs. 8.02AA-CB. The divider divides down an input clock
8 signal. In the illustrated embodiment, the input clock signal is a 9.5
9 MHz clock signal. The input clock signal is divided down by a desired
10 factor to get a reference clock for the actual loop shown at the bottom
11 of Figs. 8.02AA-CB. In the preferred embodiment, the reference clock
12 for the loop shown in Figs. 8.02AA-CB runs at 8 kHz. The loop
13 receives a loop enable signal "LoopEN", shown at the lower left of
14 Figs. 8.02AA-CB. The loop enable signal "LoopEN" enables this
15 frequency locked loop to operate in a loop configuration. The loop
16 enable signal "LoopEN" is asserted when a valid message has been
17 certified and on power up. Those are the only two times the loop
18 enable signal is asserted.

19 The frequency of the current controlled oscillator "lpcco" is
20 determined by current input into the current controlled oscillator
21 "lpcco." A selection of the number of current steps for controlling the
22 oscillator is made by the outputs of the up/down counter "udcounter."
23 The up/down counter has outputs select 1 "Sel1," select 2 "Sel2," select
24 4 "Sel4," and select 8 "Sel8." The outputs of the up/down counter are

1 labelled according to their binary weights, and that is also how currents
2 are rated within the current controlled oscillator. When the loop is
3 disabled, at the end of processing of a valid command, the count on
4 the output of the up/down counter is frozen so that the select 1
5 through select 8 lines remain constant and they keep that same
6 frequency in the low power frequency locked loop "lpfll" until the next
7 valid command is processed. At the time when the next valid command
8 is processed, if the clock frequency of the low power frequency locked
9 loop has drifted, the loop sets the frequency back to the desired
10 frequency (e.g., 8 kHz).

11 Figs. 8.0201AA-AB provide a circuit drawing showing construction
12 details of a timed lockout divider cell "tldcel_bypass" included in the
13 circuit of Figs. 8.02AA-BC.

14 Figs. 8.0202AA-CD provide a circuit drawing of a frequency
15 comparator "freqcomp" of the frequency locked loop "lpfll." The
16 frequency comparator counts a certain number of cycles of the
17 reference clock and also counts how many cycles of the low power
18 clock occurred within that number of cycles. The frequency comparator
19 thus determines whether the low power clock "lpfll" is running too fast,
20 too slow, or on time. If the clock is running too fast or too slow, the
21 frequency comparator makes an adjustment by causing the counter
22 "udcounter" to either count up or count down. If no adjustment is
23 necessary, the frequency comparator makes no adjustment to the
24 counter.

1 Figs. 8.0203AA-BC provide a circuit drawing showing construction
2 details of the up/down counter "udcounter" included in the low power
3 frequency locked loop "lpfll." The counter has some logic on the
4 counter's output so that if the counter counts all the way down to
5 zero, the counter does not wrap around and go to all ones. Instead,
6 the counter stops at zero (until a signal requesting an up count is
7 received). Similarly, if the counter counts all the way up to all ones,
8 the counter does not wrap around to all zeros. Instead, the counter
9 stops at all ones (until a signal requesting a down count is received).

10 Figs. 8.020301AA-BB provide a circuit drawing showing construction
11 details of an adder "udcounter_adder" included in the up/down counter.

12 Figs. 8.020302AA-AB provide a circuit drawing showing construction
13 details of a D type flip-flop "udcounter_dff" included in the up/down
14 counter.

15 16 Details of Low Power Current Controlled Oscillator

17 The integrated circuit 16 includes the low power current controlled
18 oscillator "lpcco." The oscillator consumes very little current (e.g., less
19 than 100 nA). The oscillator "lpcco" includes digital input lines, and
20 oscillates at a frequency controlled by the digital input lines. The
21 circuit includes a thermal generator, a digitally controlled current mirror,
22 an oscillator, and an output driver.

23 Figs. 8.0204AA-EJ provide a circuit drawing of the low power
24 current controlled oscillator "lpcco." The low power current controlled

1 oscillator "lpcco" includes a thermal voltage generator, including a string
2 of resistors, shown in Figs. 8.0204AA-EJ in the upper left corner. The
3 thermal voltage generator generates a small voltage proportional to kT/q
4 across the string of resistors where k is Boltzmann's constant, 1.38×10^{-23}
5 Joules per degree Kelvin, T is temperature in degrees Kelvin, and q is
6 the electron charge in Coulombs. The voltage kT/q is approximately
7 equal to 26 mV at room temperature. That small voltage divided by
8 the resistor value sets the current in the circuit. This current is
9 approximately equal to $(kT/qR) \ln ((W/L)Q1)/(W/L)Q2)$. In the
10 illustrated embodiment, the current is set to a low value (e.g.,
11 approximately three nano-amps).

12 Thermal generators are known in the art. See for example,
13 "CMOS Analog Integrated Circuits Based on Weak Inversion Operation"
14 by Eric Vittoz and Jean Fellrath, IEEE Journal of Solid-State Circuits,
15 Vol. SC-12, No. 3, June 1977. See particularly Fig. 8 of this article,
16 and the associated description.

17 The low power current controlled oscillator "lpcco" also includes
18 a wake up circuit shown to the far left of the thermal voltage
19 generator that causes a much higher current to flow initially to turn on
20 the feedback loop. The wake up circuit then shuts off and leaves the
21 low value (nano-amp) current flowing. Thus, initialization occurs on
22 power up and the wake up circuit is off after that unless power is
23 removed and reapplied. The outputs of the up/down counter
24 "udcounter," select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select

1 8 "Sel8" come into the low power current controlled oscillator as shown
2 on the left edge of Figs. 8.0204AA-EJ. The low power current
3 controlled oscillator further includes control circuitry shown on the
4 bottom strip of Figs. 8.0204AA-EJ. These outputs of the up/down
5 counter control the number of currents that are mirrored into this
6 control circuitry by a current mirror. The current mirror is digitally
7 controlled and weightings are binary in the illustrated embodiment;
8 however, any weighting scheme can be used. The current mirror
9 includes transistors operating in the subthreshold, or weak inversion
10 mode, due to the extremely low current level.

11 More particularly, referring to Figs. 8.0204AA-EJ, there are five
12 transistors to the right of the string of resistors, mirrored down to one
13 about the center of the page providing a divide by five. Current is
14 then mirrored through all the p-channel devices. The block shown in
15 the upper right of Figs. 8.0204AA-EJ is a selectable current mirror.
16 The first stage generates one current equal to the reference current and
17 that is always flowing into the n-channel diode down at the bottom of
18 that stack. Shown to the right of the n-channel diode are the
19 selectable groups of p-channels. The first one has one, the next two,
20 the next four, the next eight in a binary sequence. The transistors
21 shown below the p-channels transistors are select devices and they are
22 controlled by the digital signals select 1 "Sel1," select 2 "Sel2," select
23 4 "Sel4," and select 8 "Sel8." Thus, the number of currents can be
24

1 selected and however many are selected are added into the one that
2 is always flowing in the diode.

3 The current from groups of p-channel transistors that are not
4 selected is diverted over to a separate or second diode shown on the
5 far right of Figs. 8.0204AA-EJ. This is so that when a block of
6 transistors is not selected, their drain nodes do not get pulled up to
7 V_{DD} . By sinking the current in this second diode, the voltage at the
8 drain node of an unselected block of transistors is kept down near the
9 voltage at which it will operate when and if it is actually connected
10 over to the first diode. This is so that, upon switching a select line,
11 a capacitance doesn't have to be charged from V_{DD} down to the
12 proper operating voltage. In any case, the selected number of currents
13 are added together into the first diode, and then that voltage is carried
14 on the line shown in Figs.8.0204AA-EJ as going down the right side of
15 page, which line has a capacitor tied to it. That capacitor is a filter
16 capacitor so that the voltage on that node does not change abruptly
17 when the select lines change or when some unrelated signal nearby
18 switches. Since all of these transistors are operating in a sub-threshold
19 or weak inversion mode, a small change in the voltage on their gate
20 will otherwise result in a rather large impact on the operation of the
21 circuit. That line is the input for the circuitry shown across the
22 bottom of Figs.8.0204AA-EJ. There is a current mirror situation there,
23 so that the sum of all the selected currents plus the one default
24 current flowing in the diode above is mirrored and flows through the

1 p-channel devices of this circuitry. There is then another mirror to
2 generate bias voltages for the n-channel current source devices for the
3 VCO ring oscillator. The p-channel gate voltages are used in mirroring
4 into the p-channel load devices of the same ring oscillator. The
5 frequency of this ring oscillator is controlled by the current mirrored to
6 them.

7 The low power current controlled oscillator includes a four stage
8 ring oscillator. The frequency of oscillation is approximately
9 proportional to the amount of current flowing. The frequency of
10 oscillation of the four stage ring oscillator is directly proportional to its
11 bias current over a wide range of frequencies. For example, frequency
12 is directly proportional to bias current for frequencies between
13 approximately 100 Hz and tens of MHZ (e.g. to twenty MHZ).

14 The low power current controlled oscillator further includes an
15 output driver. In the illustrated embodiment, the output driver includes
16 a comparator circuit receiving the output of the fourth stage ring. The
17 purpose for this comparator is to convert the small output signal of the
18 oscillator to full digital levels. In the illustrated embodiment, full digital
19 levels are zero volts and V_{DD} . In the illustrated embodiment, V_{DD} is
20 3.3 Volts ± 0.3 Volts. In an alternative embodiment, V_{DD} is 5 Volts
21 ± 10 or 20%. Another other suitable values can be employed for V_{DD}
22 and the digital levels.

23 Circuitry is included to eliminate the crossover current in the n
24 and p channel devices in the first few invertors. This is because, when

1 operated at very low current levels, the rise and fall times are long and
2 could allow substantial current to flow in the n and p channel devices
3 during switching.

4 The digital levels are buffered and amplified up by the
5 comparator to provide an output signal from the low power frequency
6 locked loop "lpfl." The output of the low power current controlled
7 oscillator is shown on the right edge of Figs. 8.0204AA-EJ. In the
8 illustrated embodiment, the low power current controlled oscillator
9 operates at eight kHz. However, if desired for alternative embodiments,
10 the low power current controlled oscillator is capable of running at a
11 frequency from approximately 100 Hz to 20 kHz. In an alternative
12 embodiment, the low power current controlled oscillator is capable of
13 running at a frequency from approximately 100 Hz to 30 kHz.

14 The low power current controlled oscillator consumes very little
15 power. For example, in the illustrated embodiment, the low power
16 current controlled oscillator consumes less than a milliAmp. More
17 particularly, in the illustrated embodiment, the low power current
18 controlled oscillator consumes approximately 100 nanoAmps.

19 In an alternative embodiment, instead of using a thermal voltage
20 generator, a transistor is biased in the subthreshold region in order to
21 define the current source and to generate a small current. However,
22 in this embodiment, the voltage on the gate of the transistor is updated
23 periodically as it leaks away.
24

1 Although the low power current controlled oscillator has been
2 described in connection with a radio frequency identification device, the
3 low power current controlled oscillator can be advantageously employed
4 in any battery powered electronic product which must keep track in
5 time.

6 Figs. 8.03AA-AB provide a circuit drawing showing construction
7 details of a counter bit "lpfl_cbit" included in the receiver "rx."

8 Figs. 8.04AA-EE provide a circuit drawing of the wake up
9 controller "rxwu." An input to the wake up controller is a clock signal
10 "LPCLK" from the low power frequency locked loop "lpfl." This clock
11 signal input is shown in the upper left of Figs. 8.04AA-EE. The clock
12 signal "LPCLK" is further divided down to provide certain time
13 intervals available for selection. These are the time intervals at which
14 the integrated circuit 16 will wake up and look for a radio frequency
15 signal. In the illustrated embodiment, these time intervals are set at
16 0.5, 16, 64 and 256 milliseconds. The selection of one of these
17 multiple available time intervals is accomplished via radio frequency
18 command from the interrogator.

19 The wake up controller includes wake up abort logic shown in the
20 lower left of Figs. 8.04AA-EE. The wake up abort logic performs a
21 number of tests (described elsewhere herein) to determine whether the
22 received signal is a valid signal and, if all tests are passed, then the
23 wake up controller asserts a signal on line "RXWU" shown on the right
24

1 of Figs. 8.04AA-EE. This signal wakes up the processor, and the
2 processor then processes the command contained in the message.
3

4 Details of Wake Up Tests

5 Figs. 8.0401AA-AB provide a circuit drawing of a wake up abort
6 logic circuit "wuabort." The wake up abort logic circuit provides for
7 conservation of battery power. If what is received is not a valid
8 message, the wake up abort logic circuit determines this quickly and the
9 device returns to the sleep mode so that the battery is not drained on
10 invalid messages or spurious communication. The wake up abort logic
11 circuit works by counting clock cycles. The wake up abort logic circuit
12 has as an input a clock signal "CHIPCLK" that is the output of the
13 clock recovery oscillator "dcr" (described below). This clock signal is
14 divided down by a factor of four, which results in a value
15 approximately equal to the spread spectrum chip rate. After the clock
16 is actually acquired from a message from the interrogator, the resulting
17 value will be equal to the chip rate.

18 Initially though, when these wake up tests are performed, a clock
19 has not yet been acquired from a message. The wake up abort logic
20 includes an RF Detect Timer, shown on the top, left of Figs. 8.0401AA-
21 EE, which performs a first test. The RF Detect Timer counts a
22 predetermined number of cycles of the clock (e.g., 13 cycles) and, if the
23 RF detect signal from the receiver is not asserted, the wake up is
24 aborted. On the other hand, if the RF detect signal is asserted within

1 those cycles, the wake up abort logic starts the next series of tests
2 without waiting for the end of the predetermined number of cycles.

3 The next series of tests are timed by a counter shown across the
4 center of the page in Figs. 8.0401AA-EE. For the next tests,
5 transitions in the incoming data stream are counted within a certain
6 time interval and the number of transitions must fall within a certain
7 range in order to pass the test. Transitions are counted by the counter
8 shown at the bottom in Figs. 8.0401AA-EE. The range limits are set
9 by knowing the number of transitions that should occur in the data
10 within the amount of time allowed. This is known because each data
11 bit is encoded as a thirty-one chip sequence as described elsewhere
12 herein. The reason there is a range is because the clock has not yet
13 been acquired accurately so there is a range of clock frequencies that
14 must be considered. In the illustrated embodiment, one test checks
15 whether, after five counts of the clock, there has been between greater
16 than or equal to one, and less than eight transitions in the data. If
17 not, the wake up is aborted and the device goes back to sleep. If yes,
18 then the next test is performed.

19 The next test checks whether, after twenty-six clock counts, there
20 are greater than or equal to fourteen and less than thirty-two transitions
21 in the data. If not, wake up is aborted and the chip goes back to the
22 sleep mode. If this test is passed, the wake up abort logic circuit
23 performs tests relating to signals generated by the clock recovery nodes.
24 One such test is a test for chip lock. Chip lock is an indication that

1 clock recovery is proceeding and has actually gotten within a few
2 percent of the desired clock frequency. The final check is whether
3 frequency lock has occurred. Again, these tests are timed. If one of
4 the signals is not asserted by the time the timer signal goes high, then
5 the wake up will be aborted and the device goes back to sleep and
6 will try again after another wake up interval. Frequency lock will come
7 into the logic in the center of the page in Figs. 8.04AA-CB, and that
8 is what causes the RXWU signal to be asserted, thus waking up the
9 processor.

10 Another function of the wake up abort logic shown in Figs.
11 8.0401AA-EE is to discriminate between high rate and low rate. The
12 wake up abort logic measures time while these tests are performed to
13 determine when the interrogator is in high rate, but the chip is in low
14 rate or vice versa and abort out of wake up (return to the sleep
15 mode).

16 These tests will now be described in connection with flowcharts
17 illustrated in Figs. 25-27.

18 The wake up controller "rxwu" was described above in connection
19 with Figs. 8.04AA-EE. The wake up tests performed by the wake up
20 controller are illustrated in flow chart form in Figs. 25-26.

21 When the integrated circuit 16 first wakes up, bias generators and
22 the receiver "rx" are powered on (step S1 in Fig. 25). After ensuring
23 that the bias is on (step S2 in Fig. 25), the master clock "dcr" is
24 started. By design, the master clock "dcr" starts at a frequency below

1 the final frequency it will achieve after the clock recovery circuit "lpfl"
2 extracts the clock frequency from the incoming signal. More
3 particularly, in the illustrated embodiment, the master clock starts at a
4 start frequency above half of the final frequency it will achieve after
5 the clock recovery circuit "lpfl" extracts the clock frequency from the
6 incoming signal. Still more particularly, in the illustrated embodiment,
7 the master clock starts at a start frequency between half and three
8 quarters of the final frequency the master clock will achieve after the
9 clock recovery circuit "lpfl" extracts the clock frequency from the
10 incoming signal. In the illustrated embodiment, the final frequency is
11 38.15 MHZ, and the start frequency is between 20 and 30 MHZ. The
12 master clock includes a frequency locked loop including a voltage
13 controlled oscillator. An offset is applied to the oscillator to make
14 sure that the clock starts at least as fast as 20 MHZ. Then, the
15 frequency locked loop adjusts the frequency to 38.15 MHZ.

16 Because the clock has not yet been acquired from the incoming
17 signal, the clock is a free running oscillator when providing the start
18 frequency. Initial wake up tests are performed at this lower start
19 frequency. The receiver "rx," digital clock and data recovery circuit
20 "dcr," pseudo random number processor "pnproc," and voltage controlled
21 oscillator "vco" are turned on (step S3 in Fig. 25).

22 The input radio frequency signal received from the interrogator 26
23 is a direct sequence spread spectrum input signal in the illustrated
24 embodiment. Spread spectrum techniques are described above. In one

embodiment, incoming radio frequency commands are included in packets that contain, in order of transmission, a preamble, a Barker code, and the command. In one embodiment, each bit of the incoming radio frequency command sent by the interrogator is modulated using a pseudo noise (PN) sequence for direct sequence spread spectrum communication.

After the clock is running, the device 12 is in a receiver on mode illustrated in Fig. 27 by a vertical line marked "WAKEUP RX ON." After the clock is running, the device 12 performs wake up tests (at the lower or start frequency).

A first test is whether the receiver "rx" detects any radio frequency signal within a predetermined number of clock cycles (step S4 in Fig. 25). In the illustrated embodiment, this predetermined number of clock cycles is 13. If no radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device 12 returns to the sleep mode. If a radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device 12 switches to a wake up abort test mode illustrated in Fig. 27 by a vertical line marked "WAKEUP ABORT TESTS," and a second test is performed.

In the second test, a determination is made as to whether a predetermined number of data transition pulses occur within a predetermined number of clock pulses for the radio frequency signal detected by the receiver "rx" (step S5 in Fig. 25). More particularly, the device 12 includes a long counter shown in Figs. 8.0401AA-EE

1 driven by a clock signal "CHIPCLK." The device 12 further includes
2 a circuit "datatx" which detects transitions in the signal received by the
3 receiver "rx" and generates a pulse ("DTX" in Fig. 26) at each
4 transition. The device 12 further includes another counter circuit shown
5 in Figs. 8.0401AA-EE which counts these pulses. Because a valid
6 incoming signal is modulated with a known PN sequence, the number
7 of transitions in a given time for a valid incoming signal is known.
8 The device 12 includes logic "wuabort" that tests whether the proper
9 number of data transition pulses occur within a certain number of clock
10 pulses. More particularly, in the illustrated embodiment, the logic tests
11 whether more than or equal to one and less than eight such data
12 transition pulses occur within five chips. If not, the device returns to
13 the sleep mode. If so, a third test is performed.

14 In the third test, a determination is made as to whether a
15 predetermined number of data transition pulses occur within a
16 predetermined number of clock pulses for the radio frequency signal
17 detected by the receiver "rx" (step S5 in Fig. 26). The third test is
18 similar to the second test, except that the number of data transition
19 pulses is tested against a number of clock pulses that is different from
20 the number in the second test. More particularly, in the illustrated
21 embodiment, the logic tests whether more than or equal to fourteen and
22 less than thirty-two such data transition pulses occur within thirty-one
23 chips. If not, the device 12 returns to the sleep mode.

1 If the above transition tests are passed, the device 12 checks to
2 see if the clock recovery circuit locks onto the incoming clock rate.
3 More particularly, in the illustrated embodiment, a determination is
4 made as to whether a clock is acquired from the incoming signal within
5 6k chips (step S7 in Fig. 26). A determination is then made as to
6 whether frequency lock is achieved within 16k chips (step S9 in Fig.
7 26). The device 12 returns to the sleep mode if any of these tests
8 fail. If these tests are passed, then the device 12 enters a processor
9 on mode illustrated in Fig. 27 by a vertical line marked "PROCESSOR
10 ON." Power is supplied to the processor (step S10 in Fig. 26) and the
11 device 12 waits for the preamble of the incoming message to end and
12 the command to begin.

13 In one embodiment, the tests of Fig. 26 are employed to
14 distinguish between incoming signals with different possible valid chipping
15 rates.

16 More particularly, in the illustrated embodiment, it is known how
17 long each of the various tests should take for valid low chipping rate
18 or high chipping rate signals, and this information can be tested to
19 determine whether the incoming signal is a high rate or low rate signal.

20 Other appropriate tests can be performed in embodiments where
21 spread spectrum is not employed. In these embodiments, knowing how
22 valid data is encoded, the wake up timer and logic still compares the
23 number of transitions received in a given amount of time with an
24 expected number of transitions for a valid signal.

1 Figs. 8.040101AA-AB provide a circuit drawing showing construction
2 details of a counter bit "wuabort-cbit" included in the wake up abort
3 logic.

4 Figs. 8.0402AA-AB provide a circuit drawing showing construction
5 details of a timed lockout divider cell "tldcel" included in the receiver
6 wake up controller.

7 8 Details of Lock Detection in a Digital Clock Recovery Loop

9 In many communications systems, it is necessary to recover a
10 clock signal from the received data. A phase locked loop is one way
11 of recovering such a clock signal. In the illustrated embodiment, such
12 a recovered clock is used as a master clock.

13 The integrated circuit 16 includes the digital clock and data
14 recovery circuit "dcr" which includes a phase locked loop. The phase
15 locked loop includes a voltage controlled oscillator "dcr_vco." The
16 frequency of the voltage controlled oscillator always starts low, at
17 between 50% and 75% of the final desired value. When the voltage
18 controlled oscillator starts running, large steps are taken (Fig. 54). As
19 the frequency approaches the final value, increasingly smaller steps are
20 taken to achieve greater accuracy. The illustrated embodiment employs
21 four step sizes: large, medium, medium-fine, and fine. For example, in
22 the illustrated embodiment, large steps up are employed between 50%
23 to 75% of the final desired value, and medium steps up are then taken
24 above 75% until pump up commands are not issued for a

1 predetermined number of transitions, then medium-fine steps up are
2 employed until the final value is overshoot, then fine steps down are
3 employed.

4 A method is needed to determine when the frequency of the
5 voltage controlled oscillator matches the desired frequencies contained
6 in the received data.

7 The voltage controlled oscillator includes a control node having
8 a voltage indicative of the frequency of the voltage controlled oscillator.
9 The behavior of this node is used to determine when frequency lock
10 has occurred.

11 After the phase locked loop has run long enough to get within
12 a few percent of the final value (at a time illustrated as T_0 in
13 Fig. 54), a signal "SDD" (start data decoding) is generated. This signal
14 "SDD" disables the large and medium steps and enables lock detect
15 circuitry for determining if frequency lock has occurred. A latch
16 "KILLSU" (kill start up) detects when the first fine step pump down
17 occurs (at T_1 in Fig. 54). This enables a latch "FREQLOCK." The
18 latch "FREQLOCK" is set when the first fine step pump up occurs (at
19 a time illustrated as T_2 in Fig. 54). A signal "FREQLOCK" is then
20 indicative that the phase locked loop has reached its final value.

21 In other words, large, medium, then medium-fine steps up are
22 followed by fine steps down. The final value is overshoot, and a
23 frequency lock signal is provided upon occurrence of the first
24 subsequent fine step up.

1 In the illustrated embodiment, the final value of the voltage on
2 the control node of the voltage controlled oscillator, where frequency
3 lock is expected, is approximately 1.2 Volts. In one embodiment, each
4 large step is approximately several hundred millivolts, each medium step
5 has a size approximately in the tens of millivolts (e.g., 25 millivolts),
6 each medium-fine step has a size of approximately a few millivolts (e.g.
7 two millivolts), and each fine step has a size approximately in the
8 tenths of millivolts. Various other relative sizes or numbers of steps
9 are employed in alternative embodiments.

10 The sizes of steps is set using current sources of different values
11 that are turned on for a fixed period of time to drive to the capacitor
12 on the control node of the voltage controlled oscillator.

13 In the illustrated embodiment, the fine step generator is not
14 disabled before time T_0 so there is a possibility that a combination of
15 fine steps with larger steps can take place before time T_0 . In an
16 alternative embodiment, however, the fine step generator is disabled
17 before time T_0 .

18 Figs. 8.05AA-CB provide a circuit drawing of the digital clock and
19 data recovery circuit "dcr." The digital clock and data recovery circuit
20 includes a phase locked loop of a digital design, and a state machine
21 "dcr_statemachine" that drives the phase locked loop. The phase locked
22 loop includes a voltage controlled oscillator "dcr_vco" and control
23 circuitry "dcr_vcocontrol" for the voltage controlled oscillator. The
24 voltage controlled oscillator "dcr_vco" includes a control node ("OUTN")

1 and "OUTP" shown in Figs. 8.0504AA-EE and described below in
2 greater detail) and produces an oscillation at a rate dependent on the
3 value of a voltage applied to the control node. In the illustrated
4 embodiment, the state machine has four states. The phase locked loop
5 produces an output pulse on a line "OUTC" (later labeled
6 "FMASTER"). The digital clock and data recovery circuit attempts to
7 place four pulses of the output clock within one chip time.

8 The state machine "dcr_statemachine" determines when that is not
9 the case and, if not, whether to cause the oscillator to run faster or
10 to run slower. The state machine "dcr_statemachine" then issues
11 appropriate pump up or pump down signals to drive a control node of
12 the oscillator. The voltage controlled oscillator "dcr_vco" starts out at
13 a minimum frequency as determined by an offset current which is
14 present regardless of the loop. This ensures that the oscillator will
15 start up and run at greater than 50% of the final value so that the
16 phase locked loop will converge on the proper frequency. The digital
17 clock and data recovery circuit also includes a PLL start-up circuit
18 "dcr_startup." The acquisition of the clock frequency happens in stages
19 and, initially, the control node moves in large increments towards its
20 final value. The start-up circuit "dcr_startup" provides large increments
21 for controlling the loop. However, as the digital clock and data
22 recovery circuit gets closer to acquisition of clock frequency, control
23 switches from that start up circuit "dcr_startup" over to the state
24 machine "dcr_statemachine." The state machine provides very fine steps

1 as the final convergence is done with very fine steps. The data stream
2 is fed into the circuitry on the upper right. Then the data is sampled
3 during one of the states of the state machine after it has been
4 determined that the data is valid. The data stream is recreated and
5 called "RXCHIPS."

6 Figs. 8.0501AA-BE provide a circuit drawing of the start up circuit
7 "dcr_startup" included in the digital clock and data recovery circuit. In
8 the illustrated embodiment, the start up circuit provides either very
9 large or fairly large steps dependent upon how far from frequency the
10 oscillator is running. The start up circuit also has a counter (shown
11 along the bottom in Figs. 8.0501AA-BE) that determines when there
12 have been no pump up commands issued for a given count of
13 transitions. In the illustrated embodiment, the counter determines when
14 there have been no pump up commands during sixteen transitions. If
15 the given count of transitions are detected in the data and there has
16 been no pump up command (e.g., no pump up medium or pump up
17 fast command) then a signal is asserted on a line "SDD." SDD stands
18 for Start Data Decode and is an indication that the control voltage has
19 converged to within a few percent.

20 Figs. 8.050101AA-BE provide a circuit drawing showing construction
21 details of a shift register cell "dcr_sreg" included in the PLL start up
22 circuit. Figs. 8.050102AA-AB provide a circuit drawing showing
23 construction details of a counter bit "dcr_counterbit" included in the
24 PLL start up circuit.

1 Figs. 8.0502AA-CD provide a circuit drawing of the state machine
2 "dcr_statemachine." In the illustrated embodiment, the state machine
3 has four states. The state machine includes two flip-flops with feedback
4 signals providing the four states. This circuit generates pump up slow,
5 and pump down slow commands for adjusting voltage on a control node
6 of the voltage controlled oscillator.

7 This circuit also has the circuitry that turns off the start up
8 circuit and generates the frequency lock signal. When trying to acquire
9 frequency lock, there will be large and medium pump ups, without any
10 pump downs, until the final desired value is overshoot. At this point,
11 there will be a first pump down slow pulse. When the first pump
12 down slow command is issued, the start up circuitry "dcr_startup" is
13 turned off, which leaves only fine step capability for adjustment in the
14 control voltage. It takes time for the fine steps to bring down the
15 control node voltage to the proper value and the voltage on the control
16 node will overshoot the desired voltage in the negative direction. The
17 state machine will detect that it has gone too far and it will step the
18 voltage back up towards the final value and that first fine step up will
19 be detected and at that point the frequency lock signal is asserted.

20 Figs. 8.0503AA-BB provide a circuit drawing of a bias generator
21 "dcr_bias." The bias generator includes current mirrors that generate
22 the appropriate bias values for the various circuits in the digital clock
23 and data recovery block.
24

1 The digital clock and data recovery circuit "dcr" includes a VCO
2 control voltage generator "dcr_vcocontrol" which is shown in greater
3 detail in Figs. 8.0504AA-EE.

4 The digital clock and data recovery circuit "dcr" employs a phase
5 locked loop to recover the clock frequency from an incoming radio
6 frequency message. Phase locked loops use feedback to maintain an
7 output signal in a predetermined phase relationship with a reference
8 signal.

9 10 Details of Digital Clock Recovery Loop

11 Operation and design of the digital clock and data recovery circuit
12 "dcr" will now be further described with reference to Figs. 61-72

13 In many communications systems it is necessary to recover a clock
14 signal from the received digital data stream. In the device 12, this
15 clock signal is used as the master timing reference to eliminate the
16 need for an external crystal-based timing reference. Typically, a phase
17 locked loop of some type is used to extract the clock.

18 There are many requirements on the phase locked loop used to
19 recover a clock signal from the received digital data stream. Several
20 important ones for this application are that the phase locked loop must
21 acquire the desired frequency without locking to a multiple or sub-
22 multiple of the desired frequency; the phase locked loop must lock to
23 the desired frequency within a certain time of interest; and the phase
24 locked loop must yield consistent performance despite wide variation in

1 device parameters which is inherent in integrated circuit processing.
2 The phase locked loop employed in the illustrated embodiment,
3 embodied in the digital clock recovery circuitry "dcr," satisfies all of
4 these requirements.

5 In the illustrated embodiment, the forward link baseband data is
6 encoded for direct sequence spread spectrum. In the illustrated
7 embodiment, a data bit "1" is represented by a thirty-one chip sequence
8 and a data bit "0" is represented by the logical inversion of the same
9 thirty-one chip sequence.

10 The mode of operation of the device 12 is as follows. The chip
11 periodically awakens from a low-current sleep mode in order to detect
12 whether
13 an incoming RF message is present. The clock recovery loop "dcr" is
14 inactive in the low-current sleep mode. If a message is present, the
15 message is tested to make sure it is a valid message from an
16 interrogator. If the incoming signal passes these tests, the clock
17 recovery loop is enabled, the clock is acquired, the message is
18 processed, and a reply is sent. The device 12 then returns to sleep
19 mode.

20 The digital clock recovery loop is illustrated by reference numeral
21 700 in Fig. 61. The digital clock recovery loop 700 comprises several
22 sub-circuits. The digital clock recovery loop 700 includes a voltage
23 controlled oscillator 702. The voltage controlled oscillator 702 has an
24 output 704, and produces a square wave at output 704 having a

1 frequency controlled by the voltage on an input control node. When
2 the voltage on the control node is zero, the frequency at output 704
3 is at least one half of the final recovered frequency and not greater
4 than the final recovered frequency. The output frequency rises
5 monotonically, nearly linearly, as the control node voltage is increased.
6 This is shown in Fig. 62. More particularly, Fig. 62 illustrates the
7 frequency produced at the output 704 of the voltage controlled oscillator
8 702 relative to a voltage at the input control node.

9 The digital clock recovery loop 700 further includes a charge
10 pump and loop filters which control the rate of change of the voltage
11 on the control node of the voltage controlled oscillator. The charge
12 pump and loop filters are designated in Fig. 61 with reference numeral
13 706.

14 The digital clock recovery loop 700 further includes a start-up
15 circuit 708 which performs frequency detection when the voltage
16 controlled oscillator first starts up and, in conjunction with the charge
17 pump and loop filters 706, causes the voltage on the control node of
18 the voltage controlled oscillator to change rapidly.

19 The digital clock recovery loop 700 further includes a state
20 machine 710 which performs phase detection when the frequency of the
21 voltage controlled oscillator is within a few percent of its final value
22 and, in conjunction with the charge pump and loop filters, causes the
23 voltage on the control node of the voltage controlled oscillator 702 to
24 change slowly.

1 The only analog blocks are the voltage controlled oscillator 702
2 and the charge pump. The rest of the circuits of the digital clock
3 recovery loop are digital circuits which are easy to build at high yield
4 in integrated circuit processes.

5 In the preferred embodiment, the voltage controlled oscillator 702
6 is the voltage controlled oscillator "dcr_vco" shown in the detailed
7 schematic drawings, and has control nodes "OUTN" and "OUTP"; the
8 state machine 710 is the state machine "dcr_statemachine" shown in the
9 detailed schematic drawings; and the start-up circuit 708 is the start-up
10 circuit "dcr_startup" shown in the detailed schematic drawings.

11 The digital clock recovery loop causes the frequency at the output
12 of the voltage controlled oscillator to vary until a predetermined number
13 of this clock fit within the time interval of an identifiable discrete
14 segment of the incoming data. More particularly, in the illustrated
15 embodiment, the digital clock recovery loop causes the frequency at the
16 output of the voltage controlled oscillator to increase until exactly four
17 cycles of the clock fit within the time interval of a single chip. In
18 alternative embodiments, other integer numbers could be used. In the
19 illustrated embodiment, a state machine having four states is employed
20 to cause the frequency at the output of the voltage controlled oscillator
21 to increase until exactly four cycles of the clock fit within the time
22 interval of a single chip. A general description of the behavior of the
23 control node voltage can be found above in the section titled Details
24 of Lock Detection in a Digital Clock Recovery Loop.

1 What follows is a discussion of the operation of each block of
2 the digital clock recovery loop. The start-up circuit 708 is show in Fig.
3 61. Although it may be simplified from the circuitry shown in the
4 detailed schematics including "dcr_startup" shown in Figs. 8.0501AA-BE,
5 the theory of operation is the same.

6 The start-up circuit 708 includes a plurality of flip-flops 712
7 chained together, a plurality of flip-flops 714 chained together, and an
8 exclusive-or gate 716. The exclusive-or gate 716 has an output
9 connected to the input of the first of the flip-flops 714, has an input
10 connected to the output of the last of the flip-flops 712, and has
11 another input connected to the input of the same flip-flop 712. More
12 particularly, in the illustrated embodiment, each flip-flop 712 and 714
13 is a D-type flip-flop and has a D input, a clock input, and a Q output.
14 The D input of flip-flops 712 other than the first flip-flop is connected
15 to the Q output of a previous flip-flop 712. The first flip-flop 712 is
16 connected to the input data "Data In." The D input of flip-flops 714
17 other than the first flip-flop 714 is connected to the Q output of a
18 previous flip-flop 714. The first flip-flop 714 is connected to the
19 output of the exclusive-or gate 716. The clock inputs of the flip-flops
20 712 and 714 are all tied to the output 704 of the voltage controlled
21 oscillator 702. Data is shifted from the D input of each flip-flop to
22 the Q output of the same flip-flop on each clock pulse. Thus, the
23 flip-flops 712 as a group define a shift register, and the flip-flops 714
24 as a group define a shift register.

1 The start-up circuit 708 further includes an AND gate 718 that
2 has one input that is the output of the exclusive-or gate 716, has a
3 second input that is the output of the second of the flip-flops 714, and
4 defines an output "Puf1" (a first pump up fast output). The start-up
5 circuit 708 further includes an AND gate 720 that has one input that
6 is the output of the exclusive-or gate 716, has a second input that is
7 the output of the third of the flip-flops 714, and defines an output
8 "Puf2" (a second pump up fast output).

9 The start-up circuit 708 further includes a counter 722 that
10 receives as inputs "Puf1" and "Puf2" and generates an output "SDD"
11 (start data decode) when the output of the voltage controlled oscillator
12 702 is close to its final value.

13 The exclusive-or gate 716 in the center of the page generates a
14 high output whenever there is a transition in the data as sampled by
15 the clock signal output by the voltage controlled oscillator 702 output
16 clock. Assume for discussion that data is latched into all flip-flops 712
17 and 714 on the falling edge of the clock. Puf2 goes high when three
18 falling edges of the clock occur within one chip because the inputs of
19 the AND gate are spaced apart by three flip-flops. Three falling edges
20 of the clock occur within one chip when the frequency is between 75%
21 and 100% of the final value. Puf1 goes high when two falling edges
22 of the clock occur within one chip because the inputs of the AND gate
23 are spaced apart by two flip-flops. Two falling edges of the clock
24 occur within one chip when the clock frequency is 50% to 75% of its

1 final value. This is shown on the waveform diagram of Fig. 63 for the
2 case when the frequency is exactly 50%. Puf1 could be used to pump
3 up the control node of the voltage controlled oscillator 702 rapidly.
4 Puf2 could be used to pump up the control node of the voltage
5 controlled oscillator 702 at a rate equal to that for Puf1 (as is shown
6 in Fig. 61) or it could pump at a slower rate (as is done in the
7 circuitry shown in the detailed schematics). As the clock frequency
8 approaches 75% of final in the Puf1 case or 100% of final in the Puf2
9 case, pump up signals occur infrequently as error must accumulate over
10 a long time to cause the appropriate number of clock edges to shift
11 within a chip. This is used to detect when the clock frequency is close
12 to its final value.

13 The counter 722 counts transition pulses until it is cleared by a
14 Puf1 or Puf2 signal. If a predetermined large number of transitions are
15 counted before a pump up occurs, a signal is asserted on a line SDD
16 (start data decode). In the illustrated embodiment, if sixteen transitions
17 are counted before a pump up occurs, a signal is asserted on line
18 SDD. This indicates that the voltage on the control node of the
19 voltage controlled oscillator is within a few percent of its final value,
20 allowing data to be accurately recovered.

21 In the illustrated embodiment, the state machine 710 issues finer
22 pump-up signals than the start-up circuit 708, and can also issue pump-
23 down signals. In the illustrated embodiment, the start-up circuit 708
24 only issues pump up signals. The state machine 710 has as many

1 states as the number of clock cycles which fit within one chip time.
2 In the illustrated embodiment, the state machine has four states. The
3 state machine 710 counts clock pulses and expects the data to transition
4 at a count of one every time there is a transition. If the transition
5 actually occurs at a count of four then the clock is too slow and a
6 pump up is issued. If the transition actually occurs at a count of two
7 then the clock is too fast and a pump down is issued. If the
8 transition actually occurs at a count of three, it is not known whether
9 the clock is fast or slow so no adjustment is made to the voltage
10 controlled oscillator. A state diagram is shown in Fig. 64.

11 Design of a clocked sequential circuit is known in the art. See,
12 for example, chapter 6 of Digital Logic and Computer Design by M.
13 Morris Mano, 1979, Prentice-Hall, Inc. A typical design procedure
14 involves describing circuit behavior using a state diagram (see Fig. 64),
15 obtaining a state table (see Fig. 66), assigning binary values to each
16 state (see Fig. 64), determining the number of flip-flops needed (see
17 Fig. 65), choosing the type of flip-flops to be used (see Fig. 65), using
18 Karnaugh maps or other simplification methods, deriving circuit output
19 functions and flip-flop input functions (see Figs. 67 and 68), and
20 drawing the logic diagram. The numbers in parentheses in Fig. 64 are
21 the binary state numbers. ENDT enables the sampling of the data
22 (always at state two when no transition occurred). There are several
23 ways to implement a circuit to perform functions of a state diagram.
24 Assume that Q1 and Q0 are the binary state numbers in parentheses

above (Q1 on the left, Q0 on the right), and that D1 and D0 are the next state values of Q1 and Q0, respectively. This is illustrated in Fig. 65. The flip-flop outputs Q0 and Q1 are the states. Then, a state table can be derived. This is shown in Fig. 66. Using Karnaugh maps (see Figs. 67 and 68), minimum logic to perform the desired function can be derived. It should be noted, of course, that minimum logic need not be employed--logic involving an increased number of logic gates but performing the same desired function can also be employed. From the Karnaugh map shown in Fig. 67, the following equation can be derived:

$$D0 = Q1 + TX \cdot Q0 + En \cdot TX$$

which can also be written as:

$$D0 = [Q1' \cdot (TX \cdot Q0)' \cdot (En \cdot TX)']'$$

where the symbol "+" represents a logical OR, the symbol "." represents a logical AND, and the symbol "'" represents a logical NOT.

From the Karnaugh map shown in Fig. 68, the following equation can be derived:

$$D1 = TX' \cdot Q1 \cdot Q0' + En \cdot TX' \cdot Q0'$$

which can also be written as:

$$D1 = [(TX' \cdot Q1 \cdot Q0')' \cdot (En \cdot TX' \cdot Q0')']'$$

where the symbol "+" represents a logical OR, the symbol "." represents a logical AND, and the symbol "'" represents a logical NOT.

Logic to implement these equations is shown in Figs. 69 and 70.

Paths shown in Fig. 64 are defined as follows:

1 $ENDT = Q1' \cdot Q0 \cdot TX'$

2 $PumpUpSlow = Q1 \cdot Q0' \cdot TX$; and

3 $PumpDownSlow = Q1' \cdot Q0 \cdot TX$

4 Logic used to implement the state machine, in accordance with
5 one embodiment of the invention, is shown in Figs. 8.0502AA-CD.

6 A simplified timing diagram showing operation of the state
7 machine is shown in Fig. 71. The crowding and separation of states
8 in Fig. 71 is exaggerated to show the various modes of operation in a
9 compact form. More particularly, it is highly unlikely that a pump
10 down signal would be necessary so soon after a pump up signal as is
11 depicted in Fig. 71.

12 The state machine is trying to fit four cycles of the output of the
13 voltage controlled oscillator in one chip width. Referring simultaneously
14 to Figs. 71 and 64, starting at the first occurrence of state 3 in Fig.
15 71, there is no transition, so the state machine will proceed to state
16 4 on the next clock. At state 4, there is no transition, so the state
17 machine will proceed to state 1 at the next clock. At state 1, there
18 is a transition in the waveform. The state machine always proceeds to
19 state 2 from state 1. At state 2, there is no transition. From state
20 2, the state machine proceeds to state 3. This cycle is repeated and
21 these paths are followed unless the clock recovery loop drifts off
22 frequency.

23 If the clock recovery loop drifts off frequency, other paths of the
24 state diagram of Fig. 64 are followed. For example, if a transition is

1 seen at state 4, the voltage controlled oscillator is oscillating too slowly,
2 and a PumpUpSlow is issued. The state machine skips state 1 and
3 goes to state 2.

4 If, after going from state 1 to state 2, a transition is seen, the
5 voltage controlled oscillator is oscillating too fast. The state machine
6 will go from state 2 to state 2 so that state 2 is now in the proper
7 position.

8 If a transition is seen at state 3, the voltage controlled oscillator
9 may either be oscillating too fast or too slowly, so no pump up or
10 pump down signals are issued. Instead, the state machine proceeds to
11 state 2.

12 The control functions performed by the start-up circuit and state
13 machines can be used to control the frequency of any voltage controlled
14 oscillator. The particular voltage controlled oscillator 702 that is
15 employed in the illustrated embodiment is shown in Figs. 8.0505AA-EF.

16 In the illustrated embodiment, the voltage controlled oscillator 702
17 includes a current controlled four-stage ring oscillator shown in the
18 center of Figs. 8.0505AA-EF. The frequency of oscillation is very much
19 linearly proportional to the bias current flowing in each stage.

20 The voltage controlled oscillator 702 further includes an
21 Operational Transconductance Amplifier shown on the left side of Figs.
22 8.0505AA-EF. This Operational Transconductance Amplifier converts a
23 voltage difference at its inputs to a current difference at its outputs.
24

1 This Operational Transconductance Amplifier has a characteristic that is
2 linear over a range of input voltage.

3 The composite circuit is a voltage controlled oscillator 702 with
4 nearly linear operation about the operating point of 38.15 MHz. The
5 circuit shown to the right in Figs. 8.0505AA-EF converts the small
6 signal output of the oscillator to full digital levels.

7 The input reference voltage is generated by a bandgap regulator
8 and has a value of about 1.2 volts. The circuit is designed so that at
9 nominal conditions the control node needs to pump to about equal to
10 the reference voltage to oscillate at 38.15 MHz.

11 The start-up circuit requires that the oscillator start at greater
12 than half frequency (approximately 19 MHz) and less than full frequency
13 over all operating conditions and for all process variations. This
14 oscillator start frequency is set by providing an offset current to the
15 bias of the oscillator which is not controlled by the input voltage. In
16 the illustrated embodiment, the range of allowed offset currents is
17 $7.437\mu\text{A}$ to $9.763\mu\text{A}$. A value of $8.2\mu\text{A}$ was chosen. Thus, the
18 oscillator start frequency will vary from about 20 MHz to 34 MHz.

19 The charge pump and loop filters 706 are shown in greater detail
20 in Figs. 8.0504AA-EE. The filter capacitors are shown on the right
21 side of Figs. 8.0504AA-EE. In the illustrated embodiment, the filter
22 capacitors include a first group of ten capacitors, defining a total
23 capacitance of 10 pF, and an second group of ten capacitors, defining
24 a total capacitance of 10 pF. In Figs. 8.0504AA-EE, the first group

1 of ten capacitors is shown above the second group of ten capacitors.
2 Other values or numbers are possible. In the illustrated embodiment,
3 the lower group of capacitors is connected to the reference voltage
4 input to the voltage controlled oscillator 702. The upper group of
5 capacitors is connected to the control node input of the voltage
6 controlled oscillator 702. The control node always starts at 0 Volts and
7 is pumped up. The other (reference) side is always at the bandgap
8 voltage.

9 The charge pump is shown in the center of Figs. 8.0504AA-EE.
10 In the illustrated embodiment, there are actually four charge pumps.
11 The method employed is to steer a current to charge or discharge the
12 10 pF capacitor for a prescribed period of time (one cycle of the
13 recovered clock, in the illustrated embodiment). The change in control
14 voltage for a single pump is:

$$\Delta V = (I/C) \Delta t$$

15
16 The lower three of the illustrated charge pumps are controlled by
17 the start-up circuit 708 and can only pump up. The upper pump is
18 controlled by the state machine 710 and can pump up or down in fine
19 steps. The step sizes are controlled by the current value which is set
20 accurately using a bandgap regulator to generate a reference current
21 and using current mirrors to set the pump current. The step sizes
22 used in the illustrated embodiment are shown in Fig. 72. Of course,
23 other step sizes can be employed, as desired, and various numbers of
24 different sized steps can be employed.

1 The time used for the calculations for the coarse and medium
2 cases is 40 ns, a typical value for the starting period of the oscillator.
3 26.2 ns is used for the medium fine and fine cases because these steps
4 occur when the oscillator is close to its final frequency.

5 The course and medium steps are controlled by the Puf1 and
6 Puf2 outputs of the start-up circuit. More particularly, in the illustrated
7 embodiment, the course steps are controlled by the PumpUpFast output
8 of the start-up circuit "dcr_startup" shown in the detailed schematic
9 drawings, and the medium step is controlled by the PumpUpMed output
10 of the start-up circuit "dcr_startup" shown in the detailed schematic
11 drawings. The medium fine step is also controlled by the PumpUpMed
12 signal but the step size is reduced when the SDD (start data decode)
13 signal is asserted indicating the oscillator is within a few percent of its
14 final value. The fine step is controlled by the state machine and is
15 used to "close in" on the final value.

16 While this charge pump and loop filter configuration is
17 advantageous for implementation on an integrated circuit, other
18 configuration are possible. For example, simple RC filters can be
19 employed.

20 21 Details of Transmit Frequency Derivation from Incoming Data

22 The illustrated embodiment has a loop filter including capacitors
23 on respective control nodes "OUTN" and "OUTP" (shown in Figs.
24 8.0504AA-EE) of the voltage controlled oscillator "vco." In the

1 illustrated embodiment, the loop filter capacitor on the control node
2 "OUTP" is defined by a plurality of capacitors in parallel, and the loop
3 filter capacitor on the control node "OUTN" is defined by a plurality
4 of capacitors in parallel. The voltage on the respective control nodes
5 is indicative of the frequency at which the voltage controlled oscillator
6 "vco" is oscillating. After an entire incoming message has been received
7 by the receiver "rx," the control nodes and the capacitors on the control
8 nodes are isolated from driving circuitry. The control voltage is thus
9 stored in analog form on the capacitors, and the voltage controlled
10 oscillator "vco" continues to oscillate at the recovered frequency. The
11 length of time that the voltage stored on the capacitors is valid
12 depends on leakage currents that can charge or discharge the capacitors
13 over time.

14 In the illustrated embodiment, such leakage currents are minimized
15 by minimizing n+ and p+ active areas on the control node, and by
16 minimizing drain to source voltages on devices connected to the control
17 nodes. The values for the respective capacitors are chosen, in
18 conjunction with loop filter requirements, to hold the control voltages
19 for as long as possible as required before the device 12 transmits a
20 reply to the received radio frequency command. This amount of time
21 is approximately several hundred milliseconds in the illustrated
22 embodiment.

23 The output frequency of the voltage controlled oscillator can be
24 multiplied up to generate a carrier frequency for the transmitter, as

1 described elsewhere, or can be divided down to generate tones for FSK
2 (frequency shift keyed) transmission or DPSK (differential phase shift
3 keyed) transmission depending on what form of transmission is selected
4 for the transmitter "tx."

5 In one embodiment, only one control node is employed; however,
6 in the illustrated embodiment, a differential control node scheme is
7 employed involving two control nodes "OUTN" and "OUTP." Therefore,
8 in the illustrated embodiment, a capacitor is provided on each control
9 node, and control voltages are stored in analog form on these two
10 capacitors.

11 Figs. 8.0504AA-EE provide a circuit drawing of the control voltage
12 generator "dcr_vcocontrol." The control voltage generator shows the
13 control nodes for the voltage controlled oscillator. The control voltage
14 generator is a differential circuit. The control nodes are shown on the
15 right edge of Figs. 8.0504AA-EE as "OUTP" and "OUTN," where
16 "OUTN" is actually tied to the band gap voltage, which is approximately
17 1.2 Volts. "OUTP" is the node that is pumped up to adjust frequency.
18 The control voltage generator includes step size generators shown on the
19 left half of Figs. 8.0504AA-EE. The steps are achieved by conducting
20 a current to the capacitor on the control node for a prescribed length
21 of time. For a large step, a large current is applied to this capacitor.
22 For a small step, a smaller current is applied to this capacitor. The
23 capacitor on the control node "OUTP" is defined by ten capacitors in
24 parallel in the illustrated embodiment.

1 A similar capacitor, defined by ten capacitors in parallel, is
2 provided on the other control node "OUTN."

3 Four different size currents are generated by fine, medium fine,
4 medium, and coarse step generators "dcr_finestepgen,"
5 "dcr_medfinestepgen," "dcr_medstepgen," and "dcr_coarsestepgen"
6 respectively. The currents are either steered to the control capacitor
7 on the control node or away from the capacitor, depending on whether
8 there is a pump up or pump down command.

9 Figs. 8.050401AA-CK provide a circuit drawing showing construction
10 details of the coarse step generator "dcr_coarsestepgen." The coarse
11 step generator includes a plurality of current mirrors.

12 Figs. 8.050402AA-CJ provide a circuit drawing showing construction
13 details of the medium step generator "dcr_medstepgen." The medium
14 step generator includes a plurality of current mirrors.

15 Figs. 8.050403AA-BI provide a circuit drawing showing construction
16 details of the medium fine step generator "dcr_medfinestepgen." The
17 medium fine step generator includes a plurality of current mirrors.

18 Figs. 8.050404AA-BB provide a circuit drawing showing construction
19 details of a fine step controller "dcr_finestepctrl."

20 Figs. 8.050405AA-EJ provide a circuit drawing showing construction
21 details of the fine step generator "dcr_finestepgen."

22 Figs. 8.0505AA-EF provide a circuit drawing of the voltage
23 controlled oscillator "dcr_vco." The voltage controlled oscillator
24 "dcr_vco" is a four stage ring oscillator with differential stages. The

1 voltage controlled oscillator includes an OTA (operational
2 transconductance amplifier) shown on the left side of Figs.
3 8.0505AA-DE. The OTA gives a linear relationship between the voltage
4 differential at its inputs and the current at its output. The voltage
5 controlled oscillator further includes current mirrors which mirror the
6 current at the output of the OTA to drive the voltage controlled
7 oscillator to change its frequency. The previously discussed control
8 nodes ("OUTN" and "OUTP" of Figs. 8.0504AA-EE) are shown coming
9 in on the left side Figs. 8.0505AA-DE, labelled as "INN" and "INP."
10 The voltage controlled oscillator further includes, at its output, a
11 comparator type circuit that provides digital levels for the output of the
12 voltage controlled oscillator "dcr_vco."

13 Fig. 8.0506AA-AB provide a circuit drawing of a clock generator
14 "dcr_rxclkgen." Different frequencies are needed for different functions.
15 The clock generator provides outputs at different frequencies. For
16 example, the clock generator provides an output "PROCCLK" (for the
17 processor), an output "CHIPCLK" (chip clock); and outputs "PLLCLKP"
18 and "PLLCLKN" for the clock that drives the state machine. The
19 clock generator "dcr_rxclkgen" has an input "LOWRATE" for low rate
20 which is a signal indicative that the chip is in low rate and can expect
21 data to come in at a chip rate of one-half the normal chip rate. The
22 loop is adjusted in a manner such that the frequency of "FMASTER"
23 does not change regardless of whether the chip is in high rate or low
24 rate. However, the clock "CHIPCLK" for the integrated circuit 16 is

1 half as fast in low rate, and it takes twice as long to get data in as
2 it would to get the same amount of data in at the high rate.

3 Fig. 8.050601 provides a circuit drawing showing construction
4 details of a flip-flop "dcr_rxclkgenff" included in the clock generator.

5 Figs. 8.0507AA-AB provide a circuit drawing of a non-overlapping
6 clock generator "dcr_clkgen." The non-overlapping clock generator
7 receives as inputs true and compliment clock signals "ClkInP" and
8 "ClkInN" and provides buffered true and compliment clock signals
9 "ClkOut" and "ClkOutN." The non-overlapping clock generator buffers
10 the true and compliment clock signals "ClkInP" and "ClkInN" in such
11 a way that before "ClkOut" can go high, "ClkOutN" must be low, and
12 then at the end of that cycle, before "ClkOutN" can go high, "ClkOut"
13 must be low. Any overlap between the two clocks occurs when they
14 are both low. They are never both high at the same time. This is
15 quite commonly required in many circuits throughout the integrated
16 circuit 16 where shift register type techniques are used, and one stage
17 passes information to another. Non-overlapping clocks are required for
18 such functions.

19 The circuit of Figs. 6AA-EK further includes a transmitter "tx."
20 The transmitter "tx" is capable of transmitting using different modulation
21 schemes, and the modulation scheme is selectable by the interrogator.
22 More particularly, if it is desired to change the modulation scheme, the
23 interrogator sends an appropriate command via radio frequency. The
24 transmitter can switch between multiple available modulation schemes

1 such as Frequency Shift Keying (FSK), Binary Phase Shift Keying
2 (BPSK), Direct Sequence Spread Spectrum, On-Off Keying (OOK),
3 Amplitude Modulation (AM), and Modulated Backscatter (MBS).

4 The output responses are included in packets that contain, in
5 order of transmission, a preamble, a Barker code, and the reply data.

6 In one embodiment, each bit of the radio frequency reply sent by
7 the device 12 is modulated using a pseudo noise (PN) sequence for
8 direct sequence spread spectrum communication. The sequence is
9 generated in part by a linear feedback shift register "pngshr" having a
10 plurality of registers "pngsreg." In one embodiment, the linear feedback
11 shift register is in the form [5,2] which means that the input to the
12 first register is the result of combining the output of the fifth register
13 by the exclusive-OR with the output of the second register. This
14 produces thirty-one states. In one embodiment, the linear feedback shift
15 register is in the form [6,1] for a sixty-three chip sequence. In another
16 embodiment, the linear feedback shift register is in the form [8,4,3,2]
17 for a two hundred and fifty-five chip sequence. In a preferred
18 embodiment, the shift register is selectable between multiple of the
19 above forms. In the form [6,1], the input to the first of six registers
20 is the result of combining the output of the sixth register by exclusive-
21 OR with the output of the first register. In the form [8,4,3,2], the
22 input to the first of eight registers is the result of combining the
23 outputs of registers eight, four, three, and two by exclusive-OR. The
24 sixty-three chip output sequence requires less time for signal

1 synchronization than the two hundred and fifty-five chip sequence.
2 However, the two hundred and fifty-five chip output sequence provides
3 better performance in systems having poor signal to noise ratio.

4 Figs. 8.06AA-ED provide a circuit drawing of the transmitter "tx."
5 Figs. 8.06AA-ED show a transmitter PLL "txpllfsyn," a test mode data
6 selector "txdatasel," a BPSK modulation driver "txbpsk," a frequency
7 doubler "txdoubler," a second frequency doubler "txdoubler2," a
8 transmitter power amp "txpoweramp," a transmitter bias generator
9 "txbias," and a modulated backscatter transmitter "txmbs." Figs. 8.06AA-
10 ED actually shows two different transmitters. Much of Figs. 8.06AA-ED
11 illustrates circuitry employed for an active transmitter which is used in
12 accordance with an alternative embodiment of the invention, but not in
13 accordance with the preferred embodiment. Figs. 8.06AA-ED also
14 illustrate the modulated backscatter transmitter "txmbs" that is employed
15 in a preferred embodiment. The active transmitter will be discussed
16 first.

17 In embodiment where the active transmitter is employed, the
18 active transmitter operates by taking the "FMASTER" clock that was
19 recovered from the incoming data stream and using a phase locked loop
20 "txpllfsyn" (an analog phase locked loop in the illustrated embodiment)
21 to multiply up the frequency. In the illustrated embodiment, the
22 frequency is multiplied up by a factor of sixteen from 38 MHZ to 610
23 MHZ. The phase locked loop includes an oscillator that generates
24 eight phases which are 45° out of phase with respect to each other.

1 The eight phases generated by the oscillator are applied to first
2 doubler circuits "txdoubler" and "txdoubler2" in order to generate the
3 proper phased outputs at double the frequency that then again serve
4 as inputs to the other doubler circuit. The active transmitter further
5 includes a transmitter power amp "txpoweramp." The transmitter power
6 amp includes the other doubler that receives the outputs of the first
7 doubler circuits "txdoubler" and "txdoubler2." Capability for several
8 different modulation techniques is provided for the active transmitter.
9 One such modulation technique is BPSK where the phase of the carrier
10 (2.44 GHz in the illustrated embodiment) is inverted to indicate a bit
11 change. Another such modulation technique is amplitude modulation
12 (AM). In the illustrated embodiment, 100% modulation, or on/off
13 keying, is employed with the amplitude modulation.

14 Figs. 8.0601AA-BB provide a circuit drawing of the transmitter
15 phase locked loop "txpllfsyn." The phase locked loop "txpllfsyn"
16 includes a voltage controlled oscillator "txvco" that receives an analog
17 tune voltage and provides an output frequency in accordance with the
18 analog tune voltage. The phase locked loop further includes a divider
19 "txdivider" which receives the output signal of the voltage controlled
20 oscillator "txvco" and divides the frequency of the output of the
21 oscillator "txvco" by a factor of sixteen. It will be understood that this
22 division ratio of sixteen is for an exemplary embodiment, and the scope
23 of the present invention encompasses other division ratios. The phase
24 locked loop "txpllfsyn" includes a phase/frequency detector "txpfdet."

1 At the phase/frequency detector "txpfdet," the output of the divider
2 "txdivider" is compared to the signal received at the reference input of
3 the detector, which reference input, in accordance with one embodiment,
4 is the signal "FMASTER" recovered from the incoming data stream.
5 The phase/frequency detector "txpfdet" compares the fed back signal
6 (i.e., having a frequency of the voltage controlled oscillator "txvco"
7 divided by sixteen) with the signal received at the reference input and
8 puts out a pump up signal "PU" or pump down signal "PD" in
9 accordance with phase and frequency difference therebetween. The
10 phase locked loop "txpllfsyn" further includes a charge pump
11 "txchgpump." The pump up signal "PU" or pump down signal "PD"
12 put out by the phase/frequency detector "txpfdet" drive the charge pump
13 "txchgpump." The phase locked loop "txpllfsyn" further includes a loop
14 filter "txloopfilter" that receives an output signal from the charge pump
15 "txchgpump" and filters this output signal for providing the tune voltage
16 for controlling the voltage controlled oscillator "txvco." The filter
17 "txloopfilter" removes transients and establishes loop dynamics, i.e.
18 responsiveness, of the resulting phase locked loop.

19 Again, the voltage controlled oscillator provides an output signal
20 having a frequency proportional to the tune voltage received at its
21 input. When the phase locked loop is locked, the frequency and phase
22 of the signal fed back to the phase/frequency detector is equal to the
23 frequency and phase of the reference input signal. Therefore, the
24 output frequency of the voltage controlled oscillator "txvco" is equal to

1 N times the frequency of the reference signal, where N is equal to the
2 division factor of the divider. For the exemplary embodiment described
3 above, N is equal to sixteen and the output frequency of the voltage
4 controlled oscillator "txvco" is equal to sixteen times the frequency of
5 the reference signal, e.g. $16 \times 38.15 \text{ MHz} = 610.45 \text{ MHz}$. By providing
6 various output taps distributed along a ring topology of the voltage
7 controlled oscillator "txvco," output signals of different phase
8 relationships (but of equal frequency) are obtained from the voltage
9 controlled oscillator "txvco." In a preferred embodiment, eight separate
10 output taps from the voltage controlled oscillator "txvco" provide eight
11 different output signals having substantially 45° differences in phase
12 therebetween, e.g., 0° , 45° , 90° , 135° , 180° , 225° , 270° , and 315° . Thus,
13 in the illustrated embodiment, the voltage controlled oscillator "txvco"
14 generates eight phases spaced 45° .

15 Figs. 8.060101AA-BB provide a circuit drawing showing construction
16 details of the phase/frequency detector "txpfdet." The phase/frequency
17 detector puts out a pump up signal "PU" or pump down signal "PD",
18 and drives the charge pump.

19 Figs. 8.060102AA-BB provide a circuit drawing showing construction
20 details of the charge pump "txchgpump." The charge pump drives the
21 loop filter.

22 Figs. 8.060103AA-CB provide a circuit drawing showing construction
23 details of the loop filter "txloopfilter."
24

1 Figs. 8.060104AA-DC provide a circuit drawing showing
2 construction details of the transmitter voltage controlled oscillator
3 "txvco." The voltage controlled oscillator "txvco" generates eight phases
4 spaced 45°.

5
6 Details of CMOS High Frequency VCO Stage

7 The voltage controlled oscillator "txvco" comprises a ring oscillator
8 having four stages. Fig. 32 is a simplified schematic illustrating one
9 stage 104. Four such stages are connected in a chain, with the outputs
10 of the chain connected to the inputs of the chain, to define the ring
11 oscillator. The stage 104 includes a p-channel transistor 105 having a
12 gate defining a control node "V control," having a source connected to
13 a supply voltage "V+," and having a drain; and a p-channel transistor
14 106 having a gate connected to the control node "V control," having
15 a source connected to the supply voltage "V+," and having a drain.
16 The stage 104 further includes an n-channel transistor 107 having a gate
17 defining an input "IN P," a drain connected to the drain of the
18 transistor 105 and defining a node "B," and a source; and an n-channel
19 transistor 108 having a gate defining an input "IN N," a drain
20 connected to the drain of the transistor 106 and defining a node "A,"
21 and a source. The stage 104 further includes an ideal current
22 source 109 connected to the sources of the transistors 107 and 108 and
23 directing current from the sources of the transistors 107 and 108 to
24 ground. The stage 104 further includes a resistor 110 connected

1 between the voltage "V+" and the drain of the transistor 107, and a
2 resistor 111 connected between the voltage "V+" and drain of the
3 transistor 108. The stage 104 further includes a source follower 112
4 including an n-channel transistor 113 having a gate connected to the
5 node "A," having a drain connected to a supply voltage "V+," and
6 having a source defining an output "OUT P"; and an ideal current
7 source 114 connected to the source of the transistor 113 and directing
8 current from the source of the transistor 113 to ground. The stage 104
9 further includes a source follower 115 including an n-channel transistor
10 116 having a gate connected to the node "B," having a drain connected
11 to the supply voltage "V+," and having a source defining an output
12 "OUT N"; and an ideal current source 117 connected to the source of
13 the transistor 116. A source follower is a circuit where the signal at
14 the source terminal of a transistor is approximately equal to the signal
15 at the gate of the transistor. The source followers 112 and 115 are
16 provided in the stage 104 to provide the necessary drive for the outputs
17 "OUT P" and "OUT N" to drive a load. More particularly, the
18 outputs "OUT P" and "OUT N" drive amplifiers that drive frequency
19 doublers described elsewhere herein. Nodes "A" and B" are connected
20 to another stage in the chain (e.g., by connecting the nodes "A" and
21 "B" to inputs "IN P" and "IN N" of a subsequent stage).

22 The ideal current source 109 drives a current "IBIAS," and the
23 values of the resistors 110 and 111 and of "IBIAS" are chosen such
24 that transistors 107 and 108 are in saturation. More particularly, the

1 values of the resistor 110 and the current "IBIAS" are chosen such that
2 the value of the resistance of resistor 110 multiplied by the current
3 "IBIAS" is less than a maximum voltage (e.g. 800 mV) to cause
4 saturation of transistor 107. In the illustrated embodiment, resistors 110
5 and 111 have the same resistance value. The resistors 110 and 111 are
6 made from n-well, n+, p+, or polysilicon depending on the process
7 used to manufacture the integrated circuit 16. Parasitic capacitance on
8 nodes A and B is minimized by compact arrangement of the
9 components of the stage 104. Computer software, such as from
10 Cadence, can also be employed to reduce parasitic capacitance.

11 The stage 104 provides a differential amplifier capable of switching
12 at a very high frequency. The switching frequency is adjustable by
13 adjusting the voltage at control node "V control." More particularly,
14 as the voltage at the control node "V control" decreases, the p-channel
15 transistors 105 and 106 become more conductive, and there is less
16 impedance between the supply voltage "V+," and the drains of the
17 transistors 107 and 108. This provides for a faster switching rate.
18 There is a linear change in frequency versus the voltage at the control
19 node "V control" for at least some range of voltages.

20 Figs. 8.06010401AA-DC provide a circuit drawing showing
21 construction details of a stage "txvcostage" included in the transmitter
22 voltage controlled oscillator. Fig. 8.0601040101 is a layout plot showing
23 how the components of the stage 104 of Fig. 32 are laid out. More
24 particularly, Fig. 8.0601040101 actually shows four stages. Fig.

1 8.0601040101 shows locations 400 defining resistors; a line 402 providing
2 VREG (V+ of Fig. 32); locations 404 defining source followers of Fig.
3 32; a location 406 defining input "IN P" of Fig. 32; a location 408
4 defining input "IN N" of Fig. 32; locations 410 defining the n-channel
5 differential pair and the current source of Fig. 32; locations 412
6 defining the p-channel devices of Fig. 32; a line 414 providing the
7 control voltage "V control" of Fig. 32; and 915 MHZ option
8 capacitors 416.

9 Figs. 8.060105AA-DD provide a circuit drawing showing
10 construction details of the divider "txdivider."

11 Figs. 8.06010501AA-AB provide a circuit drawing showing
12 construction details of a flip-flop "txdivtff" included in the divider.

13 Figs. 8.0602AA-AB provide a circuit drawing showing construction
14 details of a test mode data selector "txdatasel."

15 Figs. 8.0603AA-AB provide a circuit drawing showing construction
16 details of a BPSK modulation driver "txbpsk."

17 18 Details of Frequency Doubler

19 Analog multipliers are known in the art. An analog multiplier
20 includes two inputs, and includes an output providing a signal that is
21 representative of a multiplication of one of the inputs with the other
22 of the inputs. One known analog multiplier is known as a Gilbert
23 multiplier cell. For a detailed discussion of Gilbert cells, see Four
24 Quadrant Multiplier, B. Gilbert, IEEE Journal of Solid State Circuits,

1 1968, pp. 365-373. Such Gilbert multiplier cells are also described in
2 detail in Analysis and Design of Analog Integrated Circuits, Paul R.
3 Gray and Robert G. Meyer, Third Edition, 1993, John Wiley & Sons,
4 Inc., pp. 667--681. Such Gilbert multiplier cells include two cross-
5 coupled, emitter-coupled pairs of bipolar junction transistors in series
6 with an emitter coupled pair of bipolar junction transistors. A Gilbert
7 multiplier cell employing bipolar junction transistors produces an output
8 that is the hyperbolic tangent of two input voltages. This is because
9 a characteristic of bipolar junction transistors is exponential non-linearity.
10 If the input voltages are sufficiently low, the hyperbolic tangent function
11 can be approximated as linear, and the circuit behaves as a multiplier
12 which multiplies together the two input voltages.

13 The multiplier cell originally developed by Gilbert employed
14 bipolar junction transistors. It is also known to employ MOS transistors
15 to produce a Gilbert multiplier cell. See, for example, Analog
16 Integrated Circuits for Communication, Principles, Simulation and Design,
17 Donald O. Pederson and Kartikeya Mayaram, Kuwer Academic
18 Publishers, Third Printing, 1994, pp. 431-433.

19 Fig. 34 illustrates a frequency doubler circuit 119 that includes a
20 Gilbert cell 120. The Gilbert cell 120 includes a pair 122 defined by
21 transistors 124 and 126. The Gilbert cell 120 further includes a pair
22 128 defined by transistors 130 and 132. The transistors 124 and 126
23 have sources that are connected together. Thus, the pair 122 is a
24

1 source coupled pair. The transistors 130 and 132 have sources that are
2 connected together. Thus, the pair 128 is a source coupled pair.

3 The transistors 126 and 130 have gates that are connected
4 together to define a first input node. The transistors 124 and 132 have
5 gates that are connected together to define a second input node. The
6 transistors 124 and 130 have drains that are connected together, and the
7 transistors 126 and 132 have drains that are connected together (shown
8 as a criss-cross pattern in Fig. 34).

9 The Gilbert cell 120 further includes another pair 134 including
10 transistors 136 and 138 having sources coupled together. Thus, the
11 pair 134 is a source coupled pair. The pair 134 is in series with the
12 pairs 122 and 128. More particularly, the transistor 136 has a drain
13 connected to the sources of the transistors 124 and 126, and the
14 transistor 138 has a drain connected to the sources of the transistors
15 130 and 132. The transistor 138 has a gate defining a third input
16 node, and the transistor 136 has a gate defining a fourth input node.

17 The Gilbert cell 120 further includes an ideal current source 140
18 driving current from the sources of the transistors 136 and 138 to
19 ground. The frequency doubler 119 further includes a resistor 142
20 connected between the drain of the transistor 124 and a voltage, and
21 a resistor 144 connected between the drain of the transistor 132 and
22 the voltage. The resistors 142 and 144 define loads for current steering
23 that produces output voltage swings.
24

1 For low amplitude signals, the Gilbert cell 120 provides an output
2 between the drain of the transistor 124 and the drain of the transistor
3 132 that is an analog multiplication of a first input signal applied
4 between the first and second input nodes, by a second input signal
5 applied between the third and fourth input nodes.

6 It is known to use a Gilbert cell to multiply together sine waves
7 of different phases to produce a doubled frequency (Figs. 34 and 35).
8 This is based on a known trigonometric relationship:

$$\sin 2\theta = 2 \sin \theta \cos \theta$$

9
10 Signals that are 180° apart are applied to the first and second input
11 nodes, and a phase shifter produces 90° shifted signals that are applied
12 to the third and fourth input nodes. However, in such embodiments,
13 an integrator is required, and the phase shifter is required to be
14 feedback controlled, because slight errors in the required 90° phase shift
15 would otherwise cause the output signals to have different average
16 values and different amplitudes as shown in Fig. 33. Fig. 33 is a
17 waveform diagram illustrating the effect of errors in frequency doubler
18 circuits that necessitates correction, such as by using an integrator and
19 feedback. Fig. 34 is a circuit schematic illustrating a frequency doubler
20 circuit that employs an integrator and feedback to solve the problem
21 illustrated in Fig. 33. Fig. 35 is a waveform diagram illustrating input
22 and output waves created and employed by a frequency doubler circuit
23 such as the one shown in Fig. 34.
24

1 It is desirable to avoid the need for feedback. Frequency
2 multiplier circuits employing feedback are susceptible to being disturbed.
3 For example, if substrate noise or an adjacent line switches and causes
4 a shift at the integrator, the output will be distorted from the desired
5 output until the integrator has a chance to recover. The integrator can
6 take a long time to recover. Therefore, it is desirable to eliminate
7 feedback loops from a frequency multiplier.

8 Fig. 36 is a circuit schematic illustrating a symmetric frequency
9 doubler circuit 146 that does not require an integrator and feedback to
10 solve the problem illustrated in Fig. 33. The frequency doubler circuit
11 of Fig. 36 creates and employs waveforms such as those shown in
12 Fig. 35.

13 The frequency doubler circuit 146 includes a first Gilbert cell 148,
14 and a second Gilbert cell 150 coupled to the first Gilbert cell 148.

15 The first Gilbert cell 148 includes a pair 152 defined by
16 transistors 154 and 156. The transistors 154 and 156 have sources that
17 are connected together. Thus, the pair 152 is a source coupled pair.
18 The Gilbert cell 148 further includes a pair 158 defined by transistors
19 160 and 162. The transistors 160 and 162 have sources that are
20 connected together. Thus, the pair 158 is a source coupled pair.

21 The transistors 156 and 160 have gates that are connected
22 together to define a first input node 163. The transistors 154 and 162
23 have gates that are connected together to define a second input node
24 165. The transistors 154 and 160 have drains that are connected

1 together, and the transistors 156 and 162 have drains that are connected
2 together (shown as a criss-cross pattern in Fig. 36).

3 The Gilbert cell 148 further includes another pair 164 including
4 transistors 166 and 168 having sources coupled together. Thus, the
5 pair 164 is a source coupled pair. The pair 164 is in series with the
6 pairs 152 and 158. More particularly, the transistor 166 has a drain
7 connected to the sources of the transistors 154 and 156, and the
8 transistor 168 has a drain connected to the sources of the
9 transistors 160 and 162. The transistor 168 has a gate defining a third
10 input node 169, and the transistor 166 has a gate defining a fourth
11 input node 171.

12 The Gilbert cell 148 further includes an ideal current source 170
13 driving current from the sources of the transistors 166 and 168 to
14 ground. The frequency doubler 146 further includes a resistor 172
15 connected between the drain of the transistor 154 and a voltage, and
16 a resistor 174 connected between the drain of the transistor 162 and
17 the voltage. The resistors 172 and 174 define loads for current steering
18 that produces output voltage swings.

19 The second Gilbert cell 150 includes a pair 182 defined by
20 transistors 184 and 186. The transistors 184 and 186 have sources that
21 are connected together. Thus, the pair 182 is a source coupled pair.
22 The Gilbert cell 150 further includes a pair 188 defined by transistors
23 190 and 192. The transistors 190 and 192 have sources that are
24 connected together. Thus, the pair 188 is a source coupled pair.

1 The transistors 186 and 190 have gates that are connected
2 together to define a first input node 193 of the second Gilbert cell
3 150. The transistors 184 and 192 have gates that are connected
4 together to define a second input node 195 of the second Gilbert
5 cell 150. The transistors 184 and 190 have drains that are connected
6 together, and the transistors 186 and 192 have drains that are connected
7 together (shown as a criss-cross pattern in Fig. 36).

8 The Gilbert cell 150 further includes another pair 194 including
9 transistors 196 and 198 having sources coupled together. Thus, the
10 pair 194 is a source coupled pair. The pair 194 is in series with the
11 pairs 182 and 188. More particularly, the transistor 196 has a drain
12 connected to the sources of the transistors 184 and 186, and the
13 transistor 198 has a drain connected to the sources of the
14 transistors 190 and 192. The transistor 198 has a gate defining a third
15 input node 199, and the transistor 196 has a gate defining a fourth
16 input node 201.

17 The Gilbert cell 150 further includes an ideal current source 200
18 driving current from the sources of the transistors 196 and 198 to
19 ground.

20 The outputs of the second Gilbert cell are connected to the
21 outputs of the first Gilbert cell. More particularly, the drain of the
22 transistor 184 is connected to the drain of the transistor 154 and the
23 drain of the transistor 192 is connected to the drain of the
24 transistor 162.

1 The first input node 193 of the second Gilbert cell 150 is
2 connected to the fourth input node 171 of the first Gilbert cell 148.
3 The third input node 199 of the second Gilbert cell 150 is connected
4 to the second input node 165 of the first Gilbert cell 148. The fourth
5 input node 201 of the second Gilbert cell 150 is connected to the first
6 input node 163 of the first Gilbert cell 148.

7 In operation, a first sinusoidal signal is applied to the second
8 input node 165 of the first Gilbert cell 148. A second sinusoidal
9 signal, 180° out of phase with the first sinusoidal signal, is applied to
10 the first input node 163 of the first Gilbert cell 148 (and to the fourth
11 input node of the second Gilbert cell 150). A third sinusoidal signal,
12 90° out of phase with the first sinusoidal signal, is applied to the
13 second input node 195 of the second Gilbert cell 150. A fourth
14 sinusoidal signal, 270° out of phase with the first sinusoidal signal, is
15 applied to the first input node of the second Gilbert cell 150. This
16 relationship of phases on the inputs to the first and second Gilbert
17 cells causes the output to be symmetrical so that the problem of
18 Fig. 33 is avoided without the need for feedback. Even with slight
19 errors in phases between the input signals, a symmetrical output is
20 produced.

21 Generally speaking, each Gilbert cell adds current from bottom
22 transistors to top transistors through the resistor loads to form output
23 voltages. In the illustrated embodiment, a phase arrangement applied
24

1 to the upper Gilbert cell is generally reversed for the bottom Gilbert
2 cell so undesirable offsets cancel each other.

3 In one embodiment, the second, third, and fourth input sinusoidal
4 signals are derived from the first input sinusoidal signal using a simple
5 four stage differential oscillator.

6 A doubled frequency is thus obtained at the outputs, which are
7 defined at the drain of the transistor 154 and the drain of the
8 transistor 162, without the need for an integrator and feedback.

9 Figs. 8.0604AA-AB provide a circuit drawing of the frequency
10 doubler "txdoubler." The frequency doubler circuit "txdoubler" includes
11 a doubler core "txfdbl" having two tiers of transistors. The two tiers
12 of transistors are shown in Figs. 8.060401AA-FE as being a top tier and
13 a bottom tier. The frequency doubler requires different levels
14 depending on whether the top tier of transistors or bottom tier of
15 transistors are driven by a particular phase. The frequency doubler
16 "txdoubler" therefore includes driver amplifiers "txfdbldrv" which provide
17 that level shifting. There is no intended phase shift introduced by the
18 driver amplifiers.

19 Figs. 8.060401AA-FE provide a circuit drawing of the frequency
20 doubler core "txfdbl." The frequency doubler core "txfdbl" includes
21 level shifting circuitry. The level shift is a little level shift, and is
22 accomplished by a resistor and capacitor shown at the top of the right
23 stack (Fig. 8.060401AD). The level shift is performed in order to
24

1 adjust output levels down in voltage because this frequency doubler core
2 drives another frequency doubler.

3 Figs. 8.0605AA-AB provide a circuit drawing of the frequency
4 doubler "txdoubler2." The frequency doubler "txdoubler2" is substantially
5 similar to the first frequency doubler "txdoubler." The main difference
6 has to do with the bias arrangements for the driver amps and for the
7 doubler core. In an alternative embodiment, the first and second
8 frequency doublers "txdoubler" and "txdoubler2" are identical.

9 Figs. 8.060501AA-CD provide a circuit drawing showing
10 construction details of the doubler driver amplifier "txfdbldrv."

11 Figs. 8.060502AA-CD provide a circuit drawing showing
12 construction details of a second doubler driver amplifier "txfdbldrv2"
13 included in the frequency doubler "txdoubler2." The second doubler
14 driver amplifier "txfdbldrv2" include a bias diode. The doubler driver
15 amplifier "txfdbldrv2" includes circuitry (the criss-cross configuration in
16 Figs. 8.060502AA-CD) where bi-phase (binary phase shift keying)
17 modulation is performed. This is where a phase can be switched from
18 one side to another by the state of two inputs "BPMODINP" and
19 "PMODINN." Thus, a phase reversal can be accomplished in this
20 circuit.

21 Figs. 8.060503AA-FE provide a circuit drawing of a frequency
22 doubler core "txfdbl2." The frequency doubler core "txfdbl2" is
23 substantially identical to the frequency doubler core "txfdbl" except for
24 the biasing transistors.

Details of Single Antenna Receiver and Active Transmitter

Fig. 50 provides a simplified circuit schematic showing the antenna 44 being shared by the active transmitter and the Schottky diode detector 84. The Schottky diode detector 84 was described above in detail in connection with Fig. 29, like reference numerals indicating like components.

The detector 84 includes a Schottky diode 86 having an anode connected to the antenna 44 and having a cathode. The detector 84 further includes an ideal current source 88 connected to the cathode of the Schottky diode 86 and driving current through the antenna and Schottky diode 86 in the direction from the anode to the cathode. The detector 84 further includes a capacitor 90 connected between the cathode of the Schottky diode 86 and ground and providing a radio frequency short to ground. The detector 84 further includes a capacitor 92 having a first terminal connected to the cathode, having a second terminal defining an output of the detector 84, providing an AC short to video frequency, and defining the output of the detector 84.

The active transmitter is described elsewhere herein, and is illustrated as a block 330 in Fig. 50.

The antenna is a loop antenna and has one end connected to a bias voltage (V_{dd}) and has another end connected to the anode of the Schottky diode 86.

1 The transmitter has an antenna output (or RF output) 332, and
2 the detector 84 has an antenna input (or RF input) 334. In the
3 illustrated embodiment, the integrated circuit 16 having the
4 transmitter 330 and detector 84 includes a contact connected to the
5 antenna output 332 and accessible from outside the IC package; and a
6 contact connected to the antenna input 334 and accessible from outside
7 the IC package. These contacts are connected together by a short
8 outside the package. This provides for flexibility in that different
9 antenna configurations are possible, separate antennas can be used for
10 the detector 84 and transmitter 330, if desired, an external amplifier can
11 be used to amplify the output of the transmitter 330, etc.

12 The detector and transmitter do not operate simultaneously.

13 In one embodiment, the integrated circuit 16 further includes a
14 pull up transistor 336 connected to the cathode of the Schottky diode
15 86 and configured to connect the cathode to the bias voltage (Vdd)
16 when the transmitter is operating. The pull up transistor 336 can be
17 included if necessary so the detector does not interfere with the
18 transmitter 330 while the transmitter 330 is transmitting.

19 By using a common antenna for the active transmitter and the
20 Schottky diode detector, space savings are achieved.

21 The active transmitter 330 is shown in greater detail in Fig. 51.
22 The active transmitter includes a differential pair 338 of transistors
23 driven by the frequency doubler. The function of the differential pair
24 338 is to steer current to the antenna 44 or away from the antenna

44. If bi-phase modulation is employed, the differential pair 338 steers one phase or the other phase to the antenna 44. More particularly, if bi-phase modulation is employed, then a signal on line "ENABLEAM" (see Figs 8.06AA-ED, and 8.0605AA-AB to 8.0608AA-BB) is low and the leftmost of three current steering transistors (sources connected to the current source) is off because its gate is low. Current is then steered to the antenna by the transistor shown on the right. Its phase is determined in an earlier stage. The other phase is present in the middle transistor. When data is reversed the current phases switch sides in response to the earlier stage. If amplitude modulation is employed, the differential pair either sends current to the antenna 44, or is sends none to provide on/off keying. More particularly, in the amplitude modulation mode, a signal on line "ENABLEAM" is high and current is steered to the antenna by the transistor shown to the right if a signal on line "AMDATA" is high, and the current is steered to Vdd (not to the antenna) if the signal on line "AMDATA" is low.

Figs. 8.0606AA-IE provide a circuit drawing of a transmitter power amplifier "txpoweramp." The transmitter power amplifier includes a frequency doubler, shown in the left half of Figs. 8.0606AA-IE. In the illustrated embodiment, the frequency doubler receives inputs at 1.22 GHz, and provides outputs at 2.44 GHz. The transmitter power amplifier includes the differential pair of transistors, shown on the right side of Figs. 8.0606AA-IE, driven by the frequency doubler. The differential pair steers current to the antenna or away from the

1 antenna, as described above. If bi-phase modulation is employed, the
2 differential pair steers one phase or the other phase to the antenna.
3 If amplitude modulation is employed, the differential pair either sends
4 current to the antenna, or it sends none to provide on/off keying.

5 Figs. 8.0607AA-JJ provide a circuit drawing of a transmitter bias
6 generator "txbias." The transmitter bias generator includes various
7 current mirrors in order to provide the proper bias currents to the
8 various blocks of the transmitter "tx."

9 10 Details of Single Antenna Receiver and Backscatter Transmitter

11 Fig. 52 provides a simplified circuit schematic showing an antenna
12 350 being shared by the backscatter transmitter and the Schottky diode
13 detector 84, in a manner similar to the antenna sharing possibility
14 described in connection with Figs. 50-51. The Schottky diode detector
15 84 was described above in detail in connection with Fig. 29, like
16 reference numerals indicating like components.

17 In the illustrated embodiment, the antenna 350 is a loop antenna
18 and has one end connected to a bias voltage (Vdd) and has another
19 end connected to the detector 84 via a detector input illustrated as
20 RXANT in Fig. 52. For antenna sharing with a backscatter transmitter,
21 capacitors 352 and 354 external of the integrated circuit 16 are
22 employed, as illustrated in Fig. 52, to isolate the antenna from the
23 backscatter antenna driver when the detector is using the antenna.

24 The detector and transmitter do not operate simultaneously.

1 By using a common antenna for the backscatter transmitter and
2 the Schottky diode detector, space savings are achieved.

3 In an alternative embodiment shown in Fig. 53, a single
4 antenna 350 is shared by the detector 94 (shown in Fig. 30 and
5 described elsewhere herein) and a backscatter transmitter. An n-channel
6 transistor 356 is provided having power electrodes connected to opposite
7 ends of the antenna, and having a control electrode connecting to
8 transmitter modulation circuitry. The control electrode is held low when
9 the antenna is being used by the receiver.

10 Figs. 8.0608AA-BB provide a circuit drawing of a modulated
11 backscatter transmitter "txmbs." The modulated backscatter transmitter
12 "txmbs" includes circuitry that creates non-overlapping drive signals. The
13 modulated backscatter transmitter "txmbs" includes primary antenna ports
14 "BS1" and "BS2." Each of these antenna ports is intended to be
15 connected to one-half of a dipole antenna having a length appropriate
16 for the transmission frequency. In the illustrated embodiment, the
17 halves of the dipole antenna have respective sizes appropriate for 2.44
18 Ghz. The halves of the dipole antenna are not included on the
19 integrated circuit 16, in the illustrated embodiment, but are instead
20 provided "off chip." Other antenna arrangements are possible.

21 The modulated backscatter transmitter "txmbs" further includes an
22 n-channel transistor marked 900 micron in Figs. 8.0608AA-BB, and two
23 n-channel pull-up transistors marked 100 micron and respectively
24 connected between a voltage vdd! and the 900 micron transistor. When

1 the gate of the transistor marked 900 micron is high, then the two
2 dipole halves are shorted together with a fairly low impedance (e.g., on
3 the order of 15 Ohms, plus any bond wire impedance that might be
4 present depending on how the device is packaged). The antenna
5 becomes substantially similar to a single half-wavelength antenna. In a
6 backscatter mode, when the two halves of the antenna are shorted
7 together, the antenna reflects a portion of the power being transmitted
8 by the interrogator. In the other state, the gate of the 900 micron
9 transistor is low. The 900 micron transistor is then off, but the two
10 100 micron transistors that pull up the voltage vdd! are on, lifting
11 antenna ports "BS1" and "BS2" both up to a voltage of vdd! minus an
12 n-channel V_t . The two antenna ports "BS1" and "BS2" are then
13 isolated from each other by an open circuit. This isolation changes the
14 radar cross-section of the dipole antenna dramatically from when the
15 two halves are shorted together. The antenna becomes substantially
16 similar to two quarter wavelength antennas. In a Backscatter mode,
17 when the two halves of the antenna are isolated, the antenna reflects
18 very little of the power transmitted by the interrogator.

19 The modulated backscatter transmitter "txmbs" further includes
20 cross-coupled circuitry shown near the middle in Figs. 8.0608AA-BB.
21 The cross-coupled circuitry is provided to make sure that both the pull
22 up transistors and the shorting device are not on at the same time.

23 The modulated backscatter transmitter "txmbs" further includes
24 another antenna port "BS3" that is intended to be used when the

1 integrated circuit 16 is packaged in the standard SOIC package. The
2 antenna port "BS3" provides another option for configuring a backscatter
3 antenna. The antenna port "BS3" supplies a one milliamp current and
4 can drive an external PIN diode that would be situated between the
5 two halves of the dipole antenna or any other suitable antenna. The
6 other side of that external PIN diode can be returned to either the
7 antenna port "BS1" or "BS2." Because PIN diodes are good shorting
8 and opening devices for backscatter applications, the transmission range
9 of a device 12 built with the integrated circuit 16 can be extended over
10 the range that is obtained using only the internal circuitry of the
11 integrated circuit 16. This is at the expense of the need for an
12 external component and an accompanying increase in cost of the device
13 12.

14 Figs. 8.07AA-BB provide a partial circuit drawing illustrating a 915
15 MHZ transmitter "tx915" that can be included instead of the active
16 transmitter described above. The transmitter "tx915" has one less stage
17 of doubling. The chip rate also changes.

18 Figs. 8.0701AA-CB provide a circuit drawing of a VCO stage
19 modified for use with the 915 MHZ transmitter "tx915" by adding
20 capacitors to the output. The modified VCO stage is manufactured by
21 making a metal mask adjustment employed in an alternative embodiment
22 of the invention.

23 Figs. 9AA-CB provide a circuit drawing of the analog processor
24 "analgproc." The analog processor "analgproc" includes a master bias

1 source "mbs," voltage regulators "vrg" and "vrgtx," a bias OK circuit
2 "biasok," an analog port current source "aportcs," an analog multiplexor
3 decoder "asl," a random number clock generator "rcg" for the pseudo
4 random number generator, a power up detector "pup," and an analog
5 to digital (A/D) converter "ada_new." The analog multiplexor decoder
6 "asl" is an address selector used, in one embodiment, to choose from
7 among various possible inputs to the analog to digital converter. The
8 power up detector "pup" puts out a master reset pulse upon power up.
9 The power up detector also puts out another pulse that lasts throughout
10 a power up cycle in which the processor performs operations
11 appropriate upon power up, the last operation being to reset the wake
12 up pulse. The random number clock generator "rcg" generates random
13 numbers for use in arbitration schemes and generates a pseudo-random
14 sequence. The master bias source "mbs" includes a band gap regulator.
15 The voltage regulators "vrg" and "vrgtx" generate supply voltages for
16 various blocks of circuitry. The bias OK circuit "biasok" determines
17 when the regulator voltage has reached a final level, and then enables
18 the circuitry that is driven by the regulator.

19 20 Details of Low Battery Detection

21 The integrated circuit 16 includes a differential I/O op-amp or
22 comparator comparing the voltage of the battery with a predetermined
23 voltage (e.g., with band gap voltage). A low battery signal is generated
24 if the voltage of the battery is less than the predetermined voltage.

1 More particularly, one of the status registers is a battery status register
2 and has a value indicating if the voltage of the battery is less than the
3 predetermined voltage. The transmitter "tx" transmits the value of this
4 battery status register via radio frequency when responding to commands
5 from the interrogator. In the illustrated embodiment, a battery voltage
6 detector is shown in Figs. 16 (and in Figs 11 and 9.010304AA-BB);
7 however, the battery voltage detector can be provided in a different
8 location of the integrated circuit 16.

9 Figs. 9.01AA-DH provide a circuit drawing of the analog to digital
10 converter "ada_new." In the illustrated embodiment, the analog to
11 digital converter is substantially disabled and is used only to provide a
12 latch circuit for reading the low battery voltage detector. In a
13 preferred embodiment, the analog to digital converter is used in
14 connection with analog sensors and to provide alarm signals when
15 thresholds are exceeded.

16 Figs. 9.0101AA-CK provide a circuit drawing showing construction
17 details of the differential I/O op-amp "dopamp" included in the analog
18 to digital converter.

19 Figs. 9.0102AA-DH provide a circuit drawing showing construction
20 details of an analog divider (divide by two) "adaprescale" included in
21 the analog to digital converter.

22 Figs. 9.0103AJ-FP provide a circuit drawing showing construction
23 details of a control PLA "adactl_new" included in the analog to digital
24 converter circuit of Figs. 9.01AA-DH.

1 Figs. 9.010301AA-CC provide a circuit drawing showing construction
2 details of a clock generator "adacgen_new" included in the control PLA.

3 Figs. 9.010302AA-AB provide a circuit drawing showing construction
4 details of a control output driver "adacdrv_new" included in the control
5 PLA.

6 Figs. 9.010303AA-AB provide a circuit drawing showing construction
7 details of a control output driver "adacdrvn_new" included in the control
8 PLA.

9 Figs. 9.010304AA-BB provide a circuit drawing showing construction
10 details of a data latch "adadlat_new" which is included in the control
11 PLA and which is presently used as part of the battery voltage
12 detector.

13 Figs. 9.0104AA-DD provide a circuit drawing showing construction
14 details of the analog bias circuit "adabias_new" included in the analog
15 to digital converter.

16 Figs. 9.02AA-DK provide a circuit drawing of a Vdd power up
17 detector "pup" included in the analog processor. The power up
18 detector puts out a master reset pulse upon power up. The power up
19 detector also puts out another pulse that extends throughout a power
20 up cycle while the processor performs a number of operation, the last
21 one of which is to reset the wake up pulse. The power up detector
22 uses a thermal voltage generator, which is a circuit such as is used for
23 the low power current controlled oscillator, described above. The
24 thermal voltage generator generates a small current. The power up

1 circuit "pup" further includes current mirrors, and a capacitor illustrated
2 near the top center of Figs. 9.02AA-DK. The current mirrors mirror
3 the small current generated by the thermal voltage generator. The
4 mirrored current holds down one side of the capacitor illustrated near
5 the top center of Figs. 9.02AA-DK. When the power supply first rises
6 from zero to its final value, whatever that might be (e.g., 3 Volts or
7 5 Volts), the capacitor couples up the bottom plate causing a signal to
8 rise on a line "PWRUP." The small mirrored current then slowly
9 discharges the bottom plate until "PWRUP" switches back low. A
10 signal from before the final inverter producing "PWRUP" goes down to
11 circuitry shown on the lower right of Figs. 9.02AA-DK. That circuitry
12 provides a hard pull down on the bottom of the capacitor to impede
13 any switching back and forth. After the "PWRUP" pulse, the circuitry
14 switches the bottom of the capacitor back down to ground much more
15 rapidly than the small mirrored currents could. The circuitry then
16 resets so that the only thing left holding the bottom of the capacitor
17 low is the small current mirrored from the thermal voltage generator.
18 The power up detector also generates another pulse on a line
19 "WAKEUP" shown on the right of Figs. 9.02AA-DK. This pulse goes
20 high at the same time as the pulse on line "PWRUP" but does not
21 come down at the same time. Instead, the pulse on the line
22 "WAKEUP" does not come down until the processor issues a wake up
23 acknowledge signal on line "WUACK." The processor does not issue
24

1 the wake up acknowledge signal until completion of running of a wake
2 up program stored in the ROM.

3 Figs. 9.03AA-BB provide a circuit drawing of a master bias source
4 "mbs" included in the analog processor. The master bias source "mbs"
5 includes a band gap reference generator "mbs_bgr" to generate bias
6 voltages for various circuits of the integrated circuit 16. The master
7 bias generator includes a temperature compensated current generator
8 "mbs_cur" that is employed in one embodiment of the invention, but is
9 disconnected in the illustrated embodiment. The master bias source
10 further includes a reference current generator "mbs_iref" that comprises
11 current mirrors to replicate a reference current (e.g., 2.5 microAmps).

12 Figs. 9.0301AA-DJ provide a circuit drawing showing construction
13 details of a band gap reference generator "mbs_bgr" included in the
14 master bias source. Band gap reference generators produce a reference
15 voltage, and are known in the art. See, for example, Analysis and
16 Design of Analog Integrated Circuits, Paul R. Gray and Robert G.
17 Meyer, John Wiley & Sons. The reference voltage produced is
18 approximately equal to the band gap voltage of silicon, which is
19 approximately 1.2 Volts. A band gap reference generator generates a
20 voltage output that is independent of power supply and temperature.

21 Figs. 9.0302AA-DI provide a circuit drawing showing construction
22 details of a temperature compensated current generator "mbs_cur"
23 included in the master bias source.
24

1 Figs. 9.0303AA-CF provide a circuit drawing of the reference
2 current generator "mbs_iref" included in the master bias source. The
3 reference current generator "mbs_iref" biases various circuits of the
4 integrated circuit 16. The reference current generator "mbs_iref"
5 includes current mirrors that replicate incoming current so that the
6 reference current generator can supply the same value current to a
7 number of different circuit blocks.

8 Figs. 9.04AA-CE provide a circuit drawing of the voltage regulator
9 "vrg" included in the analog processor. The voltage regulator includes
10 an op-amp having an input receiving a reference voltage "VREF" (which
11 is approximately 1.2 Volts). The voltage regulator further includes a
12 large p-channel device driven by the output of the op-amp. In the
13 illustrated embodiment, the p-channel device is made up of a plurality
14 of p-channel devices connected together in parallel. The voltage
15 regulator further includes an output node "VREG" driven by the
16 plurality of p-channel devices. The voltage regulator further includes
17 a resistor divider, shown along the middle of the right side of Figs.
18 9.04AA-CE, connected to the output "VREG." The resistor divider
19 includes a fifty percent point (having a voltage of half of the voltage
20 at the output node "VREG") that is fed back to another input of the
21 op-amp so that the voltage at the output node "VREG" is required to
22 be two times the input voltage "VREF" to complete the feedback. In
23 the illustrated embodiment, a number of individual regulators are
24 employed in order to isolate power supplies to different areas of the

1 circuit. However, in alternative embodiments, a reduced number of
2 voltage regulators are employed.

3 Figs. 9.05AA-FE provide a circuit drawing of the voltage regulator
4 "vrgtx" included in the analog processor. The voltage regulators "vrg"
5 and "vrgtx" generate supply voltages approximately equal to two times
6 band gap voltage (about 2.4 Volts) for various blocks of circuitry. The
7 voltage regulator "vrgtx" provides substantially the same output voltage
8 as the voltage regulator "vrg"; however, it has a bigger drive capability.
9 The voltage regulator "vrgtx" is connected to the active transmitter
10 which requires a lot of current.

11 Figs. 9.0501AA-CD provide a circuit drawing showing construction
12 details of an operational amplifier without compensation "opampnc"
13 included in the voltage regulator.

14 Figs. 9.06AA-DD provide a circuit drawing of a bias OK detector
15 "biasok" included in the analog processor. The bias OK detector puts
16 out a signal indicating that regulator voltage going to the receiver is at
17 or near full level. The bias OK detector includes a voltage detector.
18 A delay is built in so that adequate time is allowed. The bias OK
19 detector allows biases to stabilize before releasing the clock recovery
20 circuit and the wake up test logic.

21 Figs. 9.07AA-EG provide a circuit drawing showing construction
22 details of an analog port current source "aportcs" included in the analog
23 processor. The analog port current source "aportcs" provides a current
24 which can be used to bias sensors external to the integrated circuit 16.

1 The value of the current supplied by the analog port current source
2 "aportcs" is selected from several available values by a radio frequency
3 command. In the illustrated embodiment, the analog port is not
4 employed. However, in alternative embodiments, an analog port is used.

5 Figs. 9.08AA-CC provide a circuit drawing showing construction
6 details of an analog multiplexer decoder "asl" included in the analog
7 processor. The analog multiplexer decoder "asl" is an address selector.
8 More particularly, in a preferred embodiment, the analog multiplexer
9 decoder "asl" is used to choose from among various possible analog
10 inputs to the analog to digital converter.

11 The random number clock generator "rcg" for the pseudo random
12 number generator is shown in greater detail in Figs. 9.09AA-BB. The
13 random clock generator generates random numbers for use in the
14 arbitration scheme of the protocol to sort between multiple responding
15 devices 12.

16 17 Details of Low Power Pseudo Random Number Generator

18 The device includes a random clock generator "rcg" including a
19 linear feedback shift register "rcg_osc" that has a plurality of stages and
20 that generates a pseudo-random sequence. The random clock generator
21 "rcg" includes an oscillator "rcg_osc" that supplies clock signals to the
22 linear feedback shift register. The device includes a low current
23 generator, such as a thermal voltage generator, to drive the oscillator
24 that supplies clock signals to the linear feedback shift register. The

1 shift register has two modes of operation; namely, a low power mode,
2 and a high power mode. The random clock generator includes current
3 mirrors referenced to the low current generator. In the low power
4 mode, the current to each stage of the shift register is limited by the
5 current mirrors. In the high power mode, the current mirror device
6 gates are driven to full supply voltages. This allows the shift register
7 to operate at a higher frequency appropriate for shifting the random
8 number into the processor.

9 This technique is illustrated, with reference to an inverter, in a
10 simplified schematic in Fig. 37. Fig. 37 shows a circuit including series
11 connected p-type transistors 210 and 212, and series connected n-type
12 transistors 214 and 216 which are connected in series with the p-type
13 transistors 210 and 212. The transistors 210, 212, 214, and 216 are
14 connected between a positive voltage "V+" and ground. The transistor
15 210 has a gate connected to a voltage "V BIAS P" and the transistor
16 216 has a gate connected to a voltage "V BIAS N."

17 When "V BIAS N" and "V BIAS P" are controlled by a low
18 current current mirror (low power mode), the turn-on voltages of
19 transistors 210 and 216 are small and current through inverter
20 transistors 212 and 214 is limited. When "V BIAS N" is pulled to
21 "V+" and "V BIAS P" is pulled to ground, the inverter operates at
22 full speed.

23 Figs. 9.09AA-BB provide a circuit drawing showing construction
24 details of the random clock generator "rcg" included in the analog

processor. The random clock generator "rcg" includes a low power oscillator and bias generator "rcg_osc." The random clock generator "rcg" further includes the linear feedback shift register "rcg_sreg." The random clock generator "rcg" further includes a clock generator "rcg_clkgen" which generates non-overlapping versions of the clock which drives the linear feedback shift register "rcg_osc." The linear feedback shift register "rcg_osc" generates the pseudo-random sequence. The random clock generator further includes circuitry (shown below the linear feedback shift register in Figs. 9.09AA-BB) for switching between clock schemes. This circuitry includes an n-channel device and a p-channel device (shown as circles with x's through them in Figs. 9.09AA-BB) allowing connection or blocking connection between the input and the output of the devices. The alternate clock sources are state one "S1," state three "S3," and phase two "P2" from the processor clock. The shift register is operable in a high power mode and in a very low power mode. When the processor wants a random number from the shift register "rcg_osc," these clocks are used and the shift register is operated in the high power mode to shift eight bits at a time in serial fashion into the processor. A total of sixteen bits are transferred, so two transfers of eight bits each take place. At other times, the shift register is in the very low power mode and is driven by the clock generated by the low power oscillator. In this manner, the shift register "rcg_osc" sequences through its pseudo-random sequence

1 continuously in the background until the shift register is called upon to
2 provide a number.

3 Figs. 9.0901AA-CH provide a circuit drawing showing construction
4 details of the linear feedback shift register "rcg_sreg" included in the
5 random clock generator. In the illustrated embodiment, the linear
6 feedback shift register "rcg_sreg" is a [17,3] shift register having an
7 output in register seventeen. The input to the first register is the
8 exclusive-or of registers seventeen and three. The linear feedback shift
9 register "rcg_sreg" includes seventeen stages, so it produces a sequence
10 of $2^{17}-1$. Therefore, the odds of two devices 12 being at the same
11 place in the sequence are low.

12 Figs. 9.090101AA-CC provide a circuit drawing showing construction
13 details of a shift register zero bit "rcg_sregbit0" included in the linear
14 feedback shift register. This bit is different from others so that it can
15 power up in a particular state. The shift register will function to
16 deliver a sequence of pseudo-random numbers as long as all registers
17 are not allowed to go to zero. Therefore, the zero bit "rcg_sregbit0"
18 of the shift register is altered to guarantee that it will be a one on
19 power up. The shift register bit "rcg_sregbit0" shown in Figs.
20 9.090101AA-CC also includes a series of n-channel and p-channel devices
21 to limit current in the logic gates. When the random clock generator
22 is in the low power mode, the bias voltages on these series devices
23 allow only very small currents; however, when the random clock
24 generator is operating in the high power mode (when the processor is

1 shifting in a random number) then these nodes are driven to full
2 supply. A line "BIASN" will be driven to Vdd, and a line "BIASP"
3 will be driven to ground. Then the logic of the random clock
4 generator operates in a normal mode.

5 Figs. 9.090102AA-BB provide a circuit drawing showing construction
6 details of a shift register bit "rcg_sregbit" included in the linear
7 feedback shift register.

8 Figs. 9.0902AA-FL provide a circuit drawing showing construction
9 details of the low power oscillator and bias generator "rcg_osc" included
10 in the random clock generator. The low power oscillator includes a
11 thermal generator, as in previously described circuitry. The low power
12 oscillator and bias generator "rcg_osc" further includes bias voltage
13 generators shown in the middle and at the bottom in Figs. 9.0902AA-
14 FL. The bias voltage generator shown at the bottom in Figs.
15 9.0902AA-FL includes extra transistors to allow switching between high
16 and low power states.

17 Figs. 9.0903AA-CC provide a circuit drawing showing construction
18 details of a clock generator "rcg_clkgen" included in the random clock
19 generator.

20 The PN processor "pnproc" shown in Figs. 6AA-EK is the spread
21 spectrum processing circuit 40 shown in Fig. 5. The PN processor
22 "pnproc" performs spread spectrum processing. Spread spectrum
23 modulation is described elsewhere. The PN processor "pnproc" is shown
24 in greater detail in Figs. 10AA-DD.

1 The PN processor "pnproc" shown in Figs. 10AA-DD includes a
2 digital PN correlator "dcorr." The correlator receives a data stream on
3 line "RXCHIPS" that comes from the receiver. The correlator has a
4 thirty-one chip register and performs a comparison of the chip pattern
5 of the incoming data stream with the expected thirty-one chip pattern.
6 When there is a total or near match, the correlator "dcorr" puts out
7 a high signal (a one) on line "RXDATA." When there is a nearly
8 total mismatch, the correlator "dcorr" puts out a low signal (a zero) on
9 line "RXDATA." Every thirty-one chips, "RXDATA" either changes
10 state or does not change state, depending on whether the PN sequence
11 was inverted or not inverted (i.e., depending on whether a zero or one
12 was defined by the thirty-one chip sequence). The output of the
13 correlator "dcorr" on line "RXDATA" is a sequence of true, non-
14 encoded, data bits of ones and zeros.

15 The PN processor further includes a PN lock detector "pnlockdet."
16 The lock detector is a circuit that determines whether a preamble is
17 present. In the illustrated embodiment, the preamble is all zeros.
18 Therefore, the lock detector "pnlockdet" determines whether or not a
19 certain length of zeros have occurred in a row. In the illustrated
20 embodiment, the lock detector "pnlockdet" determines whether or not
21 four zeros occurred in a row. The lock detector "pnlockdet" has an
22 output that is connected to the serial input output circuit "sio" in the
23 processor, and enables the processor to look for the Barker or start
24 code.

1 The PN processor further includes a clock "pngclk." The clock
2 "pngclk" is a clock generator that is based on a clock signal
3 "CHIPCLK" produced by the digital clock and data recovery circuit
4 "dcr." The clock "pngclk" puts out non-overlapping true and
5 compliment versions of the clock and these are used to drive circuitry
6 in the PN processor.

7 The PN processor further includes a shift register "pngshr." The
8 shift register is a block of logic that can be used to generate a thirty-
9 one chip sequence, a sixty-three chip sequence, and a two hundred and
10 fifty-five chip sequence. A thirty-one chip sequence is always used for
11 receiving, but for transmitting multiple selections are available. In the
12 illustrated embodiment, the integrated circuit 16 is wired to allow a
13 selection between thirty-one and sixty-three chips. In alternative
14 embodiments, it can be wired to allow a selection between thirty-one
15 and two hundred and fifty-five chips, or between thirty-one and sixty-
16 three chips. In the receive mode, the PN sequence is not used
17 explicitly, except that the middle chip and the last chip in the sequence
18 are detected, and those signals are used by circuitry labelled "Bit Rate
19 Clock Generator" in Figs. 10AA-DI to generate a bit rate clock for the
20 transmitter and receiver. Thus, the output of this shift register "pngshr"
21 is used to generate a bit rate clock, on line "TRCLK." In the
22 transmit mode, if a modulation scheme has been selected that uses
23 spread spectrum encoding, the output of this shift register is used to
24 encode the data.

1 The PN processor further includes a differential and PN encoder
2 "dpenc." The differential encoder performs differential encoding and PN
3 encoding. The differential encoder includes an input connected to a
4 line "TXDATA." The data on line "TXDATA" is differential encoded
5 by the differential encoder, if differential encoding is selected. Both
6 polarities of differential encoding are provided for and are selected
7 depending on the desired modulation scheme. The differential and PN
8 encoder can also impress the PN code on the data "TXDATA" if this
9 is selected.

10 The PN processor further includes a PSK/FSK generator "fskgen."
11 In the illustrated embodiment, PSK (phase shift keying) is performed by
12 the PSK/FSK generator "fskgen." In an alternative embodiment, FSK
13 (frequency shift keying) is performed by the PSK/FSK generator
14 "fskgen." The generator "fskgen" has both a last chip complement
15 output "FSKLASTCHIP" and a mid chip complement output
16 "FSKMIDCHIP." These outputs are connected to the bit rate clock
17 generator and override the outputs from the PN generator shift register
18 "pngshr". The bit rate clock generator then generates the appropriate
19 bit rate clock.

20 The PN processor further includes D type flip-flops "pnddff," one
21 of which is included in the bit rate clock generator.

22 The PN processor further includes circuitry shown on the lower
23 right in Figs. 10AA-DD that provides for test modes. This circuitry
24 provides a way to bring a modulating signal for the transmitter out to

1 a digital pad "DIGTXOUT" depending on whether an enable signal is
2 placed on an enable pin "DIGTX." The enable signal on enable pin
3 "DIGTX" is also used, in connection with a signal on line
4 "ForceRXON" to force the receiver to receive in a continuous fashion.
5 The output of the receiver is routed to a line "TESTRXDATA" and
6 that signal is routed to a digital output pad (the digital pad
7 "DIGTXOUT" in the illustrated embodiment).

8 Figs. 10.01AA-DJ provide a circuit drawing showing construction
9 details of the digital PN correlator "dcorr" included in the PN processor.
10 The correlator "dcorr" includes a bias generator "dcor_bias" that
11 generates bias currents for other circuitry included in the correlator.
12 The correlator "dcorr" further includes a shift register "dcorr_sreg."
13 The shift register "dcorr_sreg" performs a chip by chip comparison
14 between the incoming data stream and the expected thirty-one chip PN
15 sequence. For each chip that agrees, the shift register "dcorr_sreg"
16 puts out a current on a line "Iagree." For each chip that is in
17 disagreement, the shift register "dcorr_sreg" puts out a current on a line
18 "Idisagree." Currents are added for each of the thirty-one chips on
19 these lines "Iagree" and "Idisagree." The PN correlator "dcorr" further
20 includes two comparator structures shown in the middle of Figs.
21 10.01AA-DJ as an upper comparator and a lower comparator. The
22 upper comparator has current biasing defining a threshold, and the
23 lower comparator has current biasing defining a threshold. When a
24 sufficient number of currents flow from the shift register "dcorr_sreg"

1 into the "Iagree" line to overcome the threshold set by the current
2 biasing in the upper comparator, a one is detected, and the circuit puts
3 out a digital one. If, on the other hand, the currents in the
4 "Idisagree" line are high enough to overcome the threshold set by the
5 current biasing in the lower comparator, a zero is detected, and the
6 circuit puts out a digital zero. In other cases, the output does not
7 change. The correlator further includes circuitry shown on the right of
8 Figs. 10.01AA-DJ that synchronizes the data stream out of the correlator
9 and into other information processing circuitry.

10 Figs. 10.0101AA-BG provide a circuit drawing showing construction
11 details of the PN correlator shift register "dcorr_sreg" included in the
12 PN correlator. The shift register "dcorr_sreg" performs a chip by chip
13 comparison between the incoming data stream and the expected thirty-
14 one chip PN sequence. For each chip that agrees, the shift register
15 "dcorr_sreg" puts out a current on a line "Iagree." For each chip that
16 is in disagreement, the shift register "dcorr_sreg" puts out a current on
17 a line "Idisagree."

18 Fig. 10.010101 provides a circuit drawing showing construction
19 details of a PN correlator bit "dcorr_bit" included in the PN correlator
20 shift register.

21 Fig. 10.01010101 provides a circuit drawing showing construction
22 details of a shift register cell "dcorr_sregbit" included in the PN
23 correlator bit.
24

1 Figs. 10.0102AA-CN provide a circuit drawing showing construction
2 details of a correlator bias generator "dcorr_bias" included in the PN
3 correlator.

4 Figs. 10.02AA-BE provide a circuit drawing showing construction
5 details of a PN lock detector "pnlockdet" included in the PN processor.
6 The PN lock detector "pnlockdet" detects the preamble by counting.
7 For example, in the illustrated embodiment, the PN lock detector
8 "pnlockdet" determines that a preamble has been received if the lock
9 detector counts four consecutive zeros in a row. If the PN lock
10 detector does not achieve the four consecutive zeros, it resets and starts
11 counting again.

12 Figs. 10.0201AA-AB provide a circuit drawing showing construction
13 details of a counter bit "lockcounterbit" included in the PN lock
14 detector.

15 Figs. 10.03AA-AB provide a circuit drawing showing construction
16 details of the PN generator clock "pngclk" included in the PN processor.
17 The PN generator clock is a non-overlapping clock generator.

18 Figs. 10.04AA-CE provide a circuit drawing showing construction
19 details of a PN generator shift register "pngshr" included in the PN
20 processor. The PN generator shift register has select lines so that
21 various sized PN sequences can be generated (e.g. thirty-one, sixty-three,
22 or two hundred and fifty-five chip sequences). The PN generator shift
23 register also includes circuitry for generating mid chip and last chip
24

1 signals "MIDCHIP" and "LASTCHIP" which are used for generating the
2 bit rate clock.

3 Fig. 10.0401 provides a circuit drawing showing construction details
4 of a PN generator shift register cell "pngsreg" included in the PN
5 processor.

6 Figs. 10.0402AA-CB provide a circuit drawing showing construction
7 details of a PN generator shift register summer "pngssum" included in
8 the PN generator shift register.

9 Fig. 10.05 is a circuit drawing showing construction details of a
10 PN controller D type flip-flop "pnddff" included in the PN processor.

11 Figs. 10.06AA-DH provide a circuit drawing showing construction
12 details of differential and PN encoder "dpenc" included in the PN
13 processor. The differential and PN encoder includes circuitry shown on
14 the left in Figs. 10.06AA-DH which performs differential encoding. The
15 circuitry encodes data such that zeros in the incoming data cause the
16 output to transition from either zero to one or one to zero, and ones
17 in the incoming data cause the output not to transition. Other forms
18 of differential encoding can be performed. For example, the circuitry
19 can encode data such that ones in the incoming data cause the output
20 to transition from either zero to one or one to zero, and zeros in the
21 incoming data cause the output not to transition. A selection of one
22 of these two forms of differential encoding is performed by placing a
23 high or low signal on a selection line "DIFFSEL." Whether or not
24 differential encoding takes place at all is also selectable. The

1 differential and PN encoder further includes circuitry shown on the right
2 in Figs. 10.06AA-DH which PN encodes the data, if spread spectrum
3 modulation is selected.

4 Figs. 10.07AA-CD provide a circuit drawing showing construction
5 details of a PSK/FSK generator "fskgen" included in the PN processor.
6 The PSK/FSK generator "fskgen" takes as its input a clock which runs
7 at the chip rate (9.538 MHz in the illustrated embodiment). The
8 PSK/FSK generator "fskgen" generates a tone for phase shift keying
9 (e.g., 596 kHz in the illustrated embodiment). The PSK/FSK generator
10 "fskgen" further includes circuitry shown at the bottom in Figs. 10.07AA-
11 CD which switches phase according to the input data. In other words,
12 this circuitry compliments ones to zeros, and zeros to ones according
13 to input data. If PSK or FSK is not selected, data passes through the
14 PSK/FSK generator unaltered.

15 Figs. 10.0701AA-AB provide a circuit drawing showing construction
16 details of a FSK counter bit "fskcbt" included in the PSK/FSK
17 generator.

18 Figs. 11AA-AB provide a circuit drawing of a battery I/O buffer
19 "batalg" included in the integrated circuit 16. In one embodiment,
20 battery voltage is compared to band gap voltage (produced by the band
21 gap reference generator) using an op-amp. In one embodiment, the
22 battery I/O buffer "batalg" is used to connect a voltage to the analog
23 to digital converter; however, in the illustrated embodiment, this function
24 is performed by a circuit "tsn." The circuit "tsn" includes an enable

1 line, and includes a resistor divider. When an enable signal is placed
2 on the enable line, the resistor divider is tapped, and the output of the
3 resistor divider goes to an op-amp for comparison with band gap
4 voltage.

5 In order to detect a low battery voltage, circuitry is provided
6 which defines what is a low voltage. The lowest possible value at
7 which an indication is given that the battery voltage is low is the value
8 at which the integrated circuit 16 begins to fail to operate properly.
9 However, in a preferred embodiment, an extra margin is provided so
10 that there is time to replace the battery or replace the device before
11 the integrated circuit 16 fails. For example, in one embodiment, the
12 margin is 0.1 Volts. The circuitry "tsn" is therefore set up with a
13 voltage divider having a tap compared to the band gap voltage. The
14 voltage divider has resistor values selected so that when battery voltage
15 is at the margin (e.g. 0.1 Volts) above the lowest possible value, the
16 tap in the voltage divider has a voltage slightly below the band gap
17 voltage (e.g., 1.2 Volts).

18 Figs. 12AA-AB provide a circuit drawing of a digital I/O pad
19 buffer "paddig" included in the integrated circuit 16. The digital I/O
20 pad buffer is both an input and output buffer. The I/O pad buffer
21 "paddig" has an input "DPAD" which is connected to a bond pad of
22 the integrated circuit 16. Data entering the pad buffer "paddig" from
23 the input "DPAD" passes through an ESD protection device "esd1" and
24 then passes on to whatever circuit for which it is an input (there are

1 many such pad buffers "paddig" in the illustrated embodiment). Data
2 to be output via the pad buffer "paddig" comes into the pad buffer
3 "paddig" via a line "DOUT" along with an enable on line "ENABLE."
4 The pad buffer "paddig" includes a static pull down device shown on
5 the far right in Figs. 12AA-AB. The pad buffer "paddig" further
6 includes n-channel and p-channel transistors shown in the right in Figs.
7 12AA-AB proximate the static pulldown device. If an enable signal is
8 present on line "ENABLE" and "DOUT" is high, the two p-channel
9 devices will turn on and pull the output pad "DPAD" high. If
10 "DOUT" is low, the two n-channel devices will turn on and pull the
11 output pad "DPAD" low. The pad buffer "paddig" further includes
12 circuitry providing for gradual pulling high or pulling low to reduce
13 transient currents. This is because a user may connect the pad to
14 drive a heavy load.

15 Fig. 13 provides a circuit drawing of a digital input pad buffer
16 "padigin" included in the integrated circuit 16. Fig. 13 shows the input
17 portion only of the pad buffer "paddig."

18 Fig. 14 provides a circuit drawing of an analog I/O pad buffer
19 "padalg" included in the integrated circuit 16. In one embodiment, the
20 analog I/O pad buffer is used to connect an external sensor to the
21 analog to digital converter.
22
23
24

Details of RF Selectable Return Link

The return link configuration logic "rlconfig" provides for user customization of operation of the transmitter "tx." Various customizations are possible. For example, the transmitter "tx" is selectable as operating in a backscatter transmit mode, or an active transmit mode in response to a command from the interrogator 26. This is shown in Figs. 21 and 22. Fig. 21 is a simplified circuit schematic illustrating a transmitter "tx" switchable between an active mode and a backscatter mode, and employing separate antennas As1 and As2 for the active mode and the backscatter mode, respectively. If the active mode is selected, the micro controller connects the antenna As1 to transmit the output of the transmitter, using switch S1. If the backscatter mode is selected, the micro controller 34 connects the antenna As2 to transmit the output of the transmitter, using switch S2. In an alternative embodiment, shown in Fig. 22, the transmitter "tx" is still switchable between an active mode and a backscatter mode, but employs the same antenna 46 for both the active mode and the backscatter mode.

If the backscatter mode is selected, the interrogator 26 sends a continuous unmodulated RF signal while the transmitter "tx" transmits a response to a command from the interrogator 26. The clock recovered from the incoming message is used to derive a subcarrier for the transmitter "tx." In the illustrated embodiment, the subcarrier for the transmitter "tx" is a square wave subcarrier. The response to the

1 interrogator is modulated onto the square wave subcarrier by the
2 device 12 using a selected modulation scheme. For example, the
3 response can be modulated onto the subcarrier using Frequency Shift
4 Keying (FSK), or Binary Phase Shift Keying (BPSK).

5 If the active transmit mode is selected, the transmitter 32 is
6 selectable as using amplitude modulation, or bi-phase (Binary Phase Shift
7 Keying) modulation. The transmitter 32 is selectable as using
8 differential coding, and/or spread spectrum coding. There are various
9 combinations of options that can be selected through the commands that
10 are sent to the integrated circuit 16 by the interrogator 26. The
11 transmitter 32 is selectable as using the thirty-one chip spread spectrum
12 sequence, or a narrow band.

13 These options provide for a wide range of possible applications
14 or uses for the integrated circuit 16, and provide for the possibility of
15 using different schemes in an application for different purposes. For
16 example, an active transmit can be selected for certain purposes, while
17 a backscatter transmit can be selected for different purposes.

18 Figs. 15AA-BC provide a circuit drawing of return link
19 configuration control logic "rlconfig." The return link configuration
20 control logic "rlconfig" has inputs "TXSEL0," "TXSEL1," and "TXSEL2."
21 The values on these inputs are defined by a radio frequency command
22 sent by the interrogator. These inputs "TXSEL0," "TXSEL1," and
23 "TXSEL2" are connected to the outputs of an output register "oreg"
24 included in the processor. The return link configuration logic takes

1 each possible combination of inputs "TXSEL0," "TXSEL1," and
2 "TXSEL2" (there are a total of $2 \times 2 \times 2 = 8$ possible combinations) and
3 asserts appropriate control signals to enable the desired return link
4 configuration. The signals being controlled by the return link
5 configuration control logic "rlconfig" are: "ENDIL" for enabling the
6 data interleaver; "PNOFF" for selecting whether or not PN encoding is
7 employed for data transmitted by the device 12; "DIFFSEL" for
8 selecting which polarity of differential encoding is used for transmitted
9 data; "DIFFON" for selecting whether or not differential encoding is
10 employed for transmitted data; and "ENFSK" for selecting FSK (or PSK
11 in an alternative embodiment) for transmitted data; "BSCAT" for
12 enabling backscatter for transmitted data; and "ENABLEAM" enables
13 amplitude modulation.

14 The integrated circuit 16 further includes a number of sensors,
15 such as sensors "batalg," "tsn," and "mag," in the embodiments where an
16 A/D converter is included in the analog processor "anlgproc." The
17 sensor "batalg" is a battery voltage detector, the sensor "tsn" is a
18 temperature sensor, and the sensor "mag" is a magnetic sensor. These
19 sensors will be connected to the A/D converter in the analog processor
20 "anlgproc" in one embodiment of the invention. In one embodiment,
21 one or more of these sensors are not included or not used.

22 Using such sensors, the device 12 can monitor things such as its
23 own battery voltage, its temperature and detect the presence of a
24 magnetic field. There are various possible uses for information sensed

1 by such sensors. For example, events can be counted so that,
2 depending on the user's application, the user can determine whether or
3 how many times a certain item was exposed to temperature above or
4 below a certain value (e.g., to determine likelihood of spoilage or
5 damage). Alternatively, the user can determine whether or how many
6 times a certain item was exposed to a magnetic field of a certain value
7 (e.g., when passing a certain location).

8 Figs. 16AA-EH provide a circuit drawing showing construction
9 details of the temperature sensor "tsn." The temperature sensor "tsn"
10 was designed to put out a voltage that is linearly proportional to
11 temperature. In the illustrated embodiment, the circuit "tsn" has been
12 reconfigured for use as a low battery voltage detector.

13 Figs. 16.01AA-DI provide a circuit drawing showing construction
14 details of an operational amplifier "opamp" included in the temperature
15 sensor "tsn."

16 Figs. 17AA-BB provide a circuit drawing of a magnetic field
17 sensor "mag." The magnetic field sensor senses magnetic fields.

18 Figs. 18AA-AB provide a circuit drawing showing a chip bypass
19 capacitor "bypcap3." The capacitor "bypcap3" is a integrated circuit
20 decoupling capacitor between Vdd and ground.

21 Fig. 19AA-EK provide a circuit drawing of a semiconductor
22 integrated circuit in accordance with an alternative embodiment of the
23 invention. The integrated circuit of Figs. 19AA-EK is similar to the
24 integrated circuit shown in Figs. 6AA-EK, like components having like

1 component names, except that the integrated circuit of Figs. 19AA-EK
2 has no ROM, and is intended to be connected to an external ROM.
3 This is useful for test purposes.

4 Figs. 20AA-DF provide a circuit drawing of a data processor
5 "dataproc_t3" to be used in the integrated circuit of Fig. 19 in place
6 of the data processor "dataproc." The data processor "dataproc_t3" has
7 an interface to external ROM.

8 Figs. 20.01AA-CB provide a circuit drawing of an interface
9 "extrom" to an external ROM.

10 Figs. 20.0101AA-BB provide a circuit drawing of external ROM
11 control logic "extromctl" included in the interface "extrom."

12 Fig. 20.0102 is a circuit drawing of an external ROM address
13 interface "extromad" included in the interface "extrom."

14 Figs. 20.0103AA-AC provide a circuit drawing of a digital I/O pad
15 buffer "paddigt3" included in the interface "extrom." The digital I/O
16 pad buffer "paddigt3" is the pad driver for the external ROM.

17 Fig. 20.0104 is a circuit drawing of an external ROM databus
18 interface "extromdb" included in the interface "extrom."

19 Figs. 6AA-EK also illustrate bonding pads "PAD AA," and "PAD
20 A," "PAD B," "PAD C," "PAD D," "PAD E," "PAD F," "PAD G," "PAD
21 H," "PAD I," "PAD J," "PAD K," "PAD L," "PAD M," "PAD N," "PAD
22 O," "PAD P," "PAD Q," "PAD R," "PAD S," "PAD T," "PAD U," "PAD
23 V," "PAD W," "PAD X," "PAD Y," and "PAD Z," which are provided
24 around the edge of the die of integrated circuit 16. In the illustrated

1 embodiment, the integrated circuit 16 includes a standard 20 lead SOIC
2 package; however, any appropriate integrated circuit package can be
3 employed.

4 Connections to these pads are brought out of the package and
5 are accessible to the user. In this way, the user can somewhat tailor
6 the function of the integrated circuit 16 to their application. In one
7 embodiment, however, the entire device 12 is encapsulated in a housing
8 such as that shown in Fig. 3.

9 The pads P and Q are digital port data and clock pads, and
10 work together to provide a serial input or output, or a digital
11 connection outside the integrated circuit. For example, if desired, data
12 can be transmitted to the integrated circuit 16 via radio frequency, and
13 a response can be put out on the digital port data pad, or vice versa.

14 The pad R is a chip enable pad, and prevents wake up to look
15 for an incoming radio frequency signal. There are some applications
16 or uses where the user knows that there will be certain periods of time
17 when no valid radio frequency signals will be presented to the
18 integrated circuit 16. The user will want to prevent the integrated
19 circuit 16 from leaving the sleep mode so that power can be saved,
20 and the life of the battery 18 can be extended.

21 The pad S is a test mode pad for testing. When the integrated
22 circuit 16 is powered on (i.e., when power is first applied), if that pad
23 is held high then the micro controller 34 goes into a self-test mode.
24 After the self-test, if the pad S is no longer held high, the integrated

1 circuit 16 goes to the sleep mode, and periodically awakens to look for
2 valid radio frequency signals, as it normally would. This pad S is
3 useful to the manufacturer of the integrated circuit 16, such as for
4 testing prior to packaging the die of the integrated circuit 16 in the
5 housing of the integrated circuit 16.

6 The pad T is a digital transmit pad, and the pad U is a digital
7 transmit data pad. These pads are useful for testing. They allow the
8 integrated circuit 16 to operate in its intended manner, except that, if
9 the pad T is held high, data from the integrated circuit 16 is brought
10 out as a digital signal on the pad U instead of being transmitted via
11 radio frequency using transmitter "tx."

12 If the pad I is held high, data to the integrated circuit 16 is
13 brought in as a digital signal on the pad H instead of being received
14 via radio frequency using receiver "rx". Details of the logic associated
15 with this function are included in the Fig. 8.01 in connection with lines
16 "DIGRX" (associated with pad I) and "DIGRXDATA" (associated with
17 pad H). This logic includes the NAND gates and invertors shown
18 leading from the lines "DIGRX" and "DIGRXDATA" to a line "DataIn."

19 These pads T, U, I, and H provide for testing of most functions
20 of the integrated circuit 16 without the need to use high frequency
21 radio signals. High frequency radio signals may not always be
22 convenient in a testing lab. The pads T and U do not provide for
23 testing of some functions relating to radio frequency transmission, and
24 the pads I and H do not provide for testing of some functions relating

1 to radio frequency reception (e.g., operation of the Schottky detector).
2 These pads T, U, V, and H do provide for testing of the spread
3 spectrum processing circuit 40, and for processing of protocol commands
4 described in the appended microfiche. This allows everything but
5 operation of radio frequency transmitter 32 and receiver 30 to be
6 checked prior to proceeding with that radio frequency testing. It also
7 provides a function for the user, in that the integrated circuit 16 does
8 not necessarily need to be used as a radio frequency identification
9 device. The integrated circuit 16 has a receiver, and a transmitter, and
10 it can be used for various purposes, such as an actuator or beacon.
11 If it is not necessary to have a radio transmission or reception of data,
12 either one or both form of data can be passed directly through the
13 pads in digital form.

14 Note that there are separate enables T and I associated with
15 transmitting or receiving digital data. For example, if the digital
16 transmit pad T is taken high, then the transmitter "tx" will not cause
17 a radio frequency signal to travel to antenna 46 but instead outgoing
18 responses will come out on the pad U. However, the receiver "rx" will
19 operate normally unless the digital receive pad I is taken high.

20 The pad V is a TX clock pad, or transmit clock pad. Pad V
21 was intended to be an external input that could be used for a clock
22 for the transmitter 32 instead of the clock recovered from the incoming
23 signal. In some applications, it may be necessary to have a clock that
24 is more stable than the recovered clock, and the pad V provides a way

1 for the user to supply such a clock. For example, the user may
2 connect a crystal oscillator, external to the integrated circuit 16, and
3 that way achieve a very stable carrier frequency for the transmitter "tx."
4 In the illustrated embodiment, pad V has been reconnected to provide
5 a signal which can be used to activate an external, high performance
6 radio.

7 The pads Y, Z, AA, A, and D are antenna pads for connecting
8 the receiver 30 and transmitter 32 to the shared antenna 14 or the
9 multiple antennas 44 and 46. In the preferred embodiment, circuitry
10 that interfaces these pads is physically located on the die next to these
11 pads. More particularly, the microwave outputs of the transmitter 32
12 are arranged on the die so as to be next to (in close physical
13 proximity to) the appropriate bond pads.

14 The pad B is a test RX or test receive pad, and the pad C is
15 a test TX or test transmit pad. Because the integrated circuit 16 is
16 usually in the sleep mode, but wakes up briefly to look for a valid
17 incoming radio frequency signal, and then goes back to sleep, it can be
18 difficult to test the receiver "rx" and the transmitter "tx." Therefore the
19 pads B and C provide for forcing on the receiver "rx" and
20 transmitter "tx," respectively, such as for testing. If a high signal is
21 applied to the pad B, this forces the receiver "rx" to remain on.
22 Similarly, if a high signal is applied to the pad C, this forces the
23 transmitter "tx" to remain on.
24

1 If the pad B is used to force the receiver on in order to
2 exercise the circuitry, such as through clock recovery, an input radio
3 frequency signal is required at the appropriate frequency (e.g., 2.45
4 GHz) modulated with the spread spectrum code.

5 The pad E is a RX input or receive input pad. This pad is
6 connected to a side of the Schottky detector where the base band
7 signal is available. This pad is provided for test purposes and to allow
8 the use of a high-performance Schottky diode external to the integrated
9 circuit 16.

10 The pad G is a VSS A pad, or analog VSS pad. The pad G
11 is a connection to a ground bus that only goes to the analog circuitry.

12 Other pads J, K, L, M, N, O, and W are voltage supply or
13 voltage drain pads (Vss or Vdd).

14 15 Protocol

16 A description of a protocol which can be employed by the
17 device 12 for the commands, replies, and status information is contained
18 in a manual titled "Micron RFID Systems Developer's Guide." This
19 manual relates to a device for use with an "AMBIT" (TM) brand
20 tracking system as well as to the device 12. Also relevant is U.S.
21 Patent No. 5,500,650 to Snodgrass et al., titled "Data Communication
22 Method Using Identification Protocol," incorporated by reference.

23 Examples of commands that can be sent from the interrogator 26
24 to the device 12 are as follow:

Identify

An Identify function is used when attempting to determine the identification of one or more of the devices 12. Each device 12 has its own identification number TagId. It is possible that the interrogator will receive a garbled reply if more than one tag responds with a reply. If replies from multiple tags are received, an arbitration scheme, discussed below, is used to isolate a single device 12.

ReadAnalogPort

In one embodiment, a ReadAnalogPort function is provided which returns the voltage (eight-bit value) of a selected analog port on a device 12.

ReadDigitalPort

A ReadDigitalPort function returns data read from a serial port of a device 12.

ReadTagMemory

A ReadTagMemory function returns data from a user accessible portion of memory included in a device 12.

ReadTagStatus

A ReadTagStatus function returns system information about a specified device 12. For example, in response to this command, the

1 device 12 will transmit a confirmation of its TagId, a tag revision
2 number, the low battery status bit, and other information.

3 4 SetAlarmMode

5 In one embodiment, a SetAlarmMode function is provided which
6 is used to determine if a set point has been exceeded on an analog
7 port of the device 12 (e.g., if a sensor senses a condition exceeding a
8 predetermined threshold). There are three alarm modes:
9 SET_HIGH_BAND_ON_ALARM, SET_LOW_BAND_ON_ALARM, and
10 SET_STATUS_REG_ON_ALARM.

11 The SET_HIGH_BAND_ON_ALARM mode sets a device 12 to a
12 low data band, and clears a bit in the device's status register indicative
13 of an alarm threshold being exceeded. When a set point (threshold)
14 is violated, the device 12 will switch from the low data band to a high
15 data band.

16 The SET_LOW_BAND_ON_ALARM mode sets a device 12 to a
17 high data band, and clears a bit in the device's status register indicative
18 of an alarm threshold being exceeded. When a set point (threshold)
19 is violated, the device 12 will switch from the high data band to the
20 low data band.

21 The SET_STATUS_REG_ON_ALARM mode does not change data
22 bands, but will result in a bit ALARM_THRESHOLD_EXCEEDED in
23 the status register being set if the set point is violated.

SetMemoryPartition

A SetMemoryPartition function defines (initializes) a block of user memory in a device 12 for memory partition. After being initialized, a partition may be used to store data using a function WriteTagMemory. Data may be read from the partition using a function ReadTagMemory. The number of partitions available on a device 12 can be determined using the ReadTagStatus function.

WriteAccessId

A WriteAccessId function is used to update an access identification AccessId for one of the memory partitions.

WriteDigitalPort

A WriteDigitalPort function is used to write data to the synchronous serial port of a device 12.

WriteTagId

A WriteTagId function is used to update the TagId of a device 12.

WriteTagMemory

A WriteTagMemory function is used to write to the user memory space UserMemory of a device 12.

WriteTagsRegs

A WriteTagsRegs function is used to update selected or all registers of a device 12 including registers TagControlReg, LswTagId, TagStoredInterrId, TimedLockoutCounter, and DormantCounter for a range of RandomValueIds. This command can be used, for example, to disable a device 12. If desired, the transmitter of a device 12 can be disabled while the receiver of that device 12 is left functional. This is accomplished using bits KILL_TAG_0 and KILL_TAG_1 in a register TagControlReg.

WriteTagRegsRandIdRange and WriteTagRegsTagIdRange

WriteTagRegsRandIdRange and WriteTagRegsTagIdRange functions are used to update registers of a group of devices 12. The WriteTagRegsTagIdRange function updates selected or all registers, including registers TagControlReg, LswTagId, TagStoredInterrid, TimedLockoutCounter, and DormantCounter, for a range of TagIds.

Examples of interrogator commands are as follows:

GetCrntAntenna

A GetCrntAntenna function returns the current antenna set used to communicate with a device 12.

1 GetCrntRetries

2 A GetCrntRetries function returns the number of times a
3 command was
4 re-transmitted during the last tag-specific command.

5
6 GetInterrStats

7 A GetInterrStats function returns record-keeping parameters if the
8 interrogator performs this function.

9
10 GetReplyStats

11 A GetReplyStats function returns values that are specific to the
12 last
13 tag-specific reply if the interrogator processes this information.

14
15 SetInterrRegs

16 A SetInterrRegs function is used to set various communication
17 parameters on an interrogator. Not all of the parameters are used on
18 all interrogators.

19
20 SetInterrTest

21 A SetInterrTest function is used during testing. This function
22 should not
23 be called in normal operation.

SetTimeouts

A SetTimeouts function is used to set the system watchdog timers.

A convenience command is described as follows:

IdentifyAll

An IdentifyAll function returns the number of devices 12 found within the system's communication range. The IdentifyAll reply parameters include the TagId and RandomValueId for each device 12 that is identified.

The sequence of steps performed by a device 12 upon receipt of an Identify command from an interrogator will now be provided, reference being made to Figs. 55-57.

Fig. 55 illustrates top level steps, held in ROM, performed by the data processor of the device 12 upon wake up (upon leaving a sleep mode 500) for any reason. The sleep mode is described above.

At step 502, a determination is made as to whether the device 12 is in a test mode. Test mode is enabled by holding a special pin high at power up time. If so, the data processor proceeds to step 504; if not, the data processor proceeds to step 506.

At step 504, a test routine is performed. The current test routine checks the Rom, RAM, processor registers, and the timed

1 lockout timer. After performing step 504, the data processor proceeds
2 to step 500 (the device 12 returns to the sleep mode).

3 At step 506, a determination is made as to whether the device
4 12 is being powered up according to the status of a signal provided by
5 a power up detector circuit. If so, the data processor proceeds to step
6 508; if not, the data processor proceeds to step 510.

7 At step 508, a power up routine is performed which initializes the
8 wakeup timer, sets up the control register, and clears the RAM. After
9 performing step 508, the data processor proceeds to step 500 (the
10 device 12 returns to the sleep mode).

11 At step 510, a determination is made as to whether a protocol
12 request has been issued. If so, the data processor proceeds to step
13 512; if not, the data processor proceeds to step 514.

14 At step 512, the data processor executes a command processing
15 routine. The command processing routine is described in greater detail
16 below, in connection with Figs. 56A-B. After performing step 512, the
17 data processor proceeds to step 500 (the device 12 returns to the sleep
18 mode).

19 At step 514, a determination is made as to whether an alarm
20 timer request has been issued. This occurs once each minute. If so,
21 the data processor proceeds to step 516; if not, the data processor
22 proceeds to step 500 (the device 12 returns to the sleep mode).

23 At step 516, the data processor performs an alarm timer routine,
24 which in one embodiment allows a selected analog input to be

1 compared against a threshold. The results of the comparison can be
2 used to set a bit and optionally cause the chip to change data bands.

3 The command processing routine 512 is illustrated in greater detail
4 in Fig. 56.

5 At step 518, high signals are placed on lines SIOENABLE and
6 RFENABLE to enable the serial input output block "sio" and to enable
7 radio frequency communications. After performing step 518, the data
8 processor proceeds to step 520.

9 At step 520, a determination is made as to whether RFDET is
10 high indicating that an RF signal is still present at the receiver input.
11 If so, the data processor proceeds to step 522; if not, the data
12 processor proceeds to step 524.

13 At step 524, the command processing routine is aborted, and the
14 device 12 returns to the sleep mode.

15 Steps 522, 526, 528, and 532 are used to determine whether a
16 first byte of a command is received within a predetermined amount of
17 time after the chip wakes up and successfully acquires the clock signal
18 from the incoming preamble.

19 At step 522, a counter is initialized according to the wakeup
20 interval selected. After performing step 522, the data processor
21 proceeds to step 526.

22 At step 526, a determination is made as to whether the counter
23 has counted down to zero. If so, the data processor proceeds to step
24 524; if not, the processor proceeds to step 528.

1 At step 528, a determination is made as to whether the first byte
2 of a valid incoming radio frequency signal has been detected. If so,
3 the processor proceeds to step 530; if not, the processor proceeds to
4 step 532.

5 At step 532, the counter is decremented. After performing step
6 532, the data processor proceeds to step 526.

7 At step 530, the data processor reads in a command string from
8 the serial input output block "sio" and stores the command string in
9 random access memory. The serial input output block "sio" controls
10 transfer of an incoming radio frequency message from the receiver to
11 the data processor. After performing step 530, the data processor
12 proceeds to step 534.

13 At step 534, the high signals on lines RFENABLE and
14 SIOENABLE are cleared. After performing step 534, the data
15 processor proceeds to step 536.

16 At step 536, the receiver is turned off in order to conserve
17 power. After performing step 536, the data processor proceeds to step
18 538.

19 At step 538, a determination is made using CRC as to whether
20 transmission occurred without errors. If so, the data processor proceeds
21 to step 540; if not, the data processor proceeds to step 524. CRC is
22 cyclic redundancy checking, a technique known in the art used to detect
23 errors in transmission of data by the affirmation of error codes by both
24

1 the sending and receiving devices. In one embodiment, a check sum
2 is used in place of a CRC.

3 At step 540, a determination is made as to whether the device
4 12 was killed by a previous command. If so, the data processor
5 proceeds to step 542; if not, the data processor proceeds to step 544.

6 At step 542, a determination is made as to whether the received
7 command is a WriteTagRegs command which can reset the kill bits in
8 the control register. If so, the data processor proceeds to step 544;
9 if not, the data processor proceeds to step 548, which is identical to
10 step 524 on the previous page of the diagram.

11 At step 544, a determination is made as to whether a valid
12 command token exists for the received command. If so, the data
13 processor proceeds to step 546; if not, the data processor proceeds to
14 step 548.

15 At step 546, a determination is made as to whether variables
16 TagID and InterrID transmitted to the device 12 correctly correspond
17 to the identification number for the particular device 12 and the
18 identification number for the interrogator with which the particular
19 device 12 is to correspond. If so, the data processor proceeds to step
20 550; if not, the data processor proceeds to step 548.

21 At step 548, the command processing routine is aborted, and the
22 device 12 returns to the sleep mode.

23 At step 550, the data processor jumps to code for the specific
24 command that was received by radio frequency. If the command is an

1 Identify command, the data processor will jump to step 552, which is
2 the start of an Identify command routine.

3 The Identify command routine is illustrated in Figs. 57A-B.

4 At step 554, a determination is made as to whether a timed
5 lockout has been set by a previously received command. If so, the
6 data processor proceeds to step 556; if not, the data processor proceeds
7 to step 558.

8 At step 556, the Identify command routine is aborted, and the
9 device 12 returns to the sleep mode.

10 At step 558, a determination is made as to whether a variable
11 "InterrID" transmitted to the device 12 correctly corresponds to the
12 identification number for the interrogator with which the particular
13 device 12 is to correspond. If so, the data processor proceeds to step
14 560; if not, the data processor proceeds to step 556.

15 At step 560, Arbitration Lockout is cleared if this is requested.
16 After performing step 560, the data processor proceeds to step 562.

17 At step 562, a new random number is obtained if this is
18 requested. After performing step 562, the data processor proceeds to
19 step 564.

20 At step 564, arbitration parameters are checked. After performing
21 step 564, the data processor proceeds to step 566.

22 At step 566, a determination is made as to whether the particular
23 device 12 should respond. If so, the data processor proceeds to step
24 568; if not, the data processor proceeds to step 556.

1 At step 568, reply parameters are assembled and stored in the
2 RAM. After performing step 568, the data processor proceeds to step
3 570.

4 At step 570, a battery status bit is updated to indicate whether
5 the battery voltage is below a threshold value. This information is
6 included in the reply to the Identify command that is sent to the
7 interrogator. After performing step 570, the data processor proceeds
8 to step 572.

9 At step 572, CRC is calculated. After performing step 572, the
10 data processor proceeds to step 574.

11 At step 574, high signals are set on lines RFENABLE and
12 SIOENABLE to enable radio frequency transmission and to enable the
13 serial input output block which transfers the data to be transmitted (i.e.,
14 the reply parameters) from the processor to the transmit circuitry.
15 After performing step 574, the data processor proceeds to step 576.

16 At step 576, the device 12 sends a preamble, consisting of 2000
17 bits of alternating pairs of ones and zeros, to the interrogator via radio
18 frequency. After performing step 576, the data processor proceeds to
19 step 578.

20 At step 578, the device 12 sends the 13 bit start code to the
21 interrogator via radio frequency. After performing step 578, the data
22 processor proceeds to step 580.

1 At step 580, the data processor sends a reply to the Identify
2 command to the interrogator via radio frequency. After performing step
3 580, the data processor proceeds to step 582.

4 At step 582, the high signals on lines RFENABLE and
5 SIOENABLE are cleared. After performing step 582, the data
6 processor proceeds to step 584.

7 At step 584, transmit mode is cleared. After performing step
8 584, the data processor proceeds to step 586.

9 At step 586, the processor pulses the Protocol Request
10 Acknowledge signal which terminates the wakeup condition that initiated
11 this entire routine. After performing step 586, the data processor
12 proceeds to step 588.

13 At step 588, the data processor returns certain control register
14 bits to their proper states in preparation for sleep mode.

15 The processor then proceeds to step 500 and returns to sleep
16 mode.

17 The sequence of steps performed by an interrogator to issue an
18 Identify command will now be provided, reference being made to Figs.
19 58-60.

20 Fig. 58 illustrates steps performed by a host processor of the
21 interrogator upon initialization. Initialization is started in step 600 by
22 calling a function.

23 At step 602, a determination is made as to whether an attempt
24 is being made to open more than a maximum number of interrogators.

1 If so, the host processor proceeds to step 604; if not, the host
2 processor proceeds to step 606.

3 At step 604, an appropriate error message is returned by setting
4 the parameter RFID ErrorNum to the appropriate value, and a null
5 value is returned to the calling function.

6 At step 606, interrogator parameters are initialized. This includes
7 initializing timeout values, interrogator types and ports. After
8 performing step 606, the host processor proceeds to step 608.

9 At step 608, a determination is made as to whether a valid
10 interrogator IO port has been selected. If so, the host processor
11 proceeds to step 612; if not, the host processor proceeds to step 610.

12 At step 610, an appropriate error message is returned. The
13 parameter RFID ErrorNum is set to the appropriate value and a null
14 is returned to the calling function.

15 At step 612, function addresses are assigned. This includes the
16 function to compute CRCs or checksums and the input and output
17 routines. After performing step 612, the host processor proceeds to
18 step 614.

19 At step 614, default communication values are assigned. This
20 includes default selections for diversity and communication retries. After
21 performing step 614, the host processor proceeds to step 616.

22 At step 616, communication hardware is reset. This initializes the
23 interrogator into a known state by resetting the hardware and clearing
24

1 the I/O FIFO's. After performing step 616, the host processor proceeds
2 to step 618.

3 At step 618, a frequency synthesizer is initialized. This function
4 programs the frequency synthesizer to the desired frequency. After
5 performing step 618, the host processor proceeds to step 620.

6 At step 620, a determination is made as to whether the frequency
7 synthesizer is programmed properly. This function is used to abort the
8 initialization process if the frequency synthesizer cannot be programmed,
9 thereby preventing subsequent communications to occur on inappropriate
10 frequencies. If so, the host processor proceeds to step 622; if not, the
11 host processor proceeds to step 624.

12 At step 622, an host memory pointer is returned that points to
13 a structure that contains the initialized parameters. After performing
14 step 622, program control is returned to the Host Application Code.

15 At step 624, an appropriate error message is returned in the
16 RFID ErrorNum parameter and a null is returned to the calling
17 function.

18 Fig. 59 illustrates an example of a software application, starting
19 at step 630, that calls the Identify function and causes the interrogator
20 to transmit an Identify command via radio frequency.

21 At step 632, the function shown and described above in
22 connection with Fig. 58 is called. After a successful call to the open
23 functions (step 632) the host computer proceeds to step 634.
24

1 At step 634, a determination is made as to whether the function
2 shown and described in connection with Fig. 58 was successfully opened.
3 If so, the system proceeds to step 638; if not, the system proceeds to
4 step 636.

5 At step 636, the host processor exits the application (or takes
6 whatever steps are appropriate within the intended application).

7 At step 637, the parameters are initialized for an Identify
8 Command.

9 At step 638, an Identify function (described below in connection
10 with Fig. 60) is called. After performing step 638, the host library
11 function proceeds to step 640.

12 At step 640, a determination is made as to whether a good reply
13 was received from the device 12. If so, the host computer proceeds
14 to step 642; if not, the host processor proceeds to step 644.

15 At step 642, reply parameters received from the device 12 are
16 printed, displayed, or otherwise used or processed. After performing
17 step 642, the host computer proceeds to step 646 where the application
18 returns results and ends.

19 At step 644, the host processor exits the application or takes
20 whatever steps are appropriate for a given application.

21 Fig. 60 illustrates the sequence of steps performed by the host
22 library function at the starting at step 650, when an Identify command
23 is issued to the device 12.
24

1 At step 654, the command buffer is packetized, using the host
2 application initialized parameters. After performing step 654, the host
3 computer proceeds to step 656.

4 At step 656, the packet CRC is computed and stored at the end
5 of the packet.

6 At step 658, the packet including the CRC is stored in an
7 interrogator transmit queue that operates in a first in, first out fashion.
8 After performing step 658, the host computer proceeds to step 659.

9 At step 659, the interrogator is commanded to output the packet
10 to the RF.

11 At step 660, a watchdog timer is set. After performing step 660,
12 the host computer proceeds to step 662.

13 At step 662, a determination is made as to whether a reply is
14 available from the device 12. If so, the host computer proceeds to
15 step 668; if not, the host computer proceeds to step 664.

16 At step 664, a determination is made as to whether the watchdog
17 timer set in step 660 has expired. If so, the host computer proceeds
18 to step 666; if not, the host computer proceeds to step 662.

19 At step 666, the host computer returns no reply and terminates
20 processing for the Identify command.

21 At step 668, CRC is checked to ensure error free transmission
22 from the device 12 to the interrogator. After performing step 668, the
23 host computer proceeds to step 670.

24

1 At step 670, the reply packet is read from the reply FIFO.
2 After performing step 670, the library routine proceeds to step 672.

3 At step 672, the reply packet is parsed into separate parameter
4 buffers. After performing step 672, the host library returns program
5 control to the host application (step 674), where processing for the
6 Identify command terminates and the host application software continues.

7 8 Details of Arbitration

9 The arbitration of multiple interrogators per device 12 is a
10 detection method based upon each interrogator using a unique
11 interrogator ID (InterrId). The InterrId is sent to a device 12 in a
12 command. The device 12 also stores an interrogator ID
13 TagStoredInterrId. The TagStoredInterrId is only updated by a
14 WriteTagRegsXXX command. A RcvdInterrId is included in replies
15 from a device 12. If a TagStoredInterrId does not match the
16 RcvdInterrId then the tag will not respond with a reply.

17 The arbitration of more than one tag per interrogator 26 is
18 accomplished by using an ArbitrationValue and an ArbitrationMask
19 during an Identify command. Contained within each device 12 is a
20 random value ID (RandomValuelD) and an arbitration lockout
21 (IDENTIFY_LOCKOUT) bit. The RandomValuelD is set to a "random"
22 binary number upon command by an interrogator. It may also be set
23 by an Identify command setting a SELECT_RANDOM_VALUE bit in
24 SubCmnd.

1 The following examples use a 1-byte ArbitrationValue for
2 simplicity. If an interrogator 26 transmits an Identify command with its
3 ArbitrationMask set to 0000 0000 (binary), all devices 12 in the
4 receiving range will respond. If there is only one device 12,
5 communications may proceed between the interrogator 26 and device 12.
6 If there are multiple devices 12 responding, the interrogator 26 will
7 detect a collision and will start the arbitration sequence. To start the
8 arbitration sequence among multiple tags, the interrogator 26 instructs
9 the tags to clear their IDENTIFY_LOCKOUT bit and (possibly)
10 re-randomize their RandomValueId values. The ArbitrationValue 0000
11 0000 and ArbitrationMask 0000 0001 are then transmitted to all
12 devices 12 in range. The devices 12 perform a logical ANDing
13 (masking) of the ArbitrationMask and the RandomValueId. If the result
14 matches the ArbitrationValue sent by the interrogator 26, the device or
15 devices 12 will reply to the Identify command. If not, the interrogator
16 26 will increment the ArbitrationValue to 0000 0001 and try again.

17 The interrogator 26 then checks each of the possible binary
18 numbers (0000 0000 and 0000 0001 in this case) in the expanded mask
19 (0000 0001) for a response by a device 12. If a single device 12
20 responds to one of these values, the interrogator 26 will reply by
21 commanding it to set its lockout bit. If any collisions are detected at
22 this mask level, the mask would be widened again by one bit, and so
23 on through the eight bit wide mask (256 numbers). If no collisions are
24 detected for a particular ArbitrationValue and ArbitrationMask

1 combination, the TagId returned in the reply is used for direct
2 communication with that particular device 12. During the arbitration
3 sequence with up to about one hundred devices 12, the mask will
4 eventually grow large enough such that all devices 12 can respond
5 without collision. After the mask widens to four or five bits, more
6 devices 12 have unique random numbers and single tag replies are
7 received. Thus with each expansion of the ArbitrationMask, there are
8 fewer and fewer tags left to Identify.

9 With a large number of tags in range, it is possible that several
10 devices 12 will choose the same value for their RandomValueId. In
11 this case, the complete mask will be used. Collisions will still occur
12 and the remaining tags will be instructed to select a new Random
13 ValueId. If an application dictates, for example, that one hundred tags
14 will usually be present in range of the interrogator 26, it would be
15 advantageous to start with the mask set to eight bit wide (11111111)
16 and count up through 256 instead of starting with the mask set at 0000
17 0000, followed by 0000 0001, 0000 0011, etc. Other arbitration schemes
18 can be implemented by the user.

19 20 Applications

21 There are a large number of possible applications for devices such
22 as the device 12. Because the device 12 includes an active
23 transponder, instead of a transponder which relies on magnetic coupling
24 for power, the device 12 has a much greater range.

1 One application for devices 12 is inventory control to determine
2 the presence of particular items within a large lot of products.

3 Another application for devices 12 is electronic article surveillance
4 (EAS). The devices 12 can be attached to retail items in a store
5 having an interrogator 26 at the exits, for detection of unauthorized
6 removal of retail items. The merchant can deactivate or remove
7 devices 12 from retail items for which proper payment has been made.

8 Another application for devices 12 is to track migration of
9 animals.

10 Another application for devices 12 is to counteract terrorism by
11 monitoring luggage entering a plane to ensure that each item of luggage
12 that enters the plane is owned by a passenger who actually boards the
13 plane. The devices 12 can also be used to monitor luggage to locate
14 lost luggage.

15 The device 12 can be use to track packages, such as courier
16 packages.

17 The device 12 can be used to track hazardous chemicals or waste
18 to ensure that it safely reaches a proper disposal site.

19 The device 12 can be used for security purposes, to track
20 personnel within a building. The device 12 can also be used for access
21 control.

22 The device 12 can be used to monitor and manage freight transit.
23 For example, interrogators 26 can be placed at the entrance and exit
24

1 of a terminal (e.g., a rail or truck terminal), to monitor incoming and
2 outgoing shipments of vehicles bearing the devices 12.

3 The device 12 can be used to impede car theft. A European
4 anti-theft directive (74/61/EEC) provides that all new car models sold
5 after January 1997 must be fitted with electronic immobilizers and
6 approved alarm systems. The devices 12 can be provided on keychains
7 or within car keys, and interrogators 26 placed in cars, so that the
8 vehicle will be inoperable unless the specified device 12 for a specific
9 car is used. The interrogator 26 can control the door locks of a car,
10 or the ignition of the car, or both. Because the device 12 includes
11 memory, the interrogator 26 in the car can periodically automatically
12 change values in the device 12 (like changing a password).

13 Devices 12 can be placed in cars and used in connection with
14 electronic toll collections systems. Because the devices 12 can be used
15 to identify the respective cars in which they are placed, interrogators
16 26 in toll plazas can charge appropriate accounts based on which cars
17 have passed the toll plaza.

18 Devices 12 can be placed in cars and used in connection with
19 parking systems. Because the devices 12 can be used to identify the
20 respective cars in which they are placed, interrogators 26 in parking
21 areas can determine when a vehicle arrives and leaves a parking area.

22 The devices 12 can be used for inventory control of rental
23 equipment.
24

1 The devices 12 can be used where bar code labels will not
2 properly work because of harsh environmental conditions (e.g., grease,
3 dirt, paint).

4 In compliance with the statute, the invention has been described
5 in language more or less specific as to structural and methodical
6 features. It is to be understood, however, that the invention is not
7 limited to the specific features shown and described, since the means
8 herein disclosed comprise preferred forms of putting the invention into
9 effect. The invention is, therefore, claimed in any of its forms or
10 modifications within the proper scope of the appended claims
11 appropriately interpreted in accordance with the doctrine of equivalents.
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CLAIMS:

1. A radio frequency identification device comprising:
a monolithic integrated circuit including a receiver, a transmitter,
and a microprocessor.

2. A radio frequency identification device in accordance with
claim 1 wherein the receiver and transmitter together define an active
transponder, and wherein the device comprises a battery supplying power
to the integrated circuit.

3. A radio frequency identification device comprising:
a monolithic integrated circuit including a receiver, a transmitter
which can operate at frequencies above 400 MHz, and a microprocessor.

4. A radio frequency identification device comprising:
a monolithic integrated circuit including a receiver, a transmitter
which can operate at frequencies above 1 GHz, and a microprocessor.

5. A radio frequency identification device comprising:
a monolithic integrated circuit including a transmitter, a
microprocessor, and a receiver which can receive and interpret signals
having frequencies above 400 MHz.

1 6. A radio frequency identification device comprising:
2 a monolithic integrated circuit including a transmitter, a
3 microprocessor, and a receiver which can receive and interpret signals
4 having frequencies above 1 GHz.

5
6 7. A radio frequency identification device comprising:
7 a monolithic integrated circuit including a receiver, a microwave
8 transmitter, and a microprocessor.

9
10 8. A radio frequency identification device in accordance with
11 claim 7 wherein the receiver and transmitter together define an active
12 transponder.

13
14 9. A radio frequency identification device in accordance with
15 claim 7 wherein the receiver is a microwave receiver.

16
17 10. A radio frequency identification device comprising:
18 a monolithic integrated circuit including a microwave receiver, a
19 transmitter, and a microprocessor.

20
21 11. A radio frequency identification device in accordance with
22 claim 10 wherein the receiver and transmitter together define an active
23 transponder.

24

1 12. A radio frequency identification device in accordance with
2 claim 10 wherein the transmitter is a microwave transmitter.

3
4 13. A radio frequency identification device comprising:
5 a single die including a receiver, a transmitter, and a
6 microprocessor, the die having a size less than 90,000 mils².

7
8 14. A radio frequency identification device in accordance with
9 claim 13 wherein the die has a size less than 300 x 300 mils².

10
11 15. A radio frequency identification device in accordance with
12 claim 13 wherein the die has a size less than 37,500 mils².

13
14 16. A radio frequency identification device in accordance with
15 claim 13 wherein the die has a size less than 250 x 150 mils².

16
17 17. A radio frequency identification device comprising:
18 a single die including a receiver, a transmitter, and a
19 microprocessor, the die having a size of substantially 209 by substantially
20 116 mils².

21
22 18. A radio frequency identification device comprising:
23 a single die integrated circuit including a receiver, a transmitter,
24 and a microprocessor.

1 19. A radio frequency identification device in accordance with
2 claim 18 wherein the receiver and transmitter together define an active
3 transponder, and wherein the device comprises a battery supplying power
4 to the integrated circuit.

5
6 20. A radio frequency identification device comprising:
7 a single die with a single metal layer including a receiver, a
8 transmitter, and a microprocessor.

9
10 21. A radio frequency identification device in accordance with
11 claim 20 wherein the receiver and transmitter together define an active
12 transponder, and wherein the device comprises a battery supplying power
13 to the integrated circuit.

14
15 22. A radio frequency identification device comprising:
16 a single die integrated circuit including a receiver, a transmitter,
17 and a microprocessor formed using a single metal layer processing
18 method.

19
20 23. A radio frequency identification device in accordance with
21 claim 22 wherein the receiver and transmitter together define an active
22 transponder, and wherein the device comprises a battery supplying power
23 to the integrated circuit.

1 24. A radio frequency identification system comprising:
2 an integrated circuit including a receiver, and a transmitter; and
3 an antenna coupled to the integrated circuit, the integrated circuit
4 being responsive to radio frequency signals of multiple carrier
5 frequencies.

6
7 25. A radio frequency identification system in accordance with
8 claim 24 wherein the receiver comprises a Schottky diode detector.

9
10 26. A radio frequency identification system in accordance with
11 claim 24 wherein the transmitter comprises a modulated backscatter
12 transmitter.

13
14 27. A radio frequency identification system in accordance with
15 claim 24 wherein the integrated circuit receives commands from an
16 interrogator transmitting a radio frequency signal including a series of
17 digital data bits modulated on a carrier, the carrier having a carrier
18 frequency, wherein the integrated circuit uses the frequency of data bits
19 modulated on the carrier but does not use the carrier frequency.
20
21
22
23
24

1 28. A radio frequency identification device comprising:
2 transponder circuitry formed in a monolithic integrated circuit
3 comprising both transmitting and receiving circuits of the transponder
4 circuitry;

5 a power supply operably associated with the transponder circuitry;
6 and

7 an antenna operably associated with the transponder circuitry.
8

9 29. A radio frequency identification device comprising:
10 a monolithic semiconductor integrated circuit including a receiver
11 and a transmitter;

12 means for applying a supply of power to the integrated circuit
13 device from a battery; and

14 means for configuring the integrated circuit to receive and transmit
15 radio frequency signals.
16

17 30. A method for producing a radio frequency identification
18 device (RFID), the method comprising the following steps:

19 providing a monolithic integrated circuit having a receiver and a
20 transmitter; and

21 providing a package configured to carry the integrated circuit.
22
23
24

1 31. A method in accordance with claim 30, the configuring step
2 including providing an antenna coupled with the integrated circuit and
3 configurable to enable at least one of signal transmitting and signal
4 receiving.

5
6 32. A method for adapting a radio frequency data
7 communication device for use at a desired carrier frequency for use in
8 a radio frequency identification (RFID) device, the method comprising
9 the following steps:

10 providing an integrated circuit having tunable circuitry, the
11 integrated circuit comprising a receiver and a transmitter;

12 configuring the integrated circuit for connection with a power
13 supply to enable operation;

14 configuring the integrated circuit to receive and apply radio
15 frequency signals via an antenna, the antenna and the tunable circuitry
16 cooperating in operation there between; and

17 tuning the tunable circuitry and the antenna to realize a desired
18 carrier frequency from a wide range of possible carrier frequencies.

1 33. A method for adapting a radio frequency data
2 communication device for use at a desired carrier frequency for use in
3 a radio frequency identification (RFID) device, the method comprising
4 the following steps:

5 providing an integrated circuit having tunable circuitry, the
6 integrated circuit comprising a receiver and a transmitter;

7 configuring the integrated circuit for connection with a power
8 supply to enable operation;

9 configuring the integrated circuit to receive and apply radio
10 frequency signals via an antenna, the antenna and the tunable circuitry
11 cooperating in operation there between; and

12 tuning the antenna to realize a desired carrier frequency from a
13 wide range of possible carrier frequencies.

14
15 34. A radio frequency communications device comprising:

16 an integrated circuit including a transmitter and a receiver, the
17 integrated circuit including a clock recovery circuit recovering a clock
18 frequency from a signal received by the receiver, the clock recovery
19 circuit having a phase lock loop including a voltage controlled oscillator,
20 and a loop filter having a capacitor storing a voltage indicative of a
21 frequency at which the voltage controlled oscillator is oscillating, the
22 integrated circuit using the voltage stored on the capacitor to generate
23 a clock frequency for the transmitter.

1 35. A radio frequency communications device in accordance with
2 claim 34 and further comprising circuitry using the voltage stored on the
3 capacitor to produce a clock signal for generating a transmitter carrier
4 frequency.

5
6 36. A radio frequency communications device in accordance with
7 claim 34 wherein the transmitter transmits using differential phase shift
8 keying, and further comprising circuitry using the voltage stored on the
9 capacitor to produce a clock signal, and divider circuitry dividing the
10 clock frequency to generate tones for differential phase shift keyed
11 transmission.

1 37. A method of recovering a clock frequency from a received
2 radio frequency signal, storing the clock frequency, and using the clock
3 frequency for radio frequency transmission by a transmitter, the method
4 comprising:

5 providing a clock recovery circuit recovering a clock frequency
6 from a signal received by the receiver, the clock recovery circuit having
7 a phase lock loop including a voltage controlled oscillator, and a loop
8 filter having a capacitor;

9 using the clock recovery circuit to recover a clock frequency from
10 a received radio frequency signal;

11 storing on the capacitor a voltage indicative of frequency at which
12 the voltage controlled oscillator is oscillating;

13 using the voltage stored on the capacitor to generate a clock
14 frequency for use by the transmitter.

15
16 38. A method in accordance with claim 37 and further
17 comprising the step using the voltage stored on the capacitor to
18 produce a clock signal for generating a transmitter carrier frequency.

19
20 39. A method in accordance with claim 37 and further
21 comprising the step of using the voltage stored on the capacitor to
22 produce a clock signal for generating tones for frequency shift keyed
23 transmission.
24

1 40. A method in accordance with claim 37 and further
2 comprising the step of dividing the recovered clock frequency for
3 generating tones for differential phase shift keyed transmission.
4

5
6 41. A method of recovering and storing a clock frequency from
7 a received radio frequency signal in a radio frequency identification
8 device including a transmitter and a receiver, the method comprising:

9 providing a clock recovery circuit recovering a clock frequency
10 from a signal received by the receiver, the clock recovery circuit having
11 a phase lock loop;

12 using the clock recovery circuit to recover a clock frequency from
13 a received radio frequency signal;

14 storing in analog form a value indicative of frequency at which
15 the voltage controlled oscillator is oscillating;

16 using the analog value to generate a clock frequency for use by
17 the transmitter.
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1 42. A radio frequency communications device comprising:
2 an integrated circuit including a transmitter and a receiver, the
3 transmitter being switchable between a backscatter mode, wherein a
4 carrier for the transmitter is derived from a carrier received from an
5 interrogator spaced apart from the radio frequency communications
6 device, and an active mode, wherein a carrier for the transmitter is
7 generated by the integrated circuit itself.
8

9 43. A radio frequency communications device in accordance with
10 claim 42 wherein the transmitter switches between the backscatter and
11 active modes in response to a radio frequency command received by the
12 receiver.
13

14 44. A radio frequency communications device comprising:
15 an integrated circuit including a transmitter and a receiver, the
16 transmitter selectively transmitting a signal using a modulation scheme,
17 the transmitter being switchable for transmission using different
18 modulation schemes.
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1 45. A radio frequency communications device in accordance with
2 claim 44 wherein the transmitter is switchable between at least two
3 modulation schemes selected from the group consisting of Frequency
4 Shift Keying (FSK), Binary Phase Shift Keying (BPSK), Direct Sequence
5 Spread Spectrum, On-Off Keying (OOK), Amplitude Modulation (AM),
6 and Modulated Backscatter (MBS).

7
8 46. A method for adapting modulation schemes of a radio
9 frequency data communication device in a radio frequency identification
10 (RFID) device, the method comprising the following steps:

11 providing an integrated circuit having switching circuitry, a receiver,
12 a transmitter, and a processor; the integrated circuit having a plurality
13 of transmitting circuits including a first transmitting circuit configured
14 to realize an active transmitter scheme and a second transmitting circuit
15 configured to realize a modulated backscatter scheme;

16 configuring the integrated circuit for connection with a power
17 supply to enable operation;

18 configuring the integrated circuit to receive and apply radio
19 frequency signals via an antenna, the antenna and the tunable circuitry
20 cooperating in operation; and

21 switching the switchable circuitry with respect to the antenna to
22 enable one of the transmitting circuits to realize one of the modulation
23 schemes.

1 47. A method for adapting modulation schemes of a radio
2 frequency data communication device in a radio frequency identification
3 (RFID) device, the method comprising the following steps:

4 providing an integrated circuit having switching circuitry, a receiver,
5 a transmitter, and a processor, the integrated circuit including a plurality
6 of transmitting circuits, the plurality of transmitting circuits configured
7 to selectively realize a plurality of modulated backscatter schemes;

8 configuring the integrated circuit for connection with a power
9 supply to enable operation;

10 configuring the integrated circuit to receive and apply radio
11 frequency signals via an antenna, the antenna and the tunable circuitry
12 cooperating in operation; and

13 switching the transmitting circuits with respect to the antenna to
14 enable one of the transmitting circuits to realize one of the modulation
15 schemes.

16
17 48. A radio frequency identification device comprising:

18 an integrated circuit including a transmitter and a receiver, the
19 integrated circuit being adapted to be connected to a battery, and
20 further including a comparator comparing the voltage of the battery with
21 a predetermined voltage and generating a low battery signal if the
22 voltage of the battery is less than the predetermined voltage.

1 49. A radio frequency identification device in accordance with
2 claim 48 wherein the integrated circuit further comprises a band gap
3 voltage generator which generates a reference voltage, and wherein the
4 predetermined voltage is the reference voltage produced by the band
5 gap voltage generator.

6
7 50. A radio frequency identification device in accordance with
8 claim 48 wherein the integrated circuit responds to commands received
9 by the receiver from an interrogator, wherein the integrated circuit
10 comprises a status register having a value indicating whether battery
11 voltage is less than the predetermined voltage and wherein the
12 transmitter transmits the value of the status register in response to a
13 command received by the receiver.

14
15 51. A radio frequency identification device in accordance with
16 claim 48 wherein the transmitter selectively transmits the low battery
17 signal using a radio frequency signal.

1 52. A method for detecting a low battery condition in a radio
2 frequency data communication device for use in a radio frequency
3 identification (RFID) device, the method comprising the following steps:

4 providing an integrated circuit having switching circuitry, a receiver,
5 and a transmitter, the integrated circuit including a comparator
6 configured to compare the battery voltage with a predetermined voltage
7 and generate a low battery signal if the battery voltage is less than the
8 predetermined voltage;

9 configuring the integrated circuit for connection with the battery
10 to enable operation;

11 configuring the integrated circuit to receive and apply radio
12 frequency signals via an antenna, the antenna and the tunable circuitry
13 cooperating in operation there between;

14 determining a predetermined voltage for the battery;

15 comparing the voltage of the battery with the predetermined
16 voltage; and

17 generating a low battery signal if the voltage of the battery is
18 less than the predetermined voltage.

1 53. A radio frequency communications device comprising:
2 an integrated circuit including a transmitter and a receiver, the
3 integrated circuit periodically checking if a radio frequency signal is
4 being received by the receiver, the integrated circuit further including
5 a timer setting a time period for the checking, the timer having a
6 frequency lock loop.

7
8 54. A radio frequency communications device in accordance with
9 claim 53 wherein the frequency lock loop comprises a current controlled
10 oscillator.

11
12 55. A radio frequency communications device in accordance with
13 claim 53 wherein the integrated circuit is configured to recover a clock
14 frequency from the received signal and wherein the transmitter is
15 configured to use the recovered clock frequency.

16
17 56. A radio frequency communications device in accordance with
18 claim 53 wherein the integrated circuit switches between a sleep mode,
19 and a higher power mode in which more power is consumed than in
20 the sleep mode.

1 57. A radio frequency communications device in accordance with
2 claim 53 and further comprising a variable value divider connected to
3 the output of the frequency lock loop, the value of the divider being
4 programmable in response to a radio frequency signal received by the
5 receiver so as to program the time period of the checking.

6
7 58. A radio frequency communications device in accordance with
8 claim 53 wherein the device is configured to receive and process
9 commands from an interrogator transmitting a radio frequency signal and
10 to enable the frequency lock loop only during processing of a command,
11 to calibrate the timer to a clock frequency recovered from a received
12 command.

13
14 59. A radio frequency communications device comprising:
15 an integrated circuit including a transmitter and a receiver, the
16 integrated circuit being configured to periodically check if a radio
17 frequency signal is being received by the receiver, the integrated circuit
18 further including a timer setting a time period for the checking, the
19 timer having a phase lock loop.

20
21 60. A radio frequency communications device in accordance with
22 claim 59 wherein a clock frequency is recovered from the received
23 signal and used by the transmitter.
24

1 61. A radio frequency communications device in accordance with
2 claim 59 wherein the phase lock loop comprises a current controlled
3 oscillator.

4
5 62. A radio frequency communications device in accordance with
6 claim 59 wherein the integrated circuit switches between a sleep mode,
7 and a higher power mode in which more power is consumed than in
8 the sleep mode.

9
10 63. A radio frequency communications device in accordance with
11 claim 59 and further comprising a variable value divider connected to
12 the output of the phase lock loop, the value of the divider being
13 programmable in response to a radio frequency signal received by the
14 receiver so as to program the time period for the checking.

15
16 64. A radio frequency communications device in accordance with
17 claim 59 wherein the device receives and processes commands from an
18 interrogator transmitting a radio frequency signal, and wherein the phase
19 lock loop is enabled only during processing of a command, to calibrate
20 the timer to a clock frequency recovered from a received command.

1 65. A method for calibrating a clock in a radio frequency data
2 communication device for use in a radio frequency identification (RFID)
3 device, the method comprising the following steps:

4 providing an integrated circuit having a receiver and a transmitter,
5 the integrated circuit including a timer having a frequency lock loop
6 configured to set a time period for periodically checking if a radio
7 frequency signal is being received by the receiver;

8 configuring the integrated circuit for connection with a battery to
9 enable operation;

10 configuring the integrated circuit to receive and apply radio
11 frequency signals via an antenna, the antenna and the integrated circuit
12 cooperating in operation therebetween; and

13 periodically checking whether a radio frequency signal is being
14 received by the receiver.

15
16 66. A radio frequency identification device for receiving and
17 responding to radio frequency commands from an interrogator
18 transmitting a radio frequency signal, the device comprising:

19 an integrated circuit including a receiver, a transmitter, and a
20 connection pin, the integrated circuit being switchable between a radio
21 frequency receive mode wherein the receiver receives commands via
22 radio frequency, and a direct receive mode wherein commands are
23 received via the connection pin.

1 67. A radio frequency identification device in accordance with
2 claim 66 wherein the connection pin is a serial input pin.
3

4 68. A radio frequency identification device in accordance with
5 claim 66 and further comprising a selection pin, and wherein the
6 integrated circuit switches between the radio frequency receive mode and
7 the direct receive mode in response to a signal applied to the selection
8 pin.
9

10 69. A radio frequency identification device for receiving and
11 responding to radio frequency commands from an interrogator
12 transmitting a radio frequency signal, the device comprising:

13 an integrated circuit including a receiver, a transmitter, and a
14 digital input pin, the integrated circuit being switchable between a radio
15 frequency receive mode wherein the receiver receives commands via
16 radio frequency, and a direct receive mode wherein commands are
17 received digitally via the digital input pin.
18

19 70. A radio frequency identification device in accordance with
20 claim 69 wherein the digital input pin is a serial input pin.
21
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1 71. A radio frequency identification device in accordance with
2 claim 69 and further comprising a selection pin, and wherein the
3 integrated circuit switches between the radio frequency receive mode and
4 the direct receive mode in response to a signal applied to the selection
5 pin.

6
7 72. A radio frequency identification device for receiving
8 and responding to radio frequency commands from an interrogator
9 transmitting a radio frequency signal, the device comprising:

10 an integrated circuit including a receiver, a transmitter, and a
11 connection pin, the integrated circuit being switchable between a radio
12 frequency receive mode wherein the receiver receives commands via
13 radio frequency, and a direct receive mode wherein a modulation signal
14 without a carrier is received via the connection pin.

15
16 73. A radio frequency identification device in accordance with
17 claim 72 wherein the connection pin is a serial input pin.

18
19 74. A radio frequency identification device in accordance with
20 claim 72 and further comprising a selection pin, and wherein the
21 integrated circuit switches between the radio frequency receive mode and
22 the direct receive mode in response to a signal applied to the selection
23 pin.

1 75. A radio frequency identification device for receiving and
2 responding to radio frequency commands from an interrogator
3 transmitting a radio frequency signal, the device comprising:

4 an integrated circuit including a receiver, a transmitter, and a
5 connection pin, the integrated circuit being switchable between a radio
6 frequency transmit mode wherein the receiver transmits responses to the
7 commands via radio frequency, and a direct transmit mode wherein
8 responses are transmitted via the connection pin.

9
10 76. A radio frequency identification device in accordance with
11 claim 75 wherein the connection pin is a serial output pin.

12
13 77. A radio frequency identification device in accordance with
14 claim 75 and further comprising a selection pin, and wherein the
15 integrated circuit switches between the radio frequency transmit mode
16 and the direct transmit mode in response to a signal applied to the
17 selection pin.

1 78. A radio frequency identification device for receiving and
2 responding to radio frequency commands from an interrogator
3 transmitting a radio frequency signal, the device comprising:

4 an integrated circuit including a receiver, a transmitter, and a
5 digital output pin, the integrated circuit being switchable between a
6 radio frequency transmit mode wherein the receiver transmits responses
7 to the commands via radio frequency, and a direct transmit mode
8 wherein responses are transmitted digitally via the digital output pin.

9
10 79. A radio frequency identification device in accordance with
11 claim 78 wherein the connection pin is a serial output pin.

12
13 80. A radio frequency identification device in accordance with
14 claim 78 and further comprising a selection pin, and wherein the
15 integrated circuit switches between the radio frequency transmit mode
16 and the direct transmit mode in response to a signal applied to the
17 selection pin.

1 81. A radio frequency identification device for receiving and
2 responding to radio frequency commands from an interrogator
3 transmitting a radio frequency signal, the device comprising:

4 an integrated circuit including a receiver, a transmitter, and a
5 connection pin, the integrated circuit being switchable between a radio
6 frequency transmit mode wherein the receiver transmits responses to the
7 commands via radio frequency, and a direct transmit mode wherein a
8 modulation signal without a carrier is transmitted via the connection pin.

9
10 82. A radio frequency identification device in accordance with
11 claim 81 wherein the connection pin is a serial output pin.

12
13 83. A radio frequency identification device in accordance with
14 claim 81 and further comprising a selection pin, and wherein the
15 integrated circuit switches between the radio frequency transmit mode
16 and the direct transmit mode in response to a signal applied to the
17 selection pin.

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84. A method comprising the following steps:

providing an integrated circuit having a receiver, a transmitter, and a connection pin, the integrated circuit including a switchable circuit configured to switch between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein commands are received via the connection pin;

configuring the integrated circuit for connection with a battery;

configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and

switching to one of the radio frequency receive mode and the direct receive mode to enable receipt of radio frequency commands or commands received via the connection pin.

1 85. A method comprising the following steps:

2 providing an integrated circuit having a receiver, a transmitter, and
3 a connection pin, the integrated circuit including a switchable circuit
4 configured to switch between a radio frequency transmit mode wherein
5 the transmitter transmits information via radio frequency, and a direct
6 transmit mode wherein data is transmitted via the connection pin;

7 configuring the integrated circuit for connection with a battery;

8 configuring the integrated circuit to receive and transmit radio
9 frequency signals via an antenna, the antenna and the integrated circuit
10 cooperating in operation; and

11 switching to one of the radio frequency transmit mode and the
12 direct transmit mode to enable transmission of information via radio
13 frequency or via the connection pin.

14
15 86. An integrated circuit comprising:

16 a radio frequency receiver;

17 a unique, non-alterable indicia identifying the integrated circuit;

18 and

19 a radio frequency transmitter configured to transmit a signal
20 representative of the indicia in response to a command received by the
21 receiver.

1 87. An integrated circuit in accordance with claim 86 and
2 further comprising an antenna coupled to the integrated circuit, a
3 battery coupled to the integrated circuit and powering the integrated
4 circuit, and a tag housing encapsulating the integrated circuit, battery,
5 and antenna.

6
7 88. An integrated circuit in accordance with claim 86 wherein
8 the integrated circuit comprises a programmable read only memory, and
9 wherein the non-alterable indicia is burned into the programmable read
10 only memory.

11
12 89. An integrated circuit in accordance with claim 86 wherein
13 the non-alterable indicia comprises laser blown polysilicon links.

14
15 90. An integrated circuit in accordance with claim 86 wherein
16 the integrated circuit comprises an EEPROM containing the non-alterable
17 indicia.

18
19 91. An integrated circuit in accordance with claim 86 wherein
20 the integrated circuit comprises a flash ROM containing the non-
21 alterable indicia.

1 92. A radio frequency identification device comprising:
2 an integrated circuit including a receiver for receiving radio
3 frequency commands from an interrogation device, and a transmitter for
4 transmitting a signal identifying the device to the interrogator, the
5 transmitter and receiver being formed on a die having a lot number,
6 wafer number, and die number, the integrated circuit including non-
7 alterable indicia identifying the lot number, wafer number, and die
8 number, the transmitter being configured to transmit the non-alterable
9 indicia in response to a manufacturer's command received by the
10 receiver, the transmitted non-alterable indicia being different from the
11 identifying signal.

12
13 93. A radio frequency identification device in accordance with
14 claim 92 wherein the integrated circuit comprises a programmable read
15 only memory, and wherein the non-alterable indicia is burned into the
16 programmable read only memory.

17
18 94. An integrated circuit in accordance with claim 92 wherein
19 the non-alterable indicia comprises laser blown polysilicon links.

20
21 95. An integrated circuit in accordance with claim 92 wherein
22 the integrated circuit comprises an EEPROM containing the non-alterable
23 indicia.
24

1 96. An integrated circuit in accordance with claim 92 wherein
2 the integrated circuit comprises a flash ROM containing the non-
3 alterable indicia.

4
5 97. A radio frequency identification device in accordance with
6 claim 92 and further comprising an antenna coupled to the integrated
7 circuit, a battery coupled to the integrated circuit and powering the
8 integrated circuit, and a tag housing encapsulating the integrated circuit,
9 battery, and antenna.

10
11 98. A method of tracing manufacturing process problems by
12 tracing the origin of a defective radio frequency identification integrated
13 circuit, the method comprising:

14 forming a non-alterable indicia on a die for the integrated circuit,
15 the indicia representing the wafer lot number, wafer number, and die
16 number on the wafer, the indicia being not readily ascertainable by a
17 user; and

18 causing the integrated circuit to transmit the non-alterable indicia
19 via radio frequency in response to a manufacturer's command.

1 99. A method of tracing stolen property including a radio
2 frequency identification integrated circuit, the method comprising:

3 forming a non-alterable indicia on a die for the integrated circuit,
4 the indicia representing the wafer lot number, wafer number, and die
5 number on the wafer, the indicia being not readily ascertainable by a
6 user; and

7 causing the integrated circuit to transmit the non-alterable indicia
8 via radio frequency in response to a manufacturer's command.

9
10 100. A method of tracing manufacturing process problems in the
11 manufacture of a radio frequency integrated circuit by tracing defect
12 origin, the method comprising the following steps:

13 providing a detectable signature on the integrated circuit, the
14 signature indicative of one or more of the wafer lot number, wafer
15 number, and die number of a die for the integrated circuit; and

16 enabling the integrated circuit to transmit the signature via radio
17 frequency responsive to an inquiry command.

1 101. A radio frequency identification device comprising:
2 an integrated circuit including a microprocessor, a receiver
3 receiving radio frequency commands from an interrogation device, and
4 a transmitter transmitting a signal identifying the device to the
5 interrogator, the integrated circuit switching between a sleep mode, and
6 a microprocessor on mode, in which more power is consumed than in
7 the sleep mode, if the microprocessor determines that a signal received
8 by the receiver is a radio frequency command from an interrogation
9 device.

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1 102. A method for conserving power during operation of a radio
2 frequency identification device (RFID), the method comprising the
3 following steps:

4 providing a receiver, a transmitter, microprocessor, and wake-up
5 circuitry, the wake-up circuitry configured to selectively supply clock
6 signals to the processor and thus control power consumption of the
7 processor;

8 configuring the receiver with an antenna to receive radio frequency
9 signals from an interrogation device,

10 configuring the transmitter to transmit a signal identifying the
11 device to the interrogator;

12 selectively enabling powered wake-up of the receiver to periodically
13 check for presence of radio frequency signals;

14 detecting whether a radio frequency signal is valid; and

15 depending on whether a radio frequency signal is valid, supplying
16 clock signals to the processor.

17
18 103. A method in accordance with claim 102 wherein the
19 receiver, the transmitter, and the wake-up circuitry are provided on an
20 integrated circuit.
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1 104. A method for conserving power during operation of a radio
2 frequency identification device (RFID), the method comprising the
3 following steps:

4 providing a receiver, a transmitter, microprocessor, and wake-up
5 circuitry, the wake-up circuitry configured to selectively supply power to
6 the processor;

7 configuring the receiver with an antenna to receive radio frequency
8 signals from an interrogation device,

9 configuring the transmitter to transmit a signal identifying the
10 device to the interrogator;

11 selectively enabling powered wake-up of the receiver to periodically
12 check for presence of radio frequency signals;

13 detecting whether a radio frequency signal is valid; and

14 depending on whether a radio frequency signal is valid, supplying
15 power signals to the processor.

16
17 105. A method in accordance with claim 104 wherein the
18 receiver, the transmitter, and the wake-up circuitry are provided on an
19 integrated circuit.
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1 106. A radio frequency identification device comprising:
2 an integrated circuit including a microprocessor, a transmitter, and
3 a receiver, the integrated circuit being switchable between a sleep mode,
4 and a microprocessor on mode in which more power is consumed than
5 in the sleep mode, the integrated circuit being switched from the sleep
6 mode to the microprocessor on mode in response to a direct sequence
7 spread spectrum modulated radio frequency signal, which has a
8 predetermined number of transitions within a certain period of time,
9 being received by the receiver.

10
11 107. A method for conserving power in a radio frequency
12 identification device, the method comprising periodically switching from
13 a sleep mode to a receiver on mode and performing the following tests
14 to determine whether to further switch to a microprocessor on mode
15 because a valid radio frequency signal is present:

16 (a) determining if any radio frequency signal is present and, if
17 so, proceeding to step (b); and, if not, returning to the sleep mode;
18 and

19 (b) determining if the radio frequency signal has a
20 predetermined number of transitions per a predetermined time period
21 and, if so, switching to the microprocessor on mode; and, if not,
22 returning to the sleep mode.

23

24

1 108. A method in accordance with claim 107 wherein the radio
2 frequency identification device further comprises a clock recovery circuit
3 recovering a clock from incoming radio frequency signals, the clock
4 recovery circuit including a phase lock loop and wherein the tests
5 further comprise determining whether frequency lock is achieved on the
6 incoming radio frequency signal within a predetermined number of
7 transitions.

8
9 109. A radio frequency identification device switchable between
10 a sleep mode and a mode in which more power is consumed than in
11 the sleep mode, the radio frequency identification device comprising:

12 a transponder including a receiver and a transmitter;

13 means for periodically checking whether any radio frequency signal
14 is being received by the receiver; and

15 means for determining if a radio frequency signal has a
16 predetermined number of transitions within a predetermined period of
17 time.

1 110. A method for conserving power in a radio frequency
2 identification device, the method comprising periodically switching from
3 a sleep mode to a receiver on mode and performing the following tests
4 to determine whether to further switch to a microprocessor on mode
5 because a valid radio frequency signal is present:

6 (a) determining if any radio frequency signal is present and, if
7 so, proceeding to step (b); and, if not, returning to the sleep mode;

8 (b) determining if the radio frequency signal is modulated and
9 has a predetermined number of transitions per a predetermined period
10 of time and, if so, proceeding to step (c); and, if not, returning to the
11 sleep mode; and

12 (c) determining if the modulated radio frequency signal has a
13 predetermined number of transitions per a predetermined period of time
14 different from the predetermined time of step (b) and, if so, switching
15 to the microprocessor on mode; and, if not, returning to the sleep
16 mode.

17
18 111. A method in accordance with claim 110 wherein the radio
19 frequency identification device further comprises a clock recovery circuit
20 recovering a clock from incoming radio frequency signals, the clock
21 recovery circuit including a phase lock loop and wherein the tests
22 further comprise determining whether frequency lock is achieved on the
23 incoming radio frequency signal within a predetermined amount of time.

1 112. A method of forming an integrated circuit including a
2 Schottky diode, the method comprising:

3 providing a p-type substrate;
4 defining an n-type region relative to the substrate;
5 forming an insulator over the n-type region;
6 removing an area of the insulator for definition of a contact hole,
7 and removing an area encircling the contact hole;
8 forming n+regions in the n-type regions encircling the contact
9 hole;
10 depositing a Schottky metal in the contact hole; and
11 annealing the metal to form a silicide interface to the n-type
12 region.

13
14 113. A method in accordance with claim 112 and further
15 comprising depositing tungsten into the contact hole.
16

17 114. A method in accordance with claim 113 wherein the
18 tungsten is deposited by chemical vapor deposition.
19

20 115. A method in accordance with claim 113 and further
21 comprising planarizing the tungsten.
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1 116. A method of forming an integrated circuit including a
2 Schottky diode, the method comprising:

3 providing a substrate;
4 defining a p-type region relative to the substrate;
5 forming an insulator over the p-type region;
6 removing an area of the insulator for definition of a contact hole,
7 and removing an area encircling the contact hole;
8 forming p+regions in the p-type regions encircling the contact
9 hole;
10 depositing a Schottky metal in the contact hole; and
11 annealing the Schottky metal to form a silicide interface to the
12 p-type region.

13
14 117. A method in accordance with claim 116 and further
15 comprising depositing tungsten into the contact hole.

16
17 118. A method in accordance with claim 117 wherein the
18 tungsten is deposited by chemical vapor deposition.

19
20 119. A method in accordance with claim 117 and further
21 comprising planarizing the tungsten
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1 120. A method of forming an integrated circuit including a
2 Schottky diode, the method comprising:

3 providing a p-type substrate;
4 defining an n-well region relative to the substrate;
5 forming a BPSG insulator over the n-well region;
6 etching away an area of the BPSG for definition of a contact
7 hole, and etching an area encircling the contact hole;
8 forming n+regions in the n-well regions encircling the contact
9 hole;
10 depositing titanium in the contact hole; and
11 annealing the titanium to form a silicide interface to the n-well
12 region.

13
14 121. A method in accordance with claim 120 and further
15 comprising depositing tungsten into the contact hole.

16
17 122. A method in accordance with claim 121 wherein the
18 tungsten is deposited by chemical vapor deposition.

19
20 123. A method in accordance with claim 121 and further
21 comprising planarizing the tungsten.

1 124. A method of forming an integrated circuit including a
2 Schottky diode, the method comprising:

3 providing an n-type substrate;

4 defining a p-well region relative to the substrate;

5 forming a BPSG insulator over the p-well region;

6 etching away an area of the BPSG for definition of a contact
7 hole, and etching an area encircling the contact hole;

8 forming p+regions in the p-well regions encircling the contact
9 hole;

10 depositing titanium in the contact hole; and

11 annealing the titanium to form a silicide interface to the p-well
12 region.

13
14 125. A method in accordance with claim 124 and further
15 comprising depositing tungsten into the contact hole.

16
17 126. A method in accordance with claim 125 wherein the
18 tungsten is deposited by chemical vapor deposition.

19
20 127. A method in accordance with claim 125 and further
21 comprising planarizing the tungsten.

1 128. A radio frequency communications system comprising:
2 an antenna;
3 an integrated circuit including a receiver having a Schottky diode
4 detector including a Schottky diode coupled to the antenna; and
5 a current source connected to drive current through the antenna
6 and the Schottky diode.

7
8 129. A radio frequency communications system in accordance with
9 claim 128 wherein the receiver is inductorless.

10
11 130. An integrated circuit for radio frequency communications
12 comprising an inductorless radio frequency detector.

13
14 131. A system comprising:
15 an antenna;
16 a transponder including a receiver having a Schottky diode
17 detector including a Schottky diode having a first terminal coupled to
18 the antenna and having a second terminal; and
19 means for driving current through both the antenna and the
20 Schottky diode in a direction from the first terminal to the second
21 terminal.

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1 132. A system comprising:
2 an antenna;
3 a transponder including a receiver having a Schottky diode
4 detector including a Schottky diode having a first terminal coupled to
5 the antenna and having a second terminal; and
6 means for driving current through both the antenna and the
7 Schottky diode in a direction from the second terminal to the first
8 terminal.

9
10 133. A system comprising:
11 an antenna;
12 a transponder including a receiver having a Schottky diode
13 detector including a Schottky diode having an anode coupled to the
14 antenna and having a cathode; and
15 means for driving current through both the antenna and the
16 Schottky diode in a direction from the anode to the cathode.

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1 134. A radio frequency communications system comprising:
2 an antenna;
3 an integrated circuit including a receiver having a Schottky diode
4 detector including a Schottky diode having an anode coupled to the
5 antenna and having a cathode, the Schottky diode detector further
6 including a capacitor connected between the cathode and ground, and
7 including a capacitor having a first contact connected to the cathode
8 and having a second contact defining an output of the Schottky diode
9 detector;
10 a current source connected to the cathode to drive current
11 through the antenna and the Schottky diode in a direction from the
12 anode to the cathode.

1 135. A radio frequency communications system comprising:
2 an antenna;
3 an integrated circuit including a receiver having a Schottky diode
4 detector including a Schottky diode having a cathode coupled to the
5 antenna and having an anode, the Schottky diode detector further
6 including a capacitor connected between the anode and ground, and
7 including a capacitor having a first contact connected to the anode and
8 having a second contact defining an output of the Schottky diode
9 detector; and
10 a current source connected to the anode to drive current through
11 the antenna and the Schottky diode in a direction from the anode to
12 the cathode.

13
14 136. A system comprising:
15 an antenna;
16 a transponder including a receiver having a Schottky diode
17 detector including a Schottky diode having a cathode coupled to the
18 antenna and having an anode; and
19 means for driving current through both the antenna and the
20 Schottky diode in a direction from the anode to the cathode.

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1 137. A method for realizing an improved radio frequency detector
2 for use in a radio frequency identification device (RFID), the method
3 comprising the following steps:

4 providing an integrated circuit and an antenna, the integrated
5 circuit having a receiver and a transmitter, the integrated circuit further
6 having a Schottky diode and a current source, with the Schottky diode
7 in operation being coupled to the antenna and the current source, the
8 Schottky diode and antenna cooperating there between to form an
9 inductorless radio frequency detector;

10 applying a supply of power to the integrated circuit device from
11 a battery; and

12 applying a desired current across the Schottky diode to impart a
13 desired impedance there across relative to the impedance of the
14 antenna.

15
16 138. A frequency lock loop comprising:

17 a current controlled oscillator including a plurality of selectively
18 engageable current mirrors, the frequency of oscillation of the frequency
19 lock loop varying in response to selection of the current mirrors, the
20 current mirrors including transistors operating in a subthreshold mode.

1 139. A frequency lock loop in accordance with claim 138 and
2 further comprising a current source including a thermal voltage
3 generator, and wherein the selected current mirrors multiply up the
4 current from the current source to a current for controlling the
5 frequency of oscillation.

6
7 140. A frequency lock loop in accordance with claim 138 wherein
8 the current mirrors are arranged in selectable groups of varying numbers
9 of transistors to define a binary weighting scheme.

10
11 141. A frequency lock loop in accordance with claim 140 and
12 further comprising digital select lines, and wherein the groups are
13 selected by signals on the digital select lines.

14
15 142. An integrated circuit comprising a receiver, a transmitter,
16 and a frequency lock loop including a current source having a thermal
17 voltage generator, a current controlled oscillator having a plurality of
18 selectively engageable current mirrors multiplying up the current of the
19 current source, the frequency of oscillation of the frequency lock loop
20 varying in response to selection of the current mirrors, the current
21 mirrors including transistors operating in a subthreshold mode.

1 143. A frequency lock loop in accordance with claim 142 wherein
2 the current mirrors are arranged in selectable groups of varying numbers
3 of transistors to define a binary weighting scheme.
4

5 144. A frequency lock loop in accordance with claim 143 and
6 further comprising digital select lines, and wherein the groups are
7 selected by signals on the digital select lines.
8

9 145. A timing oscillator that consumes less than one milliAmp.
10

11 146. A method of constructing a frequency lock loop including
12 a current controlled oscillator having a plurality of selectively engageable
13 current mirrors, the frequency of oscillation of the frequency lock loop
14 varying in response to selection of the current mirrors, the method
15 comprising selecting current mirrors to vary frequency of operation, and
16 operating transistors in the current mirrors in subthreshold mode.
17

18 147. A method in accordance with claim 146 and further
19 comprising using a current source including a thermal voltage generator,
20 and arranging the current mirrors so the engaged current mirrors
21 multiply up the current from the current source to a current for
22 controlling the frequency of oscillation.
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24

1 148. A method in accordance with claim 146 and further
2 comprising arranging the current mirrors in selectable groups of varying
3 numbers of transistors to define a binary weighting scheme.
4

5 149. A method in accordance with claim 148 and further
6 comprising selecting the groups using digital signals.
7

8 150. A method of operating an integrated circuit including a
9 receiver, a transmitter, and a frequency lock loop including a current
10 source having a thermal voltage generator, a current controlled oscillator
11 having a plurality of selectively engageable current mirrors multiplying
12 up the current of the current source, the frequency of oscillation of the
13 frequency lock loop varying in response to selection of the current
14 mirrors, the method comprising engaging selected current mirrors and
15 operating transistors in the current mirrors in a subthreshold mode.
16

17 151. A method in accordance with claim 150 and further
18 comprising arranging the current mirrors in selectable groups of varying
19 numbers of transistors to define a binary weighting scheme.
20

21 152. A method in accordance with claim 151 and further
22 comprising selecting the groups using signals on digital select lines.
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1 153. An amplifier powered by a selectively engageable voltage
2 source, the amplifier comprising:

3 first and second electrodes for receiving an input signal to be
4 amplified, the input electrodes being adapted to be respectively
5 connected to coupling capacitors;

6 a differential amplifier having inputs respectively connected to the
7 first and second electrodes, and having an output;

8 selectively engageable resistances between the voltage source and
9 respective inputs of the differential amplifier and defining, with the
10 coupling capacitors, the high pass characteristics of the circuit; and

11 second selectively engageable resistances between the voltage
12 source and respective inputs of the differential amplifier, the second
13 resistances respectively having smaller values than the first mentioned
14 resistances, the second resistances being engaged then disengaged in
15 response to the voltage source being engaged.

16
17 154. An amplifier in accordance with claim 152 and further
18 comprising coupling capacitors respectively connected to the first and
19 second electrodes.

20
21 155. An amplifier in accordance with claim 152 and further
22 comprising a voltage divider, and wherein the first mentioned and
23 second resistances are connected to the voltage source via the voltage
24 divider.

1 156. An amplifier in accordance with claim 152 wherein the first
2 mentioned resistances comprise respective transistors.

3
4 157. An amplifier in accordance with claim 152 wherein the first
5 mentioned resistances comprise respective p-type transistors.

6
7 158. An amplifier in accordance with claim 152 wherein the
8 second resistances comprise respective transistors.

9
10 159. An amplifier in accordance with claim 152 wherein the
11 second resistances comprise respective p-type transistors.
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1 160. A radio frequency identification device comprising:
2 an integrated circuit including a microprocessor, a receiver
3 receiving radio frequency commands from an interrogation device, and
4 a transmitter transmitting a signal identifying the device to the
5 interrogator, the integrated circuit switching between a sleep mode, and
6 a microprocessor on mode, in which more power is consumed than in
7 the sleep mode, if the microprocessor determines that a signal received
8 by the receiver is a radio frequency command from an interrogation
9 device, the integrated circuit further including an amplifier powered by
10 a selectively engageable voltage source engaged in the microprocessor
11 on mode but not in the sleep mode, the amplifier including first and
12 second electrodes for receiving an input signal to be amplified, the
13 input electrodes being adapted to be respectively connected to coupling
14 capacitors, a differential amplifier having inputs respectively connected
15 to the first and second electrodes, and having an output, selectively
16 engageable resistances between the voltage source and respective inputs
17 of the differential amplifier, second selectively engageable resistances
18 between the voltage source and respective inputs of the differential
19 amplifier, the second resistances respectively having smaller values than
20 the first mentioned resistances, the second resistances being engaged
21 then disengaged in response to the integrated circuit switching from the
22 sleep mode to the microprocessor on mode.
23
24

1 161. A radio frequency identification device in accordance with
2 claim 160 and further comprising coupling capacitors respectively
3 connected to the first and second electrodes.
4

5 162. A radio frequency identification device in accordance with
6 claim 160 and further comprising a voltage divider, and wherein the
7 first mentioned and second resistances are connected to the voltage
8 source via the voltage divider.
9

10 163. A radio frequency identification device in accordance with
11 claim 160 wherein the first mentioned resistances comprise respective
12 transistors.
13

14 164. A radio frequency identification device in accordance with
15 claim 160 wherein the first mentioned resistances comprise respective p-
16 type transistors.
17

18 165. A radio frequency identification device in accordance with
19 claim 160 wherein the second resistances comprise respective transistors.
20

21 166. A radio frequency identification device in accordance with
22 claim 160 wherein the second resistances comprise respective p-type
23 transistors.
24

1 167. A method of speeding power up of an amplifier stage
2 powered by a voltage source and including first and second electrodes
3 for receiving an input signal to be amplified, the input electrodes being
4 adapted to be respectively connected to coupling capacitors; a
5 differential amplifier having inputs respectively connected to the first and
6 second electrodes, and having an output; and selectively engageable
7 resistances between the voltage source and respective inputs of the
8 differential amplifier, the method comprising:

9 shorting around the selectively engageable resistances for a
10 predetermined amount of time in response to the voltage source being
11 engaged.

12
13 168. A method in accordance with claim 167 wherein the shorting
14 step comprises engaging selectively engageable second resistances
15 respectively connected in parallel with the first mentioned resistances
16 and having respective resistance values lower than the first mentioned
17 resistances.

1 169. A radio frequency communications system comprising:
2 an antenna;
3 an integrated circuit including a receiver having a Schottky diode
4 detector including a Schottky diode having an anode coupled to the
5 antenna and having a cathode, the Schottky diode detector further
6 including a capacitor connected between the cathode and ground, and
7 including a capacitor having a first contact connected to the cathode
8 and having a second contact defining an output of the Schottky diode
9 detector, the integrated circuit further including a clock recovery circuit
10 recovering a clock from rising edges only of a signal at the output of
11 the Schottky diode detector; and
12 a current source connected to drive current through the antenna
13 and the Schottky diode in a direction from the anode to the cathode.

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1 170. A radio frequency communications system comprising:
2 an antenna;
3 an integrated circuit including a receiver having a Schottky diode
4 detector including a Schottky diode having a cathode coupled to the
5 antenna and having an anode, the Schottky diode detector further
6 including a capacitor connected between the anode and ground, and
7 including a capacitor having a first contact connected to the anode and
8 having a second contact defining an output of the Schottky diode
9 detector, the integrated circuit further including a clock recovery circuit
10 recovering a clock from falling edges only of a signal at the output of
11 the Schottky diode detector; and

12 a current source connected to drive current through the antenna
13 and the Schottky diode in a direction from the anode to the cathode.
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1 171. A method of recovering a clock in a radio frequency
2 communications system, the method comprising:

3 providing an antenna;

4 providing a receiver having a Schottky diode detector including a
5 Schottky diode having an anode coupled to the antenna and having a
6 cathode, the Schottky diode detector further including a capacitor
7 connected between the cathode and ground, and including a capacitor
8 having a first contact connected to the cathode and having a second
9 contact defining an output of the Schottky diode detector;

10 driving current through the antenna and the Schottky diode in a
11 direction from the anode to the cathode; and

12 recovering a clock from rising edges only of a signal at the
13 output of the Schottky diode detector.

1 172. A method of recovering a clock in a radio frequency
2 communications system, the method comprising:

3 providing an antenna;

4 providing a receiver having a Schottky diode detector including a
5 Schottky diode having a cathode coupled to the antenna and having an
6 anode, the Schottky diode detector further including a capacitor
7 connected between the anode and ground, and including a capacitor
8 having a first contact connected to the anode and having a second
9 contact defining an output of the Schottky diode detector;

10 driving current through the antenna and the Schottky diode in a
11 direction from the anode to the cathode; and

12 recovering a clock from falling edges only of a signal at the
13 output of the Schottky diode detector.
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1 173. A stage for a voltage controlled oscillator, the stage
2 comprising:

3 a first transistor having a control electrode defining a first input,
4 and having first and second power electrodes, the first power electrode
5 defining a first node;

6 a second transistor having a control electrode defining a second
7 input, and having first and second power electrodes, the first power
8 electrode of the second transistor defining a second node;

9 a current source connected to the second power electrodes of the
10 first and second transistors and directing current away from the second
11 power electrodes of the first and second transistors; and

12 means defining a variable resistance connecting the first and
13 second nodes to a supply voltage.
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1 174. A stage for a voltage controlled oscillator, the stage
2 comprising:

3 a first p-channel transistor having a gate defining a control node,
4 having a source adapted to be connected to a supply voltage, and
5 having a drain;

6 a second p-channel transistor having a gate connected to the
7 control node, having a source connected to the supply voltage, and
8 having a drain;

9 a first n-channel transistor having a gate defining a first input,
10 having a drain connected to the drain of the first p-channel transistor
11 and defining a first node, and having a source;

12 a second n-channel transistor having a gate defining a second
13 input, having a drain connected to the drain of the second p-channel
14 transistor and defining a second node, and having a source;

15 a current source connected to the sources of the first and second
16 n-channel transistors directing current from the sources of the first and
17 second n-channel transistors;

18 a first resistor connected between the supply voltage and the drain
19 of the first n-type transistor;

20 a second resistor connected between the supply voltage and drain
21 of the second n-type transistor;

22 a first source follower having an input connected to the first node
23 and having an output defining a first output of the stage; and
24

1 a second source follower having an input connected to the second
2 node and having an output defining a second output of the stage.

3
4 175. A transmitter including a ring oscillator having a chain of
5 stages, each stage comprising:

6 a first p-channel transistor having a gate defining a control node,
7 having a source adapted to be connected to a supply voltage, and
8 having a drain;

9 a second p-channel transistor having a gate connected to the
10 control node, having a source connected to the supply voltage, and
11 having a drain;

12 a first n-channel transistor having a gate defining a first input,
13 having a drain connected to the drain of the first p-channel transistor
14 and defining a first node, and having a source;

15 a second n-channel transistor having a gate defining a second
16 input, having a drain connected to the drain of the second p-channel
17 transistor and defining a second node, and having a source;

18 a current source connected to the sources of the first and second
19 n-channel transistors directing current from the sources of the first and
20 second n-channel transistors;

21 a first resistor connected between the supply voltage and the drain
22 of the first n-type transistor;

23 a second resistor connected between the supply voltage and drain
24 of the second n-type transistor;

1 a first source follower having an input connected to the first node
2 and having an output defining a first output of the stage; and

3 a second source follower having an input connected to the second
4 node and having an output defining a second output of the stage.
5

6 176. A method of varying frequency in a stage of a voltage
7 controlled oscillator having two input transistors having gates defining
8 input nodes and having drain to source paths adapted to be connected
9 between a supply voltage and a current source, the method comprising
10 providing an impedance between the input transistors and the supply
11 voltage, and varying the impedance.
12

13 177. A frequency doubler comprising:

14 a first Gilbert cell;

15 a second Gilbert cell coupled to the first Gilbert cell;

16 a frequency generator configured to apply a first sinusoidal wave
17 to the first Gilbert cell; and

18 a phase shifter applying a sinusoidal wave shifted from the first
19 sinusoidal wave to the second Gilbert cell.
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178. A frequency doubler comprising:

a first Gilbert cell including a first pair of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair having a gate defining a first input node and a first one of the transistors of the second pair having a gate connected to the first input node, a second one of the transistors of the first pair having a gate defining a second input node and a second one of the transistors of the second pair having a gate connected to the second input node, the first transistor of the first pair having a drain, and the second transistor of the second pair having a drain connected to the drain of the first transistor of the first pair, the second transistor of the first pair having a drain, and the first transistor of the second pair having a drain connected to the drain of the second transistor of the first pair, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair having a drain connected to the source of the second transistor of the first pair, the second transistor of the third pair having a drain connected to the source of the second transistor of the second pair, and a current source connected to the sources of the third pair and forward biasing the third pair, the second transistor of the third pair having a gate defining a third input node, and the first transistor of the third pair having a gate defining a fourth input node; and

1 a second Gilbert cell including a first pair of transistors having
2 sources that are connected together, a second pair of transistors having
3 sources that are connected together, a first one of the transistors of the
4 first pair of the second cell having a gate defining a first input node
5 and a first one of the transistors of the second pair of the second cell
6 having a gate connected to the first input node of the second cell, a
7 second one of the transistors of the first pair of the second cell having
8 a gate defining a second input node of the second cell and a second
9 one of the transistors of the second pair of the second cell having a
10 gate connected to the second input node of the second cell, the first
11 transistor of the first pair of the second cell having a drain, and the
12 second transistor of the second pair of the second cell having a drain
13 connected to the drain of the first transistor of the first pair of the
14 second cell, the second transistor of the first pair of the second cell
15 having a drain, and the first transistor of the second pair of the second
16 cell having a drain connected to the drain of the second transistor of
17 the first pair of the second cell, a third pair including first and second
18 transistors having sources coupled together, the first transistor of the
19 third pair of the second cell having a drain connected to the source of
20 the second transistor of the first pair of the second cell, the second
21 transistor of the third pair of the second cell having a drain connected
22 to the source of the second transistor of the second pair of the second
23 cell, and a current source connected to the sources of the third pair
24 of the second cell and forward biasing the third pair of the second cell,

1 the second transistor of the third pair of the second cell having a gate
2 defining a third input node of the second cell, and the first transistor
3 of the third pair of the second cell having a gate defining a fourth
4 input node of the second cell; the drain of the second transistor of the
5 first pair of the second cell being connected to the drain of the second
6 transistor of the first pair of the first cell, the drain of the second
7 transistor of the second pair of the second cell being connected to the
8 drain of the second transistor of the second pair of the second cell, the
9 first input node of the second cell being connected to the fourth input
10 node of the first cell, the third input node of the second cell being
11 connected to the second input node of the first cell, and the fourth
12 input node of the second cell being connected to the first input node
13 of the first cell.

14
15 179. A method of doubling frequency without using a feedback
16 loop, the method comprising:

17 providing a first Gilbert cell;

18 providing a second Gilbert cell coupled to the first Gilbert cell;

19 applying a first sinusoidal wave to the first Gilbert cell; and

20 applying a sinusoidal wave shifted from the first sinusoidal wave
21 to the second Gilbert cell.

1 180. A pseudo random number generator comprising:
2 a linear feedback shift register switchably operable in a first
3 mode, and in a second mode wherein the shift register consumes more
4 power than in the first mode.

5
6 181. A method of generating a pseudo random number, the
7 method comprising:

8 providing a linear feedback shift register;

9 providing an oscillator which generates clock signals used by the
10 linear feedback shift register for shifting; and

11 providing a first power level to the oscillator when a pseudo
12 random number is required, and providing a second power level, lower
13 than the first power level, to the oscillator at other times.

14
15 182. A method of generating a pseudo random number, the
16 method comprising:

17 providing a linear feedback shift register;

18 providing an oscillator which generates clock signals used by the
19 linear feedback shift register for shifting; and operating the oscillator at
20 a first frequency in response to a request for a pseudo random number,
21 and operating the oscillator at a second frequency lower than the first
22 frequency after the pseudo random number is generated.

23

24

1 183. A method in accordance with claim 182 and further
2 comprising supplying power to the oscillator from a thermal voltage
3 generator to cause the oscillator to operate at the second frequency.

4
5 184. A system comprising:

6 a microprocessor operating at a frequency;

7 a linear feedback shift register operable in a low power mode,
8 wherein the shift register operates at a frequency below the frequency
9 of the microprocessor, and a high power mode wherein the shift register
10 consumes more power than in the low power mode, operates at the
11 frequency of the microprocessor, and shifts data into the microprocessor.

1 185. A radio frequency identification device comprising:
2 an integrated circuit including a receiver, a transmitter, a thermal
3 voltage generator, a microprocessor operating at a frequency, a linear
4 feedback shift register operable in a low power mode, wherein the shift
5 register operates at a frequency below the frequency of the
6 microprocessor, and a high power mode wherein the shift register
7 consumes more power than in the low power mode, operates at the
8 frequency of the microprocessor, and shifts data into the microprocessor,
9 an oscillator supplying clock signals to the shift register, and current
10 mirrors supplying current to each stage of the shift register, the current
11 mirrors being referenced to the thermal voltage generator when the shift
12 register is in the low power mode, and, when the shift register is in
13 the high power mode, connected to a supply voltage potential greater
14 than the potential provided by the thermal voltage generator.

1 186. A method of generating a pseudo random number, the
2 method comprising:

3 providing a thermal voltage generator, a linear feedback shift
4 register, an oscillator supplying clock signals to the shift register, and
5 current mirrors supplying current to each stage of the shift register;

6 referencing the current mirrors to the thermal voltage generator
7 when no pseudo random number is required; and

8 connecting the current mirrors to a supply voltage potential
9 greater than the potential provided by the thermal voltage generator
10 when a pseudo random number is required.

11
12 187. An integrated circuit comprising a receiver and a transmitter
13 sharing a common antenna.

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15 188. A method of using an integrated circuit including a receiver
16 and a transmitter, the method comprising connecting the receiver and
17 transmitter to a common antenna.

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189. An integrated circuit comprising:

a die including a transmitter having an antenna output and a detector having an antenna input;

a package housing the die;

a first contact connected to the antenna output and accessible from outside the package;

a second contact connected to the antenna input and accessible from outside the package; and

a short electrically connecting the first contact to the second contact outside the package.

190. A method of using an integrated circuit including a die having a transmitter including an antenna output and a detector including an antenna input, the integrated circuit further including a package housing the die, a first contact connected to the antenna output and accessible from outside the package, and a second contact connected to the antenna input and accessible from outside the package, the method comprising:

electrically shorting the first contact to the second contact outside the package.

1 191. A transceiver comprising:

2 an antenna having a first end connected to a bias voltage, and
3 having a second end;

4 a detector including a Schottky diode having an anode connected
5 to the second end of the antenna; and

6 a transmitter having an output connected to the second end of
7 the antenna.
8

9 192. A transceiver in accordance with claim 191 wherein the
10 Schottky diode has a cathode, and further comprising a current source
11 directing current in the direction from the anode to the cathode.
12

13 193. A transceiver in accordance with claim 191 wherein the
14 receiver and transmitter do not operate simultaneously.
15

16 194. A transceiver in accordance with claim 191 wherein the
17 Schottky diode has a cathode, and wherein the detector and transmitter
18 do not operate simultaneously, the transceiver further comprising a
19 current source directing current in the direction from the anode to the
20 cathode, and a pullup transistor connected to the cathode and
21 configured to connect the cathode to the bias voltage when the
22 transmitter is operating.
23
24

1 195. A radio frequency identification device comprising:

2 an integrated circuit including both a receiver and a transmitter;

3 a first antenna connected to the receiver; and

4 a second antenna connected to the transmitter.

5
6 196. A radio frequency identification device in accordance with
7 claim 195 wherein the receiver includes a Schottky diode having a
8 cathode and an anode, and further comprising a current source directing
9 current in the direction from the anode to the cathode.

10
11 197. A radio frequency identification device in accordance with
12 claim 195 wherein the receiver and transmitter do not operate
13 simultaneously.

14
15 198. A transceiver comprising:

16 a loop antenna having a first end connected to a bias voltage,
17 and having a second end;

18 a second antenna;

19 a detector including a Schottky diode having an anode connected
20 to the second end of the antenna; and

21 a transmitter having an output connected to the second antenna.
22
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1 199. A transceiver in accordance with claim 198 wherein the
2 Schottky diode has a cathode, and further comprising a current source
3 directing current in the direction from the anode to the cathode.
4

5 200. A transceiver in accordance with claim 198 wherein the
6 receiver and transmitter do not operate simultaneously.
7

8 201. A transceiver comprising:

9 an antenna having a first end connected to a bias voltage, and
10 having a second end;

11 a detector including a Schottky diode having an anode connected
12 to the second end of the antenna; and

13 an active transmitter having an output connected to the second
14 end of the antenna.
15

16 202. A transceiver in accordance with claim 201 wherein the
17 Schottky diode has a cathode, and further comprising a current source
18 directing current in the direction from the anode to the cathode.
19

20 203. A transceiver in accordance with claim 201 wherein the
21 receiver and transmitter do not operate simultaneously.
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1 204. A transceiver in accordance with claim 201 wherein the
2 Schottky diode has a cathode, and wherein the detector and transmitter
3 do not operate simultaneously, the transceiver further comprising a
4 current source directing current in the direction from the anode to the
5 cathode, and a pullup transistor connected to the cathode and
6 configured to connect the cathode to the bias voltage when the
7 transmitter is operating.

8
9 205. A transceiver comprising:

10 an antenna having a first end, and having a second end;

11 a detector including a Schottky diode having a cathode connected
12 to the second end of the antenna and defining a potential at the
13 second end of the antenna, the first end of the antenna being
14 connected to a potential lower than the potential of the second end of
15 the antenna; and

16 a backscatter transmitter including a transistor having a first power
17 electrode connected to the first end of the antenna, a second power
18 electrode connected to the second end of the antenna, and a control
19 electrode adapted to have a modulation signal applied thereto.

20
21 206. A transceiver in accordance with claim 205 and further
22 comprising a current source directing current in the direction from the
23 anode to the cathode.

1 207. A transceiver in accordance with claim 205 wherein the
2 receiver and transmitter do not operate simultaneously.

3
4 208. A transceiver in accordance with claim 205 and further
5 comprising an integrated circuit package housing the detector and
6 transmitter, and wherein the antenna is external of the package.

7
8 209. A transceiver comprising:

9 a loop antenna having a first end connected to a bias voltage,
10 and having a second end;

11 a detector including a Schottky diode having an anode connected
12 to the second end of the antenna;

13 a backscatter transmitter having a first output and having a
14 second output;

15 a capacitor connected between the first output and the first end
16 of the antenna; and

17 a capacitor connected between the second output and the second
18 end of the antenna.

19
20 210. A transceiver in accordance with claim 209 wherein the
21 Schottky diode has a cathode, and further comprising a current source
22 directing current in the direction from the anode to the cathode.

1 211. A transceiver in accordance with claim 209 wherein the
2 receiver and transmitter do not operate simultaneously.

3
4 212. A transceiver in accordance with claim 209 and further
5 comprising an integrated circuit package housing the detector and
6 transmitter, and wherein the first and second capacitors are external of
7 the package.

8
9 213. A method of configuring a transceiver including a backscatter
10 transmitter having first and second outputs, and a detector having a
11 Schottky diode including an anode, the method comprising:

12 applying a bias voltage to a first end of an antenna;

13 connecting a second end of the antenna to the anode;

14 connecting a capacitor between the first output and the first end
15 of the antenna; and

16 connecting a capacitor between the second output and the second
17 end of the antenna.

18
19 214. A method in accordance with claim 213 wherein the
20 Schottky diode has a cathode, and further comprising directing current
21 in the direction from the anode to the cathode.

22
23 215. A method in accordance with claim 213 wherein the receiver
24 and transmitter do not operate simultaneously.

1 216. A method in accordance with claim 213 and further
2 comprising housing the detector and transmitter in an integrated circuit
3 package, and connecting the first and second capacitors external of the
4 package.

5
6 217. A method of arranging a transceiver including a backscatter
7 transmitter and a detector having a Schottky diode including a cathode,
8 the method comprising:

9 connecting a first end of an antenna to a ground potential;
10 connecting a second end of the antenna to the cathode; and
11 connecting a first power electrode of a transistor to the first end
12 of the antenna;
13 connecting a second power electrode connected to the second end
14 of the antenna; and
15 connecting a control electrode of the transistor to a modulation
16 signal.

17
18 218. A method in accordance with claim 217 and further
19 comprising a current source directing current in the direction from the
20 anode to the cathode.

21
22 219. A method in accordance with claim 217 wherein the receiver
23 and transmitter do not operate simultaneously.
24

1 220. A method in accordance with claim 217 and further
2 comprising housing the detector and transmitter in an integrated circuit
3 package, and locating the antenna external of the package.
4

5 221. A method of determining when a phase lock loop achieves
6 frequency lock relative to a desired frequency, the phase lock loop
7 including a voltage controlled oscillator having a control node and
8 oscillating at a frequency responsive to the voltage applied to the
9 control node, the method comprising:

10 crossing the voltage that would result in the phase lock loop
11 tracking the desired frequency in a first direction;

12 crossing the voltage that would result in the phase lock loop
13 tracking the desired frequency in a second direction opposite the first
14 direction; and

15 indicating that frequency lock has been achieved.
16

17 222. A method in accordance with claim 221 and further
18 comprising adjusting the voltage in the first direction after the second
19 mentioned crossing step and before the indicating step.
20

21 223. A method in accordance with claim 221 wherein the first
22 mentioned crossing comprises adjusting, using steps, the voltage applied
23 to the control node.
24

1 224. A method in accordance with claim 223 wherein the second
2 mentioned crossing comprises adjusting the voltage applied to the control
3 node using steps smaller than the steps used in the first mentioned
4 crossing.

5
6 225. A method in accordance with claim 221 and further
7 comprising adjusting the voltage in the first direction after the second
8 mentioned crossing step and before the indicating step, and wherein the
9 adjusting comprises using a step smaller than the steps used in the first
10 mentioned crossing.

1 226. A method of determining when frequency lock occurs
2 relative to a desired frequency, the method comprising:

3 providing a phase lock loop including a voltage controlled
4 oscillator that oscillates at a frequency responsive to voltage applied to
5 the voltage controlled oscillator;

6 applying a voltage to the voltage controlled oscillator to produce
7 a frequency of oscillation less than the desired frequency;

8 increasing the voltage applied to the voltage controlled oscillator
9 using one or more steps of a first size;

10 increasing the voltage applied to the voltage controlled oscillator
11 using one or more steps of a second size smaller than the first size;

12 decreasing the voltage applied to the voltage controlled oscillator
13 using one or more steps of a third size smaller than the second size;

14 increasing the voltage applied to the voltage controlled oscillator
15 using a step of the third size; and

16 indicating that lock has occurred in response to the increase of
17 the step of the third size.

18
19 227. A method in accordance with claim 226 wherein the phase
20 lock loop tracks a timing signal.

1 228. A method in accordance with claim 226 wherein the voltage
2 controlled oscillator has a control node, and wherein the voltage
3 controlled oscillator oscillates at a frequency responsive to the voltage
4 applied to the control node.

5
6 229. A method of determining when a phase lock loop achieves
7 frequency lock relative to a desired frequency, the phase lock loop
8 including a voltage controlled oscillator having a control node and
9 oscillating at a frequency responsive to the voltage applied to the
10 control node, the method comprising:

11 increasing the voltage applied to the control node to a voltage
12 above the voltage that would result in the phase lock loop tracking the
13 desired frequency;

14 decreasing the voltage applied to the control node to a voltage
15 below the voltage that would result in the phase lock loop tracking the
16 desired frequency; and

17 increasing the voltage applied to the control node and indicating
18 that frequency lock has been achieved.

19
20 230. A method in accordance with claim 229 wherein the first
21 mentioned increasing of the voltage applied to the control node
22 comprises increasing in steps the voltage applied to the control node.

1 231. A method in accordance with claim 230 wherein the
2 decreasing of the voltage applied to the control node comprises
3 decreasing the voltage applied to the control node using steps smaller
4 than the steps used in the first mentioned increasing of the voltage
5 applied to the control node.

6
7 232. A method in accordance with claim 230 wherein the second
8 mentioned increasing of the voltage applied to the control node
9 comprises increasing the voltage applied to the control node using a
10 step smaller than the steps used in the first mentioned increasing of the
11 voltage applied to the control node.

12
13 233. A radio frequency identification device comprising:
14 an integrated circuit including a microprocessor, a transmitter, and
15 a receiver, the integrated circuit periodically switching between a sleep
16 mode, and a receiver-on mode in which more power is consumed than
17 in the sleep mode, and further including a selectively engageable timer
18 preventing switching from the sleep mode to the receiver-on mode for
19 a predetermined amount of time.

20
21 234. A radio frequency identification device in accordance with
22 claim 233 wherein the timer is a countdown timer.

1 235. A radio frequency identification device in accordance with
2 claim 233 wherein the timer comprises a counter.

3
4 236. A radio frequency identification device in accordance with
5 claim 233 wherein the timer is set by a radio frequency signal received
6 by the receiver.

7
8 237. A radio frequency identification device comprising:
9 an integrated circuit including a microprocessor, a transmitter, and
10 a receiver, the integrated circuit periodically switching between a sleep
11 mode, and a receiver-on mode in which more power is consumed than
12 in the sleep mode, and further including means for selectively preventing
13 switching from the sleep mode to the receiver-on mode for a
14 predetermined amount of time.

15
16 238. A radio frequency identification device in accordance with
17 claim 237 wherein the means comprises a countdown timer.

18
19 239. A radio frequency identification device in accordance with
20 claim 237 wherein the means comprises a counter.

21
22 240. A radio frequency identification device in accordance with
23 claim 237 wherein the means prevents switching from the sleep mode
24 in response to a radio frequency signal received by the receiver.

1 241. A radio frequency identification device comprising:
2 an integrated circuit including a microprocessor, a transmitter, and
3 a receiver, the integrated circuit being switchable between a sleep mode,
4 and a mode in which more power is consumed than in the sleep mode,
5 the integrated circuit being switched from the sleep mode to the mode
6 in which more power is consumed in response to a direct sequence
7 spread spectrum modulated radio frequency signal being received by the
8 receiver which has a predetermined number of transitions within a
9 certain period of time, the integrated circuit further including a
10 selectively engageable timer which prevents switching from the sleep
11 mode for a period of time regardless of whether a signal is
12 subsequently received by the receiver which has the predetermined
13 number of transitions within a certain period of time.

14
15 242. A radio frequency identification device in accordance with
16 claim 241 wherein the timer is a countdown timer.

17
18 243. A radio frequency identification device in accordance with
19 claim 241 wherein the timer comprises a counter.

20
21 244. A radio frequency identification device in accordance with
22 claim 241 wherein the timer is set by a radio frequency signal received
23 by the receiver.
24

1 245. A method for conserving power in a radio frequency
2 identification device, the method comprising:

3 periodically switching from a sleep mode to a receiver on mode
4 and performing tests to determine whether to further switch to a
5 microprocessor on mode because a valid radio frequency signal is
6 present; and

7 selectively disabling the periodic switching from the sleep mode for
8 a predetermined amount of time.

9
10 246. A method for conserving power in accordance with
11 claim 245 wherein the selective disabling is performed in response to
12 a radio frequency command.

13
14 247. A method for conserving power in accordance with claim
15 245 wherein the selective disabling is performed in response to a radio
16 frequency command, and wherein the selective disabling cannot be
17 cancelled by a subsequent radio frequency command.

18
19 248. A method in accordance with claim 245 wherein the step
20 of selectively disabling comprises setting a timer.

21
22 249. A method in accordance with claim 245 wherein the step
23 of selectively disabling comprises setting a countdown timer.

24

1 250. A method in accordance with claim 245 wherein the
2 predetermined amount of time is selected via a radio frequency
3 command.

4
5 251. A method in accordance with claim 245 wherein the
6 predetermined amount of time is variable.

7
8 252. A method in accordance with claim 245 wherein the
9 predetermined amount of time is selectable from a number of available
10 amounts of time.

11
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ABSTRACT OF THE DISCLOSURE

A radio frequency identification device comprises an integrated circuit including a receiver, a transmitter, and a microprocessor. The receiver and transmitter together define an active transponder. The integrated circuit is preferably a monolithic single die integrated circuit including the receiver, the transmitter, and the microprocessor. Because the device includes an active transponder, instead of a transponder which relies on magnetic coupling for power, the device has a much greater range.

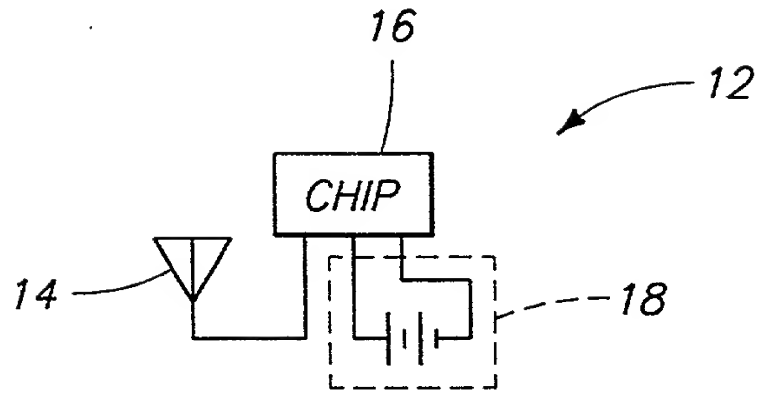


FIG. 1

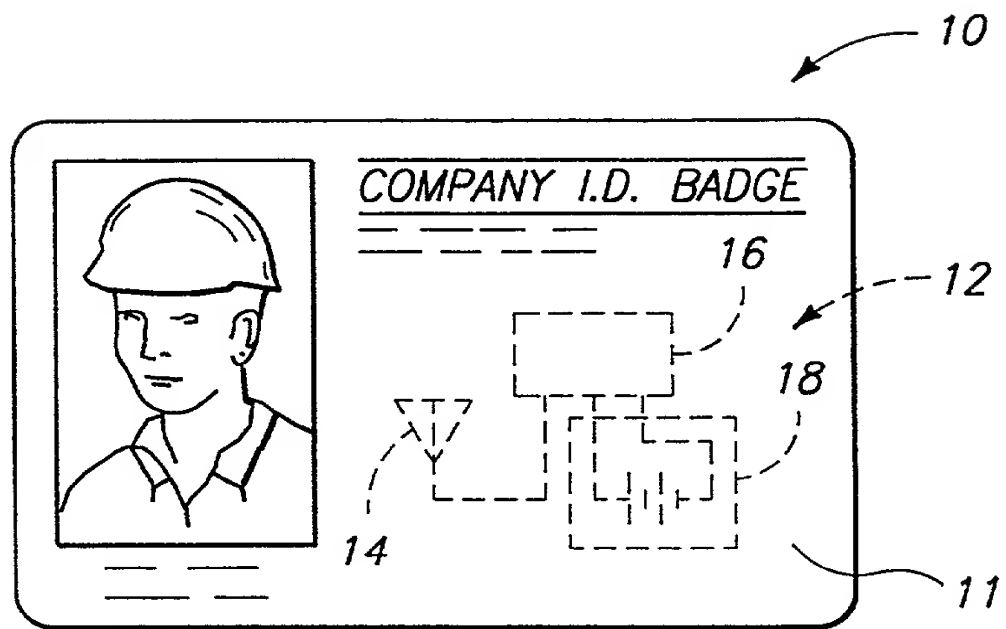


FIG. 2

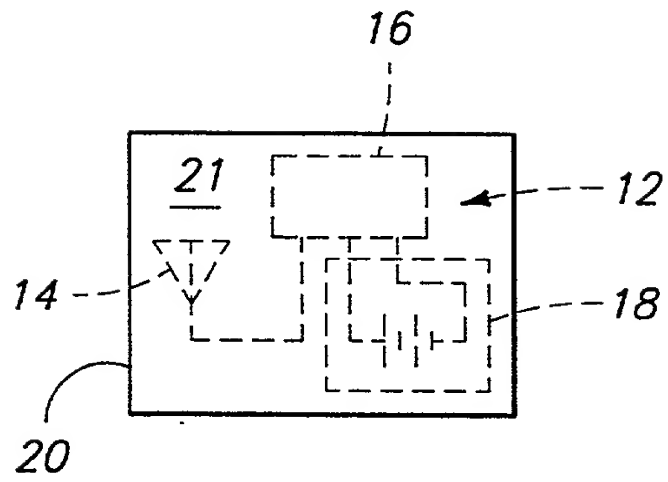


FIG. 1

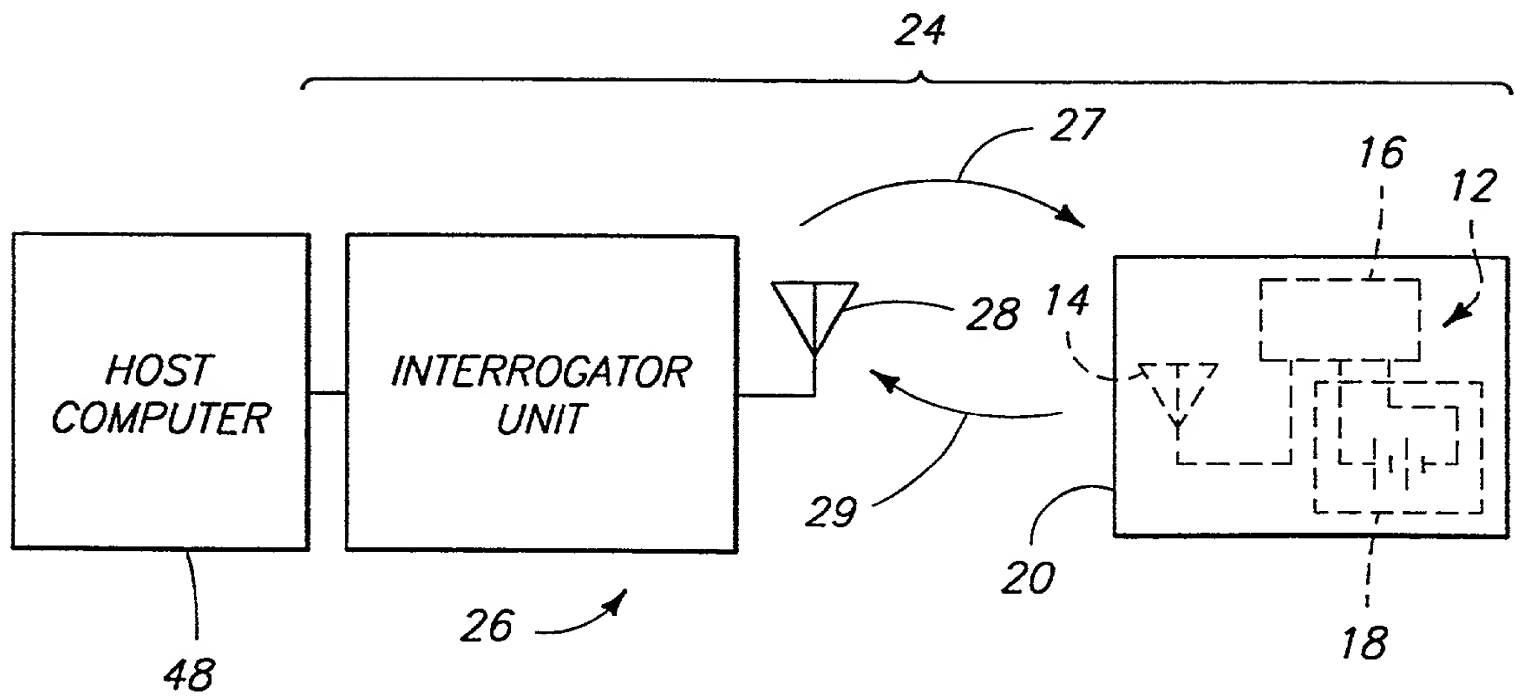
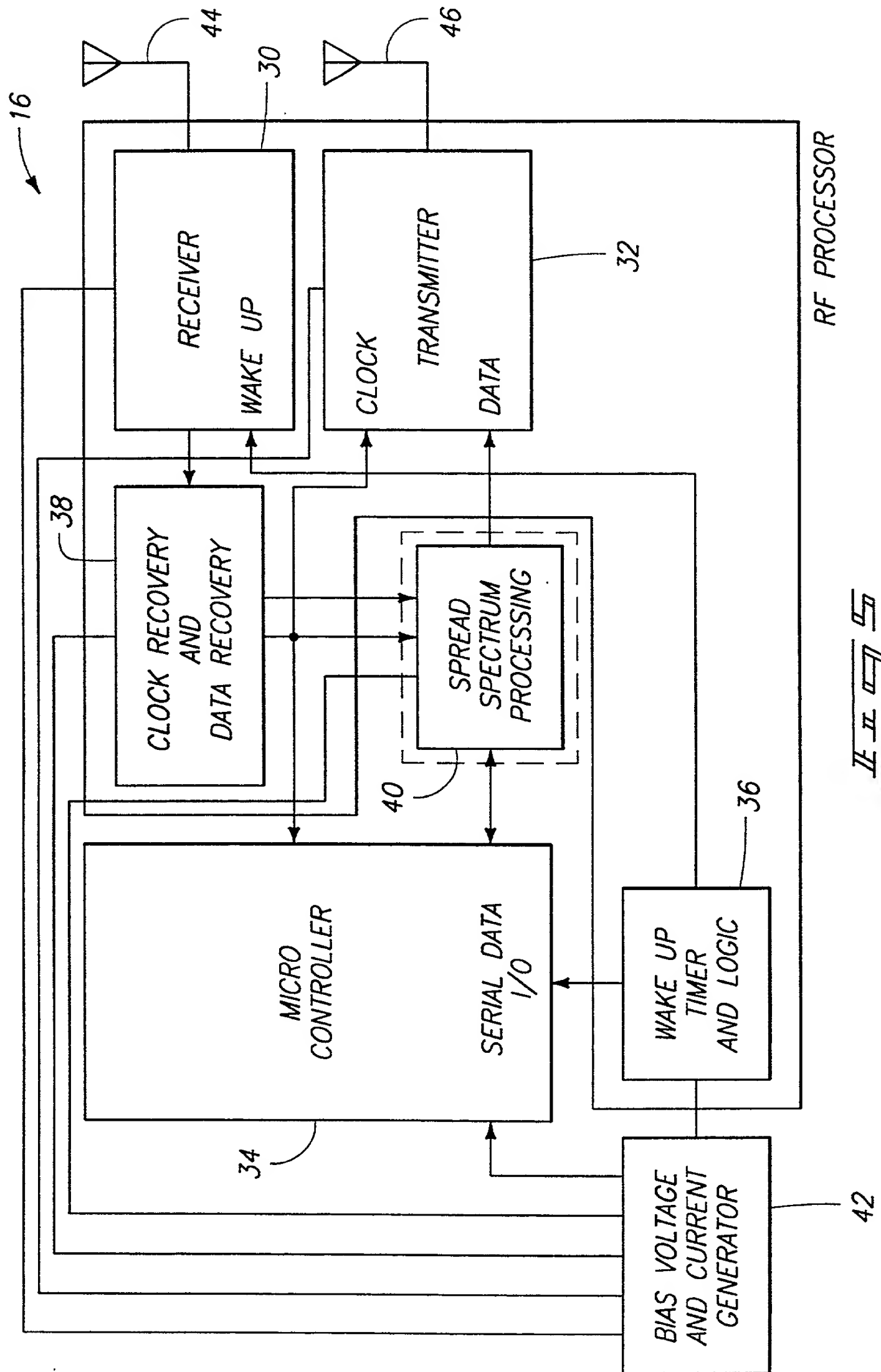
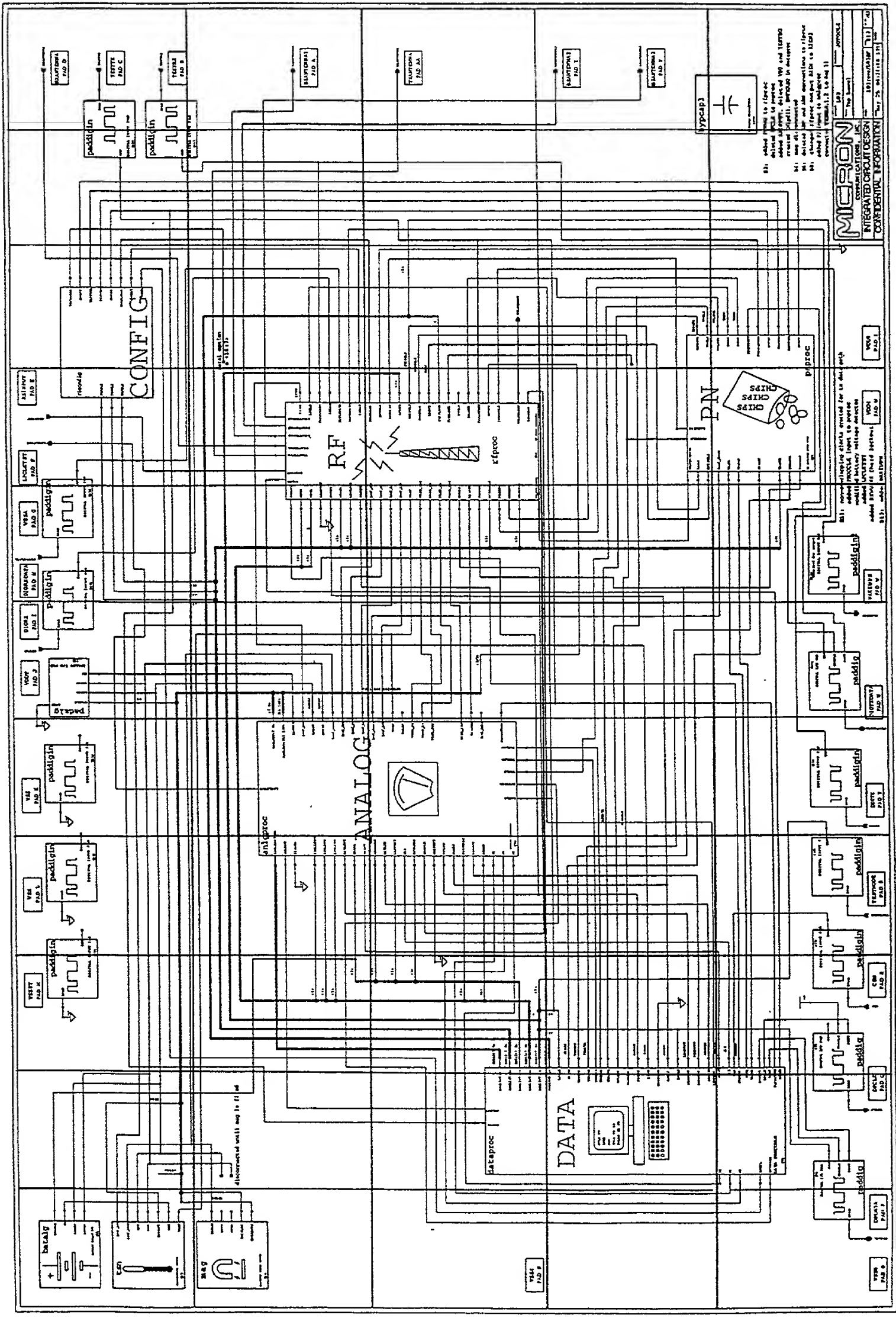


FIG. 2



6AA	6AB	6AC	6AD	6AE	6AF	6AG	6AH	6AI	6AJ	6AK
6BA	6BB	6BC	6BD	6BE	6BF	6BG	6BH	6BI	6BJ	6BK
6CA	6CB	6CC	6CD	6CE	6CF	6CG	6CH	6CI	6CJ	6CK
6DA	6DB	6DC	6DD	6DE	6DF	6DG	6DH	6DI	6DJ	6DK
6EA	6EB	6EC	6ED	6EE	6EF	6EG	6EH	6EI	6EJ	6EK

FIG. 6AA-EK



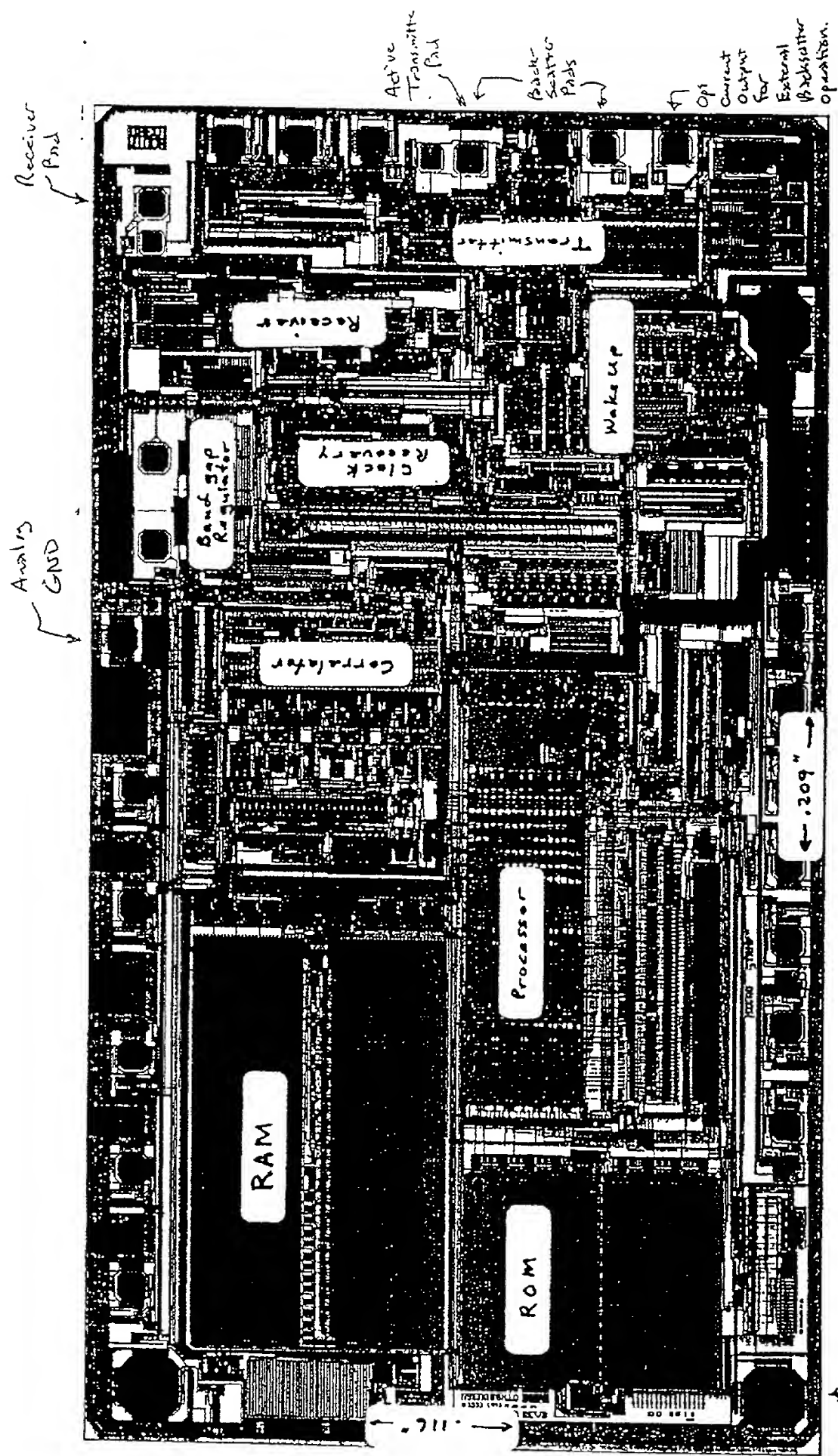
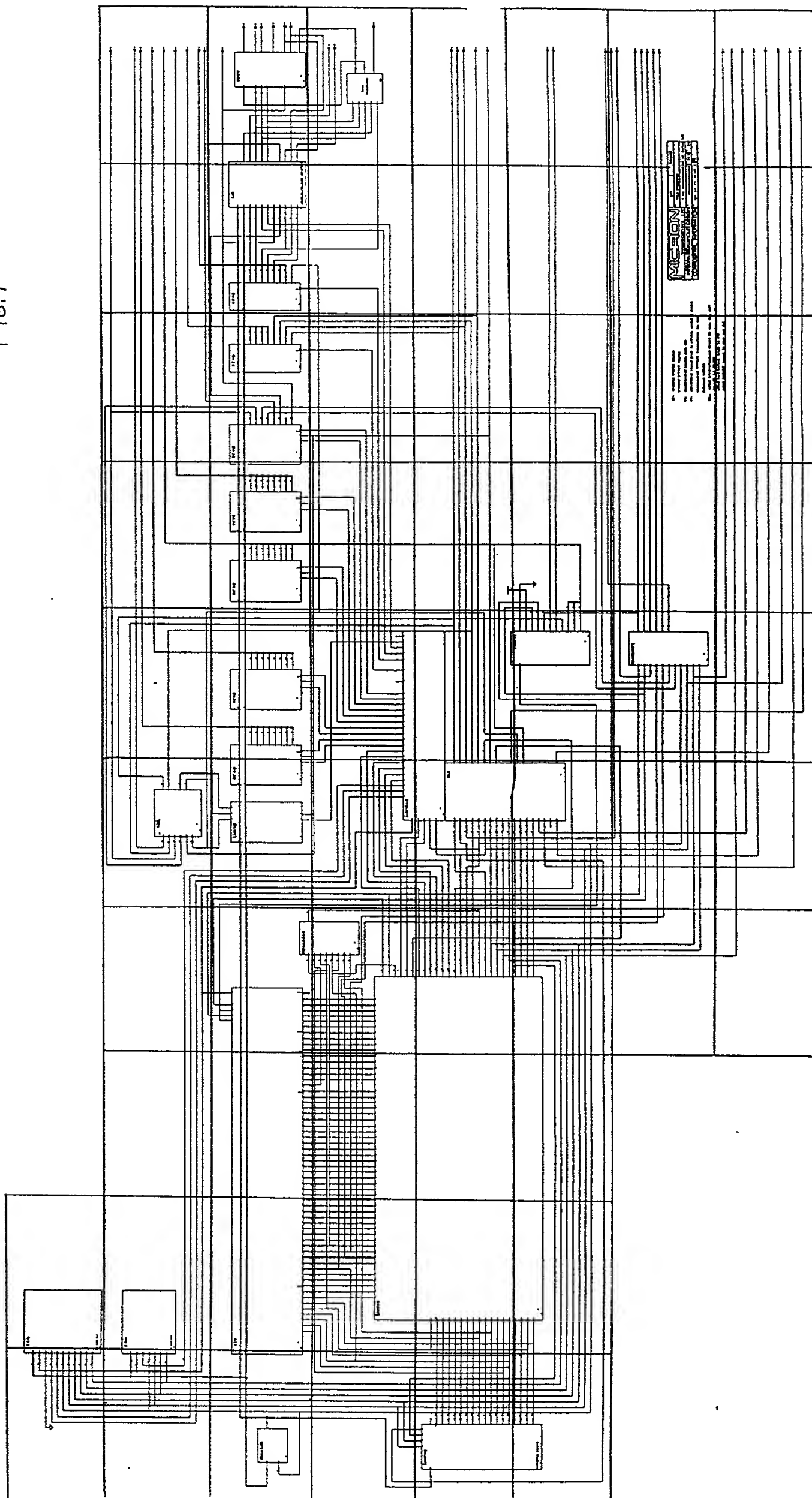


Fig. 6.01

FIG. 16.7

FIG. 16.7



7.01AA	7.01AB
7.01BA	7.01BB

7.0101AA	7.0101AB
7.0101BA	7.0101BB

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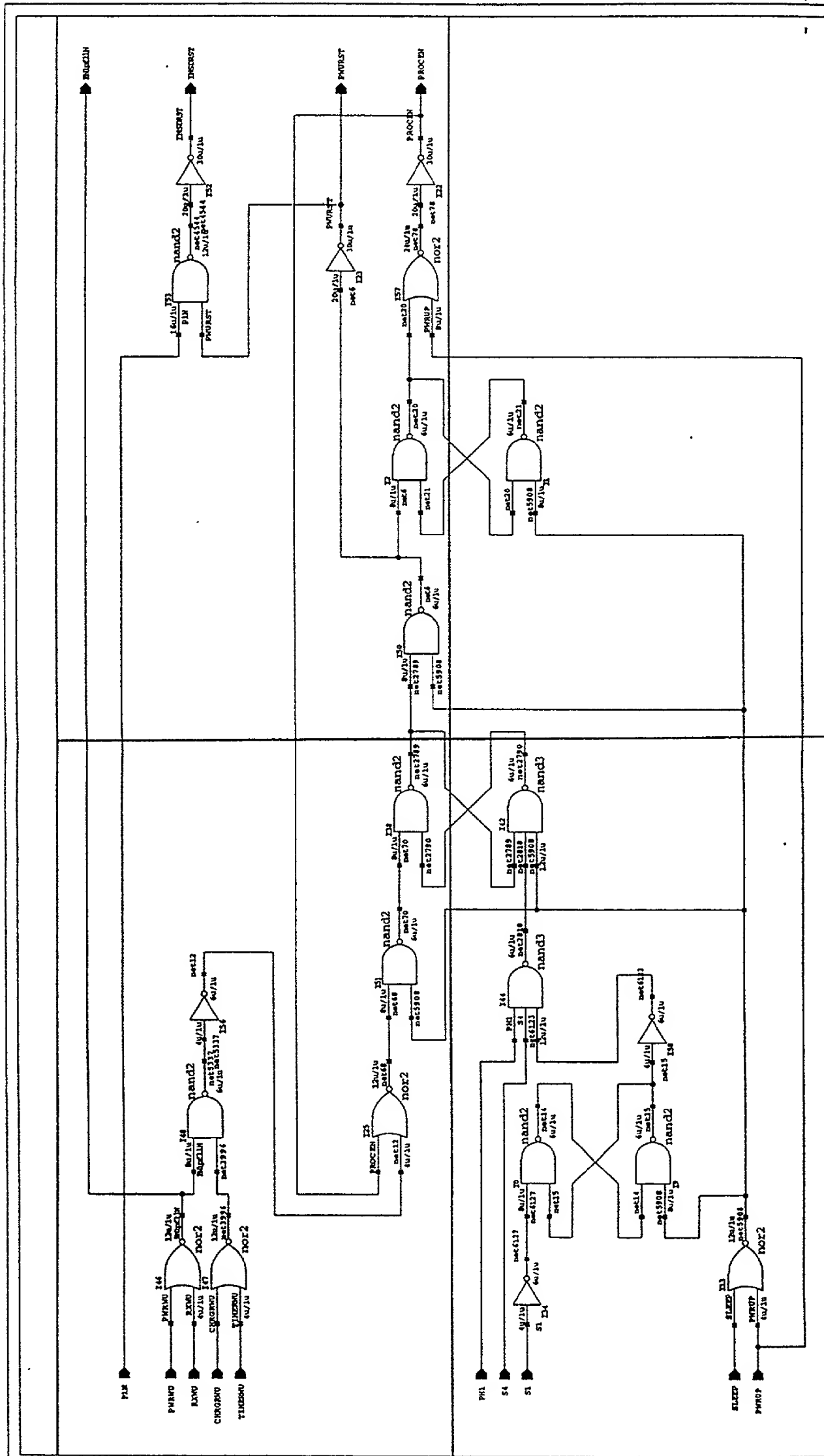


Fig. 7.0101

MICRON		PROCESSOR L03	REVISION	REVISION
COMMUNICATIONS, INC.		Processor Clock Controller		
INTEGRATED CIRCUIT DESIGN		DATE	1000000/000000	REV B2
CONFIDENTIAL INFORMATION		DATE	JUL 26 11:15:27 1995	REV B2

B2: created ENPBLIN signal

7.0102BA	7.0102BB	7.0102BC	7.0102BD	7.0102BE	7.0102BF	7.0102AG	7.0102AH	7.0102AI	7.0102AJ
7.0102CA	7.0102CB	7.0102CC	7.0102CD	7.0102CE	7.0102CF	7.0102CG	7.0102CH	7.0102CI	7.0102CJ
7.0102DA	7.0102DB	7.0102DC	7.0102DD	7.0102DE	7.0102DF	7.0102DG	7.0102DH	7.0102DI	7.0102DJ

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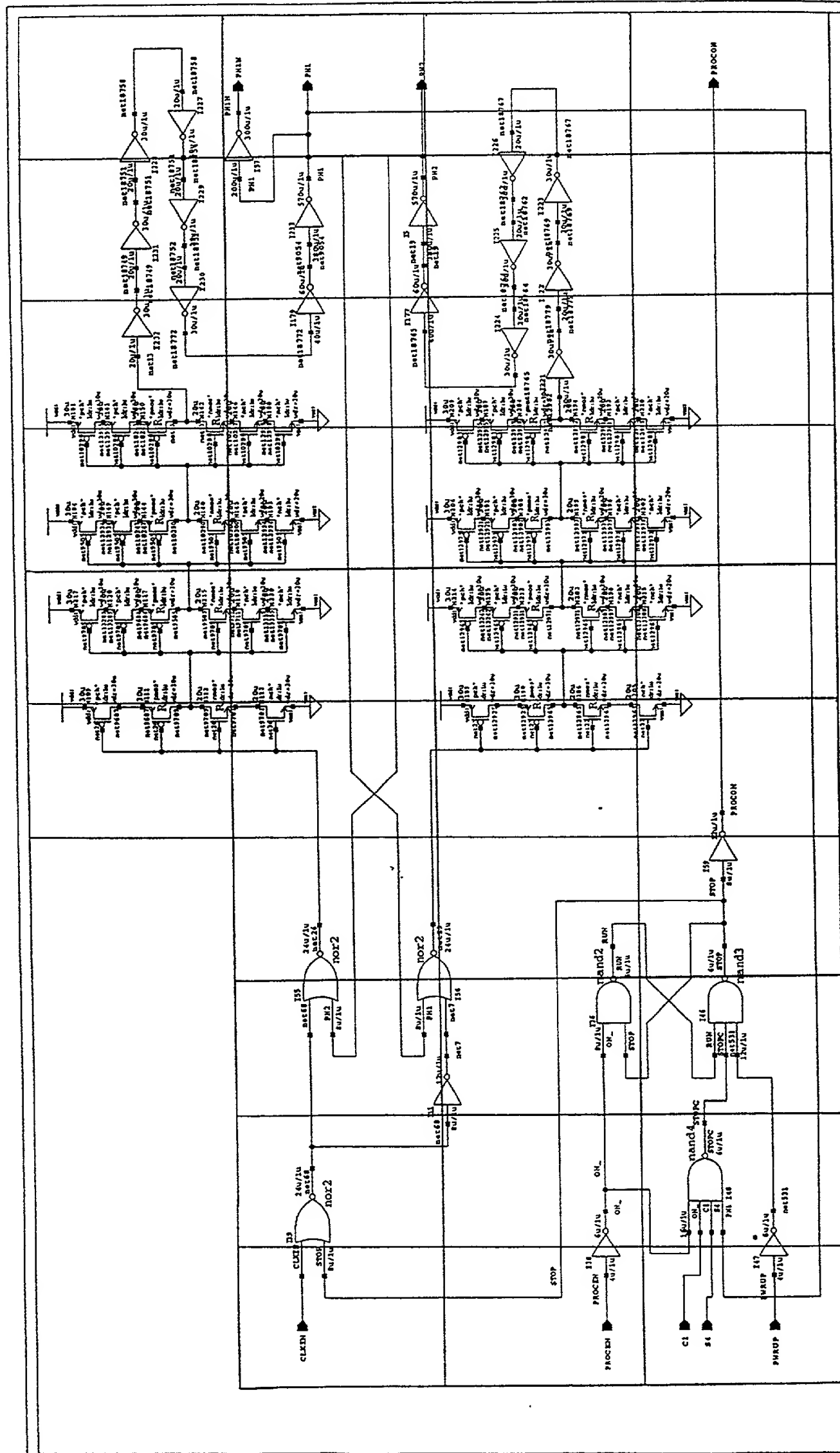


Fig. 7.0102

MICRON		PROJECT: L03	REVISION: Rev2011
COMMUNICATIONS, INC.		TITLE: Processor Phase Generator	
INTEGRATED CIRCUIT DESIGN		2-Phase Non-overlapping	
CONFIDENTIAL INFORMATION		DATE: 10/19/94	BY: B8
		DATE: Dec 5 17:55:56 1995	BY: ml

B2: Pin name changes
 B8: Added 6 inverters to non-overlap time
 Make the number of inverters adjustable on metal

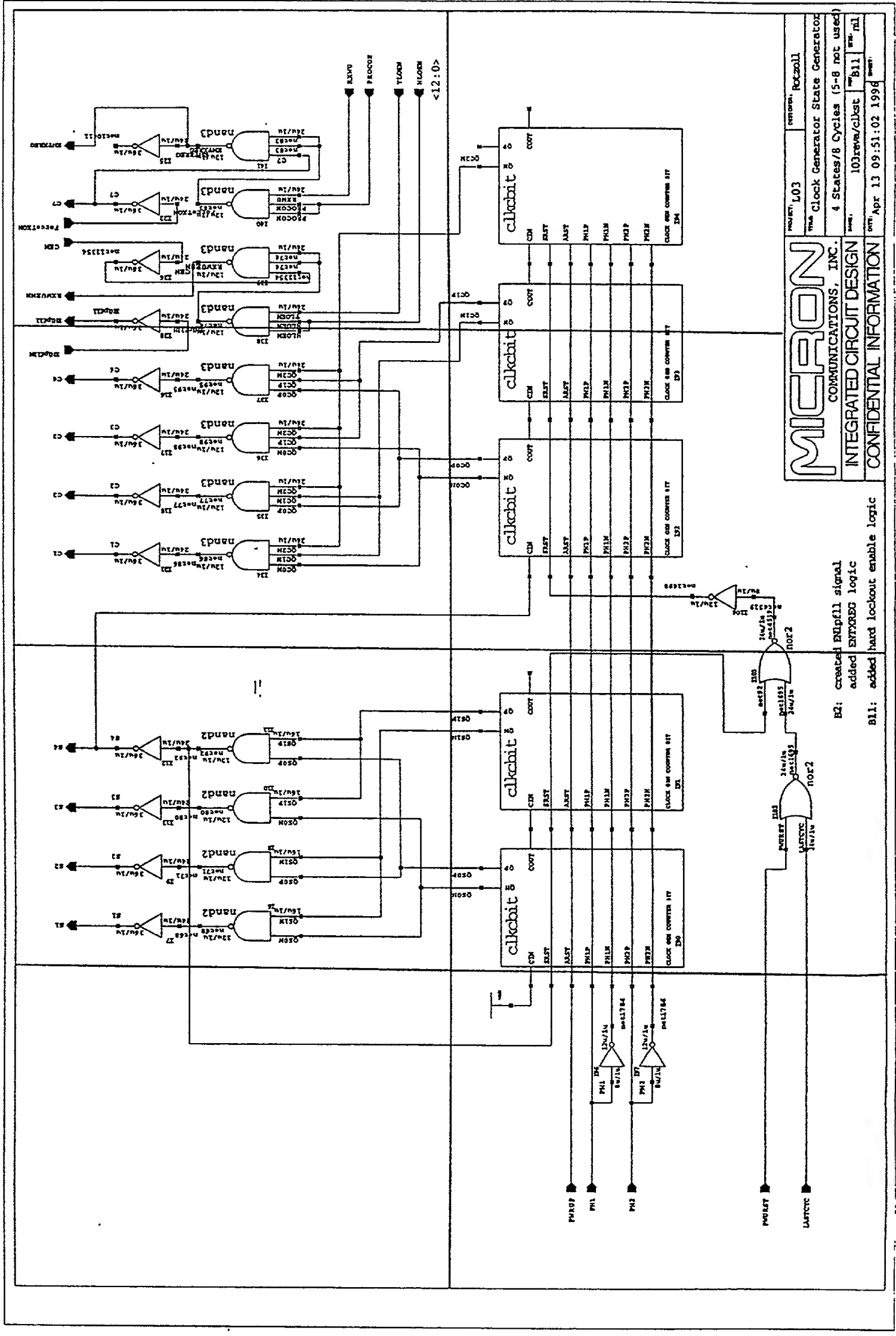
MI40-030

MI40-030

7.0103AA	7.0103AB	7.0103AC	7.0103AD	7.0103BD
7.0103BA	7.0103BB	7.0103BC		

MI40-030

FIG. 7.0103



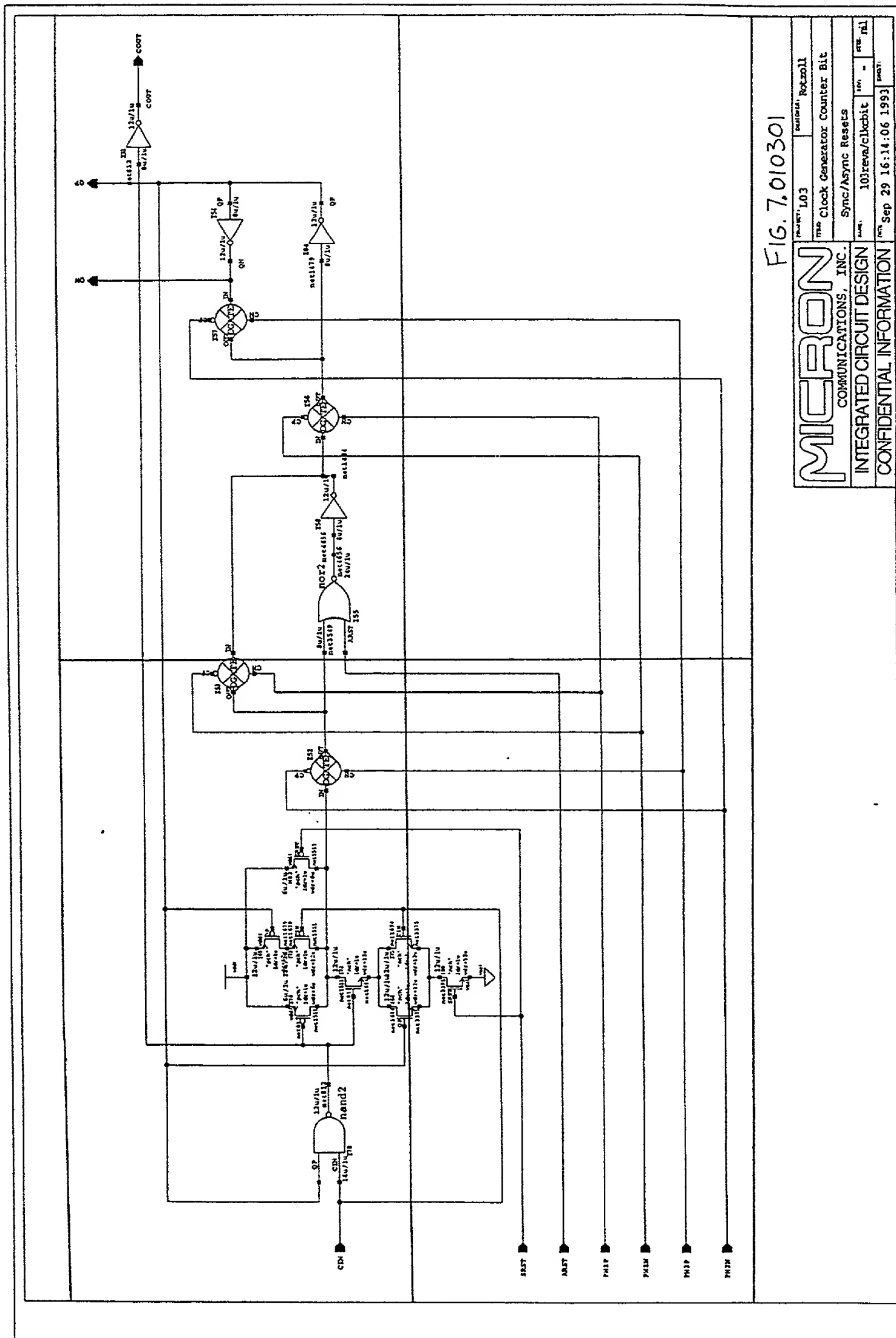
PROJECT: L03		REVISION: R02001
Clock Generator State Generator		
4 States/8 Cycles (5-8 not used)		
DATE:	103rev/clkst	B11
DATE:	Apr 13 09:51:02 1998	DATE:

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

B2: created ENUP11 signal
added ENTREG logic
B11: added hard lockout enable logic

THEO. L. L.

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7.02AA	7.02AB	7.02AC	7.02AD	7.02AE	7.02AF
7.02BA	7.02BB	7.02BC	7.02BD	7.02BE	7.02BF

CONFIDENTIAL INFORMATION

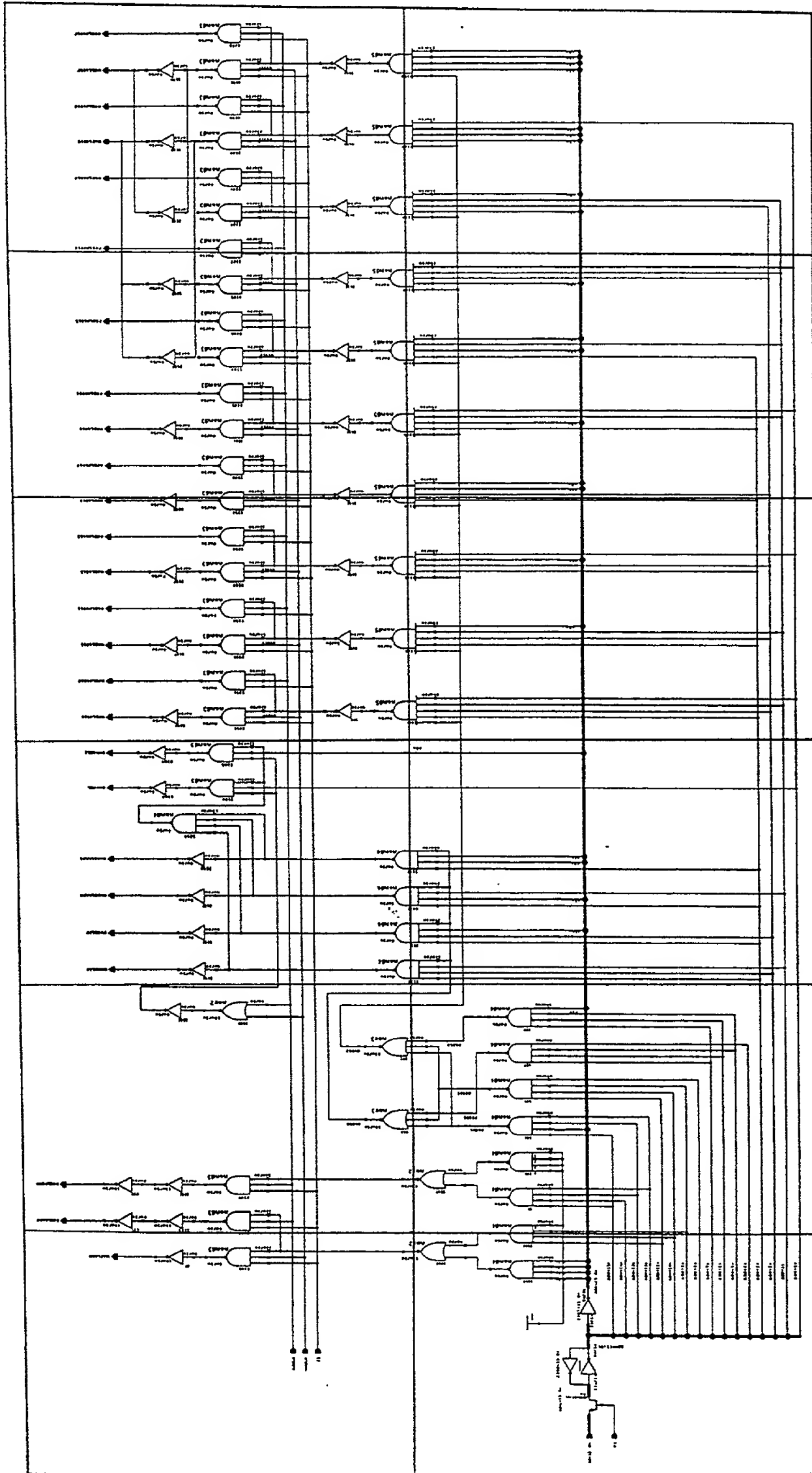


FIG. 7.02

MICRON		Address Decoder	Address Decoder
INTEGRATED CIRCUIT DESIGN		Address Decoder	Address Decoder
CONFIDENTIAL INFORMATION		Address Decoder	Address Decoder

BE 1981 used drive of memory and status

7.03AA	7.03AB	7.03AC	7.03AD	7.03AE	7.03AF	7.03AG	7.03AH
7.03BA	7.03BB	7.03BC	7.03BD	7.03BE	7.03BF	7.03BG	7.03BH
7.03CA	7.03CB	7.03CC	7.03CD	7.03CE	7.03CF	7.03CG	7.03CH
7.03DA	7.03DB	7.03DC	7.03DD	7.03DE	7.03DF	7.03DG	7.03DH
7.03EA	7.03EB	7.03EC	7.03ED	7.03EE	7.03EF	7.03EG	7.03EH

FIG. 7.03

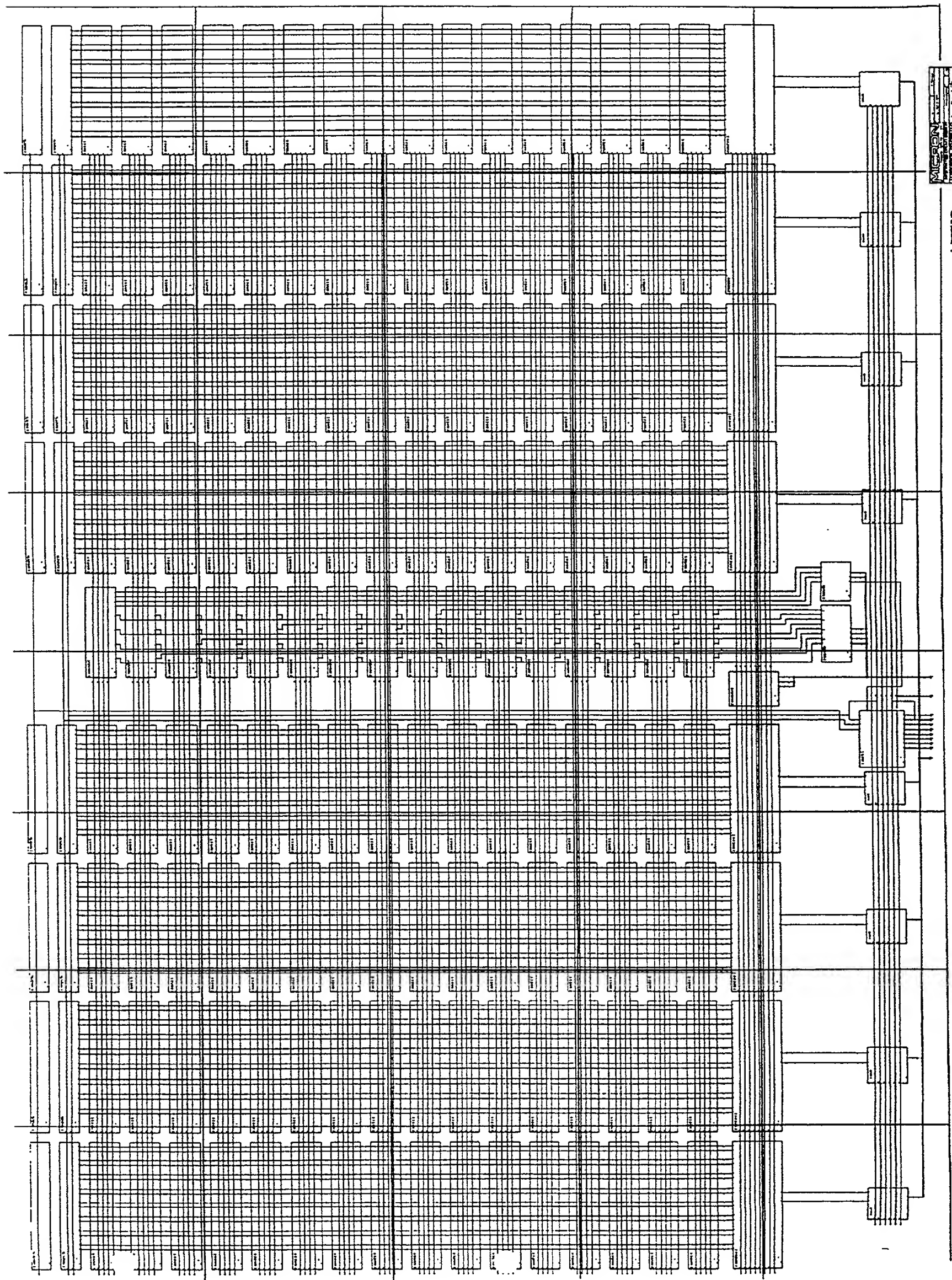


Fig 7.03

7.0301AA	7.0301AB
7.0301BA	7.0301BB

II II II II II II II II

100% design check complete 03/03/94
100% layout check complete 03/03/94
100% test plan complete 03/03/94

RAMCTL 100

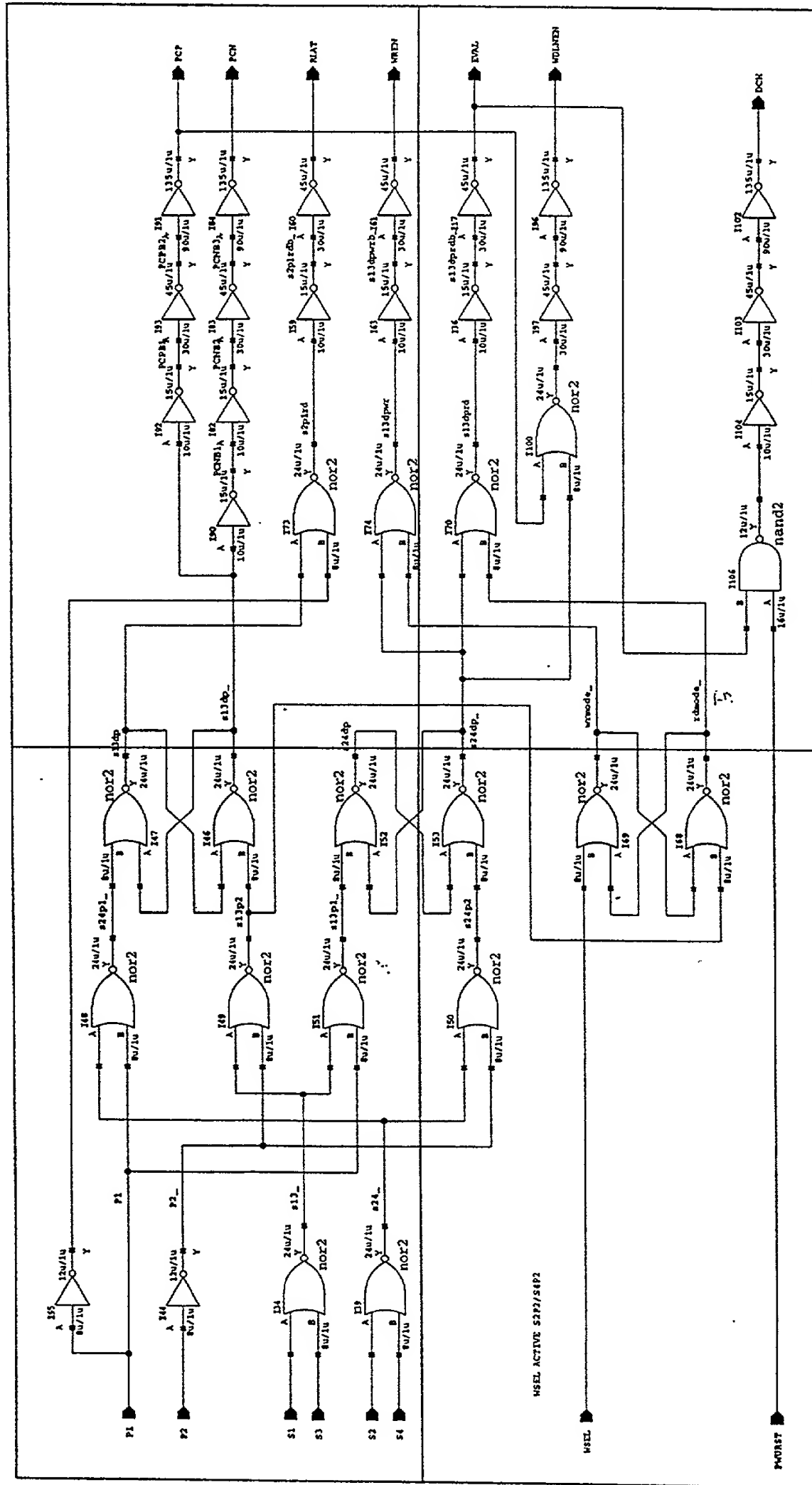


Fig. 7.0301

MICRON		PRODUCT L03	AP3	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE RAM Control		
INTEGRATED CIRCUIT DESIGN		DATE: 103reva/ramctl	REV: -	SHEET: 1 of 1
CONFIDENTIAL INFORMATION		DATE: Feb 11 16:47:36 1994		

7.0302AB

7.0302AC

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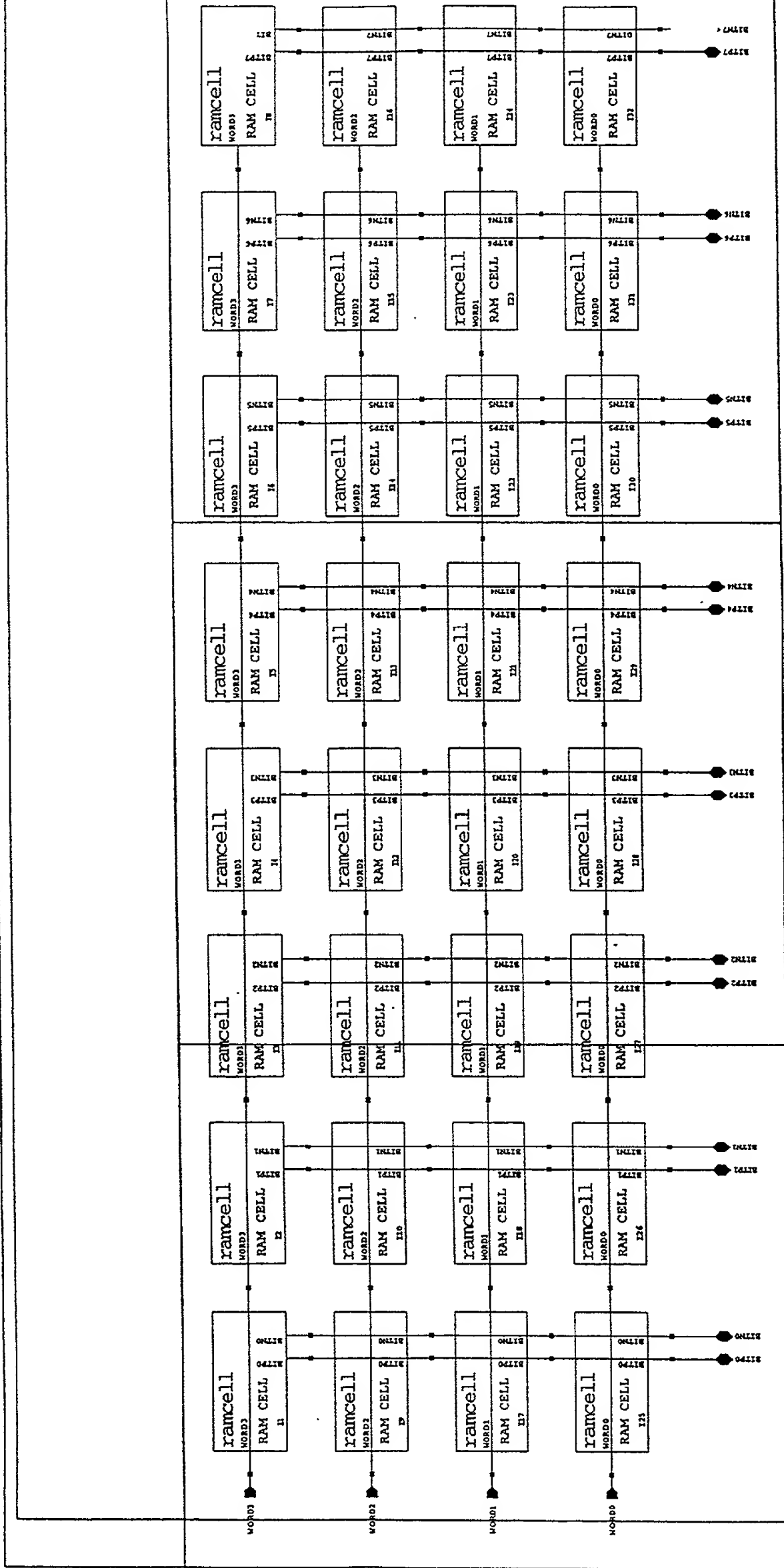


Fig. 7.0302

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PRINT: L03
TITLE: 8x4 RAM Array
DATE: 103rev0/ram8x4
REV: -
BY: ml
DATE: Nov 6 11:34:37 1993
PAGE: 0002

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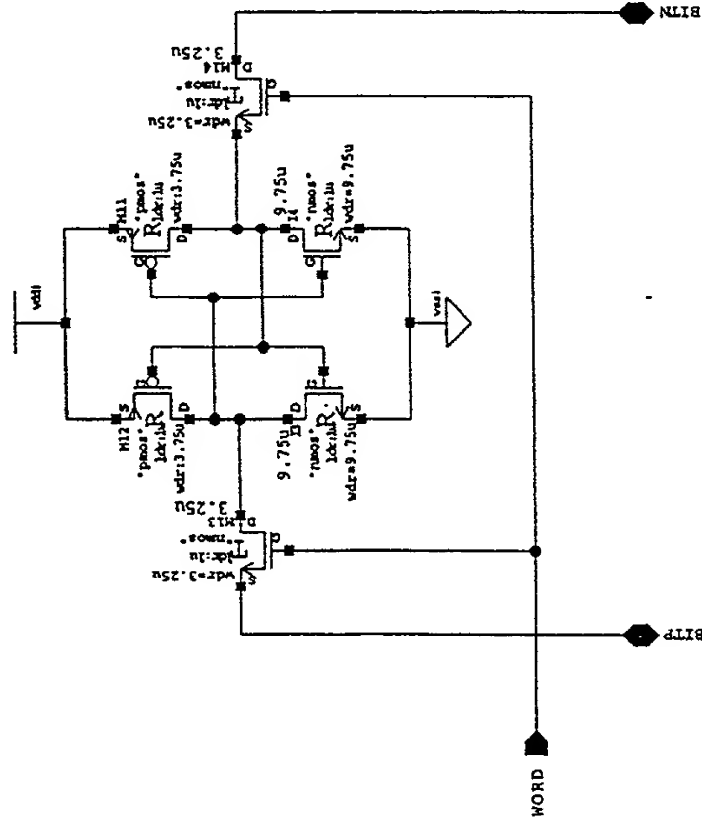


Fig. 7.030201

MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: 6T RAM Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/ramcell	REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 6 11:34:48 1993	SIZE: A
		SHEET:	

7.0303AA	7.0303AB	7.0303AC	7.0303AD
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ITEM. 11

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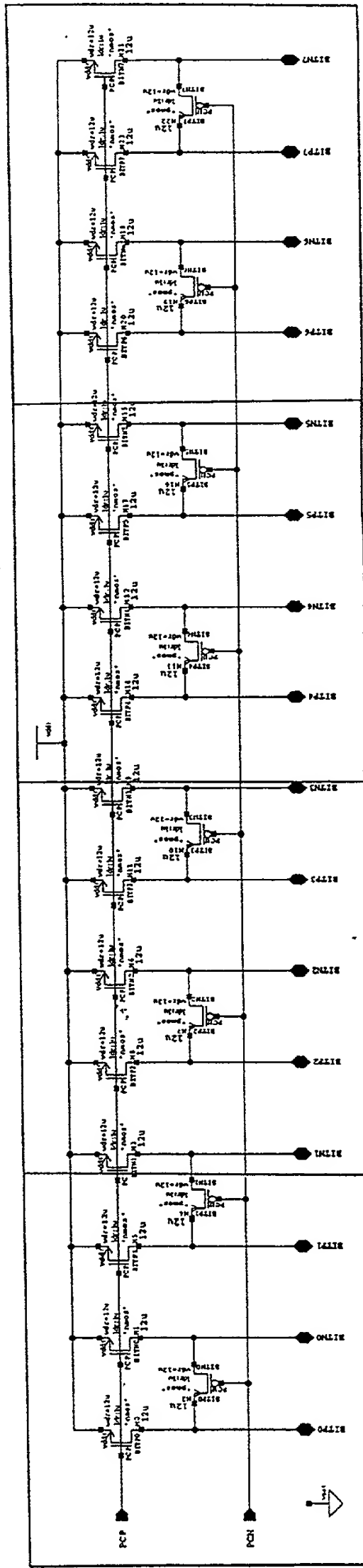


FIG. 7.0303

MICRON		DESIGNER: Rotzoll
COMMUNICATIONS, INC.		DATE: 103reva/rampch
INTEGRATED CIRCUIT DESIGN		REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 12 02:58:36 1993

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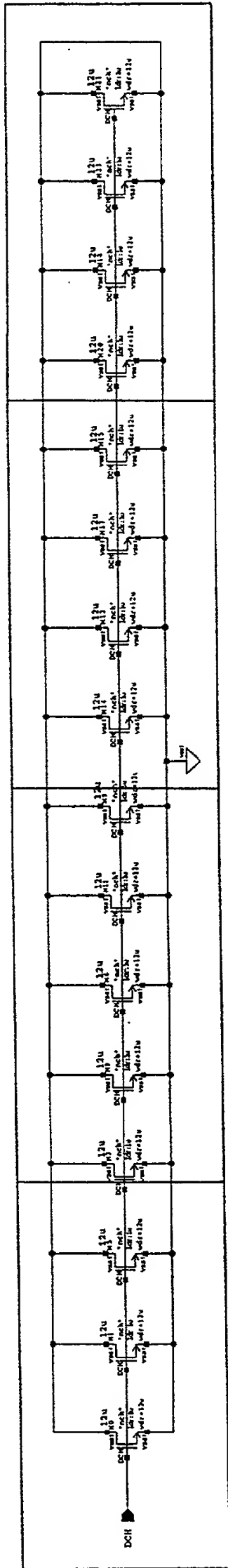
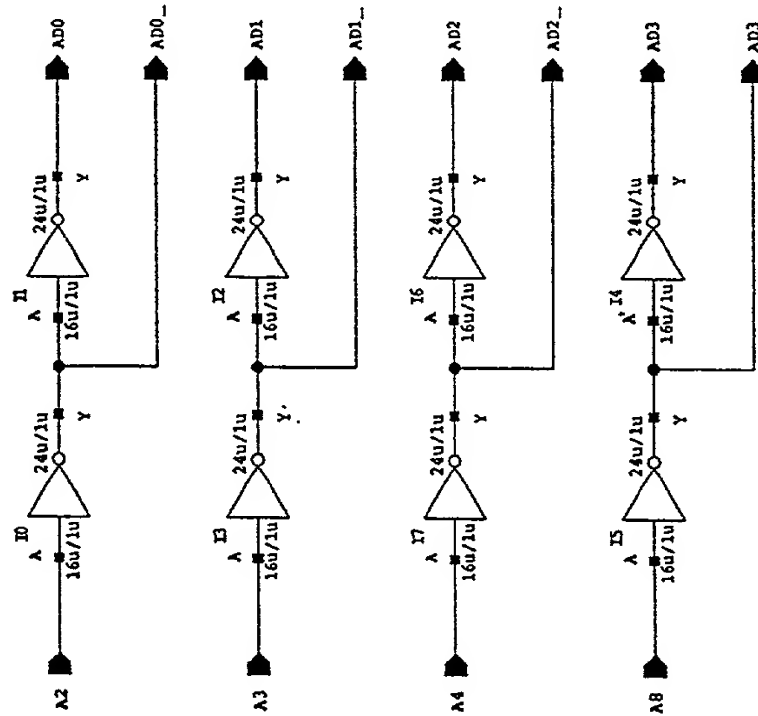


FIG. 70304

MICRON COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN CONFIDENTIAL INFORMATION	PROJECT: L03	DESIGNER: JOTOOLE
	TITLE: RAM Precharge	
	DATE: 103reva/randch	REV: B0
DATE: Jan 28 09:51:27 1996		FILE: ml

B8: disconnected dch devices from bit lines and tied to vss

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MICRON COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN CONFIDENTIAL INFORMATION	PROJECT: L03	DESIGNER: Rotzoll
	TITLE: RAM Address Buffer	
	NAME: 103reva/ramadb	REV: - SIZE: A
	DATE: Sep 29 16:04:01 1993	

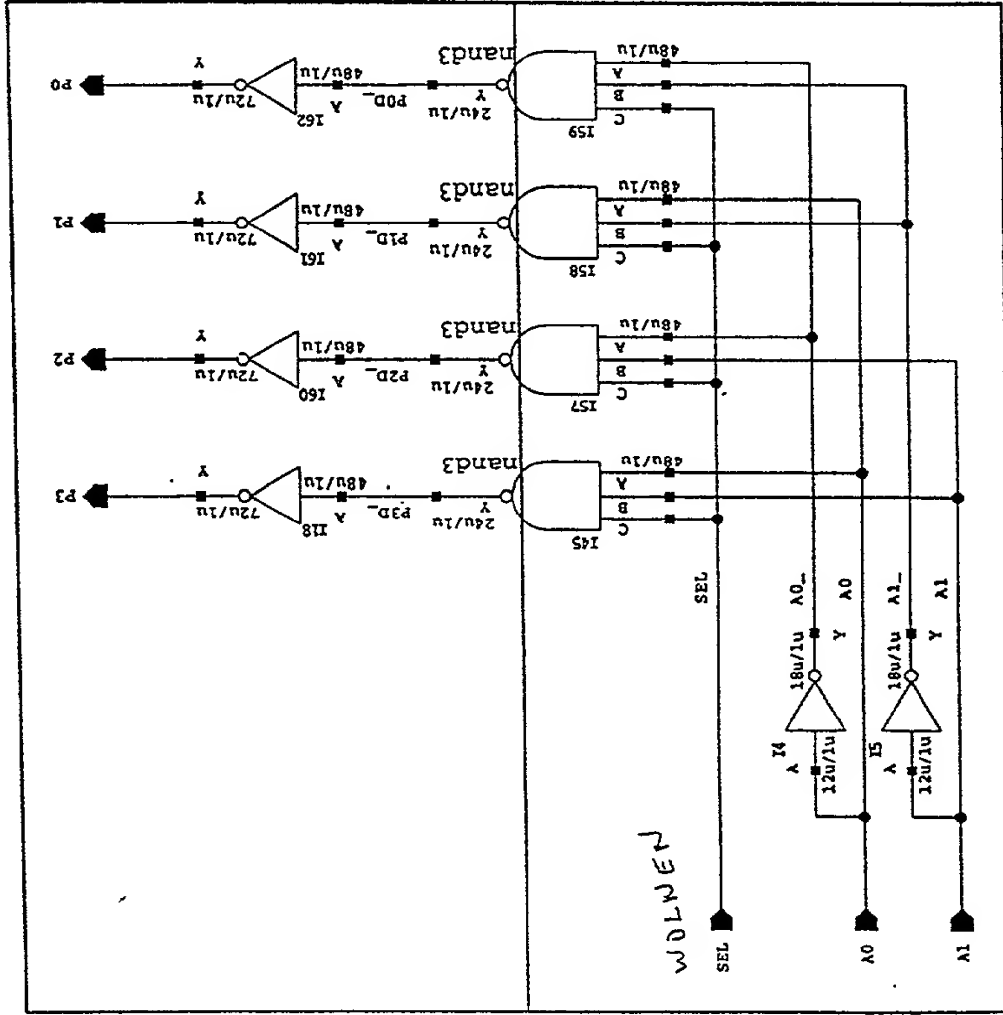
Fig. 7.0305

7.0306AA

7.0306BA

7.0306

FIG. 7.0306



MICRON COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: RAM Word Line Driver			
NAME:	103reva/ramwdr	REV: -	SIZE: A
DATE: Sep 29 16:04:16 1993		SHEET: 1	

FIG. 7.0306

7.0307BB

Итого 7.003007

7.0308AA

7.0308AB

7.0308BA

7.0308BB

7.0308BB

drawn: 10/10/93
checked: 10/10/93
approved: 10/10/93
date: 10/10/93
by: [signature]
for: [signature]

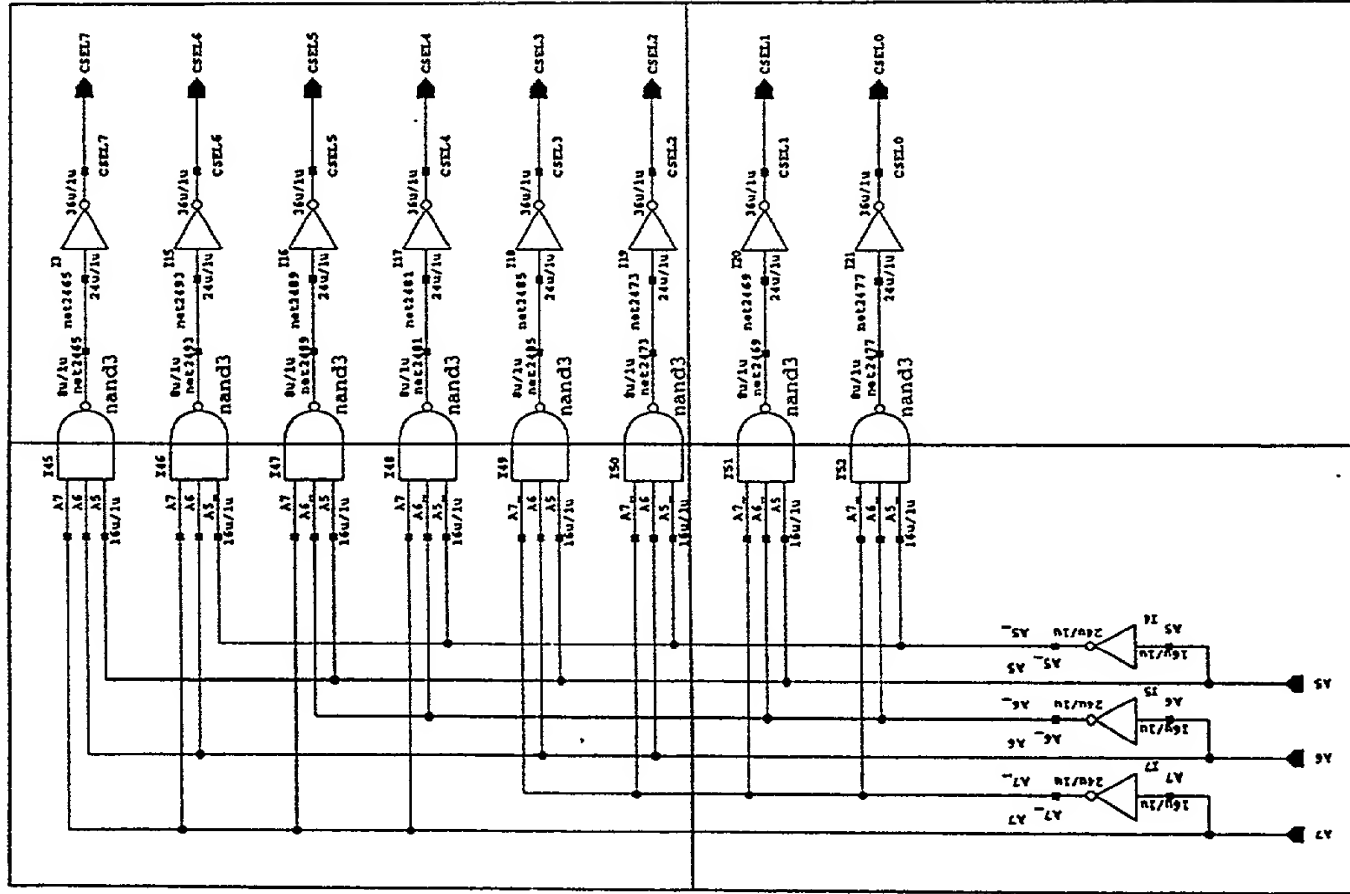


FIG. 7.0308

MICRON
COMMUNICATIONS, INC.

PRODUCT: L03
TITLE: RAM Column Select Decode
PAGE: 3 to 8
REV: -
DATE: Nov 5 17:21:07 1993

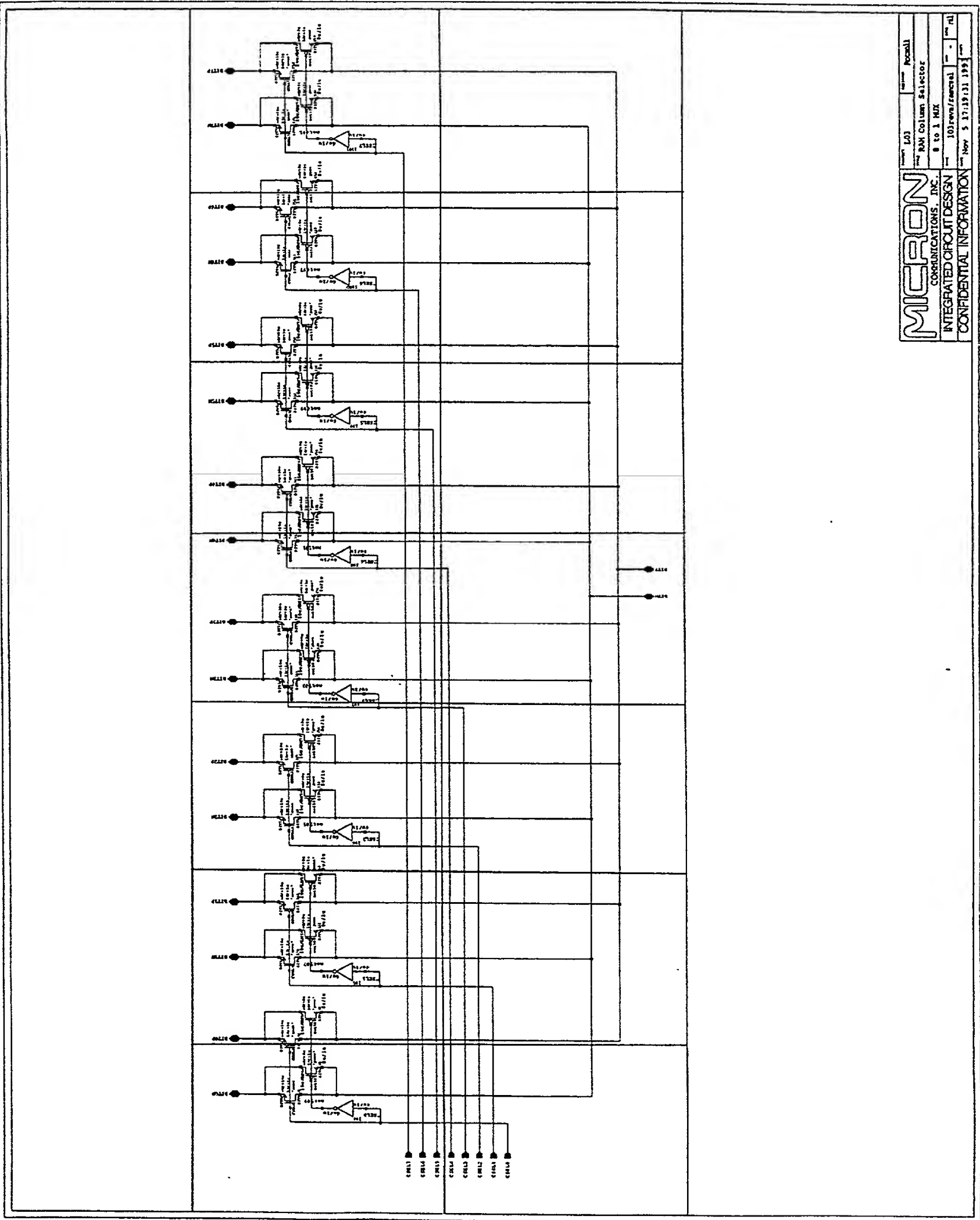
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION



7.0309AA	7.0309AB	7.0309AC	7.0309AD	7.0309AE	7.0309AF	7.0309AG
7.0309BA	7.0309BB	7.0309BC	7.0309BD	7.0309BE	7.0309BF	7.0309BG

SECRET

FIG. 7.0309



111

FIG. 7.0309

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Rev	103	Rev	103
RAM Column Selector			
8 to 1 MUX			
103 rows/selector			
Nov 5 11:13:13 1993			

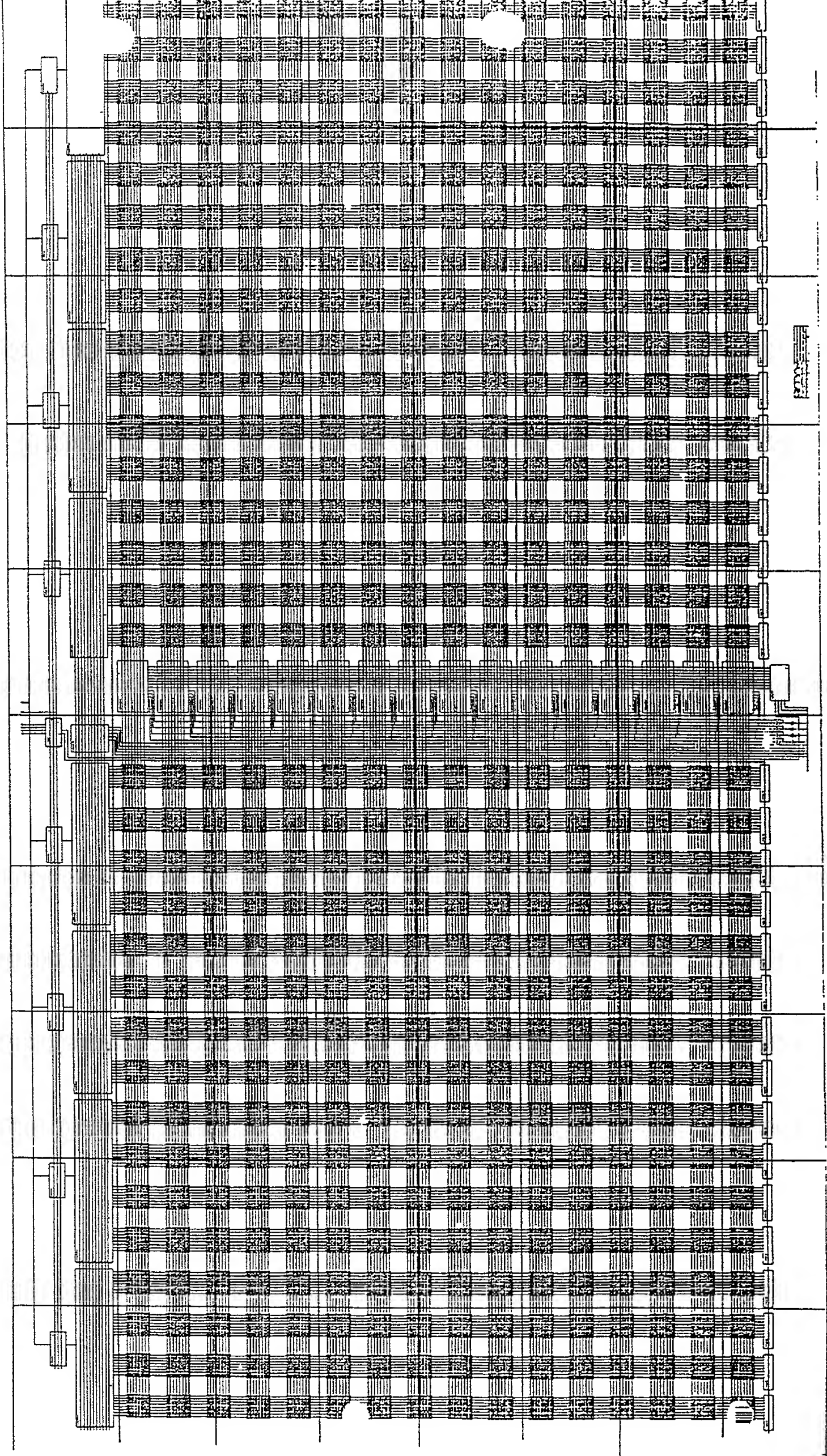
7.0310AA	7.0310AB
7.0310BA	7.0310BB

II II III III III III

7.04AA	7.04AB	7.04AC	7.04AD	7.04AE	7.04AF	7.04AG	7.04AH	7.04AI	7.04AJ
7.04BA	7.04BB	7.04BC	7.04BD	7.04BE	7.04BF	7.04BG	7.04BH	7.04BI	7.04BJ
7.04CA	7.04CB	7.04CC	7.04CD	7.04CE	7.04CF	7.04CG	7.04CH	7.04CI	7.04CJ
7.04DA	7.04DB	7.04DC	7.04DD	7.04DE	7.04DF	7.04DG	7.04DH	7.04DI	7.04DJ
7.04EA	7.04EB	7.04EC	7.04ED	7.04EE	7.04EF	7.04EG	7.04EH	7.04EI	7.04EJ
7.04FA	7.04FB	7.04FC	7.04FD	7.04FE	7.04FF	7.04FG	7.04FH	7.04FI	7.04FJ
7.04GA	7.04GB	7.04GC	7.04GD	7.04GE	7.04GF	7.04GG	7.04GH	7.04GI	7.04GJ
7.04HA	7.04HB	7.04HC	7.04HD	7.04HE	7.04HF	7.04HG	7.04HH	7.04HI	7.04HJ

FIG. 7.04

FIG. 7.04



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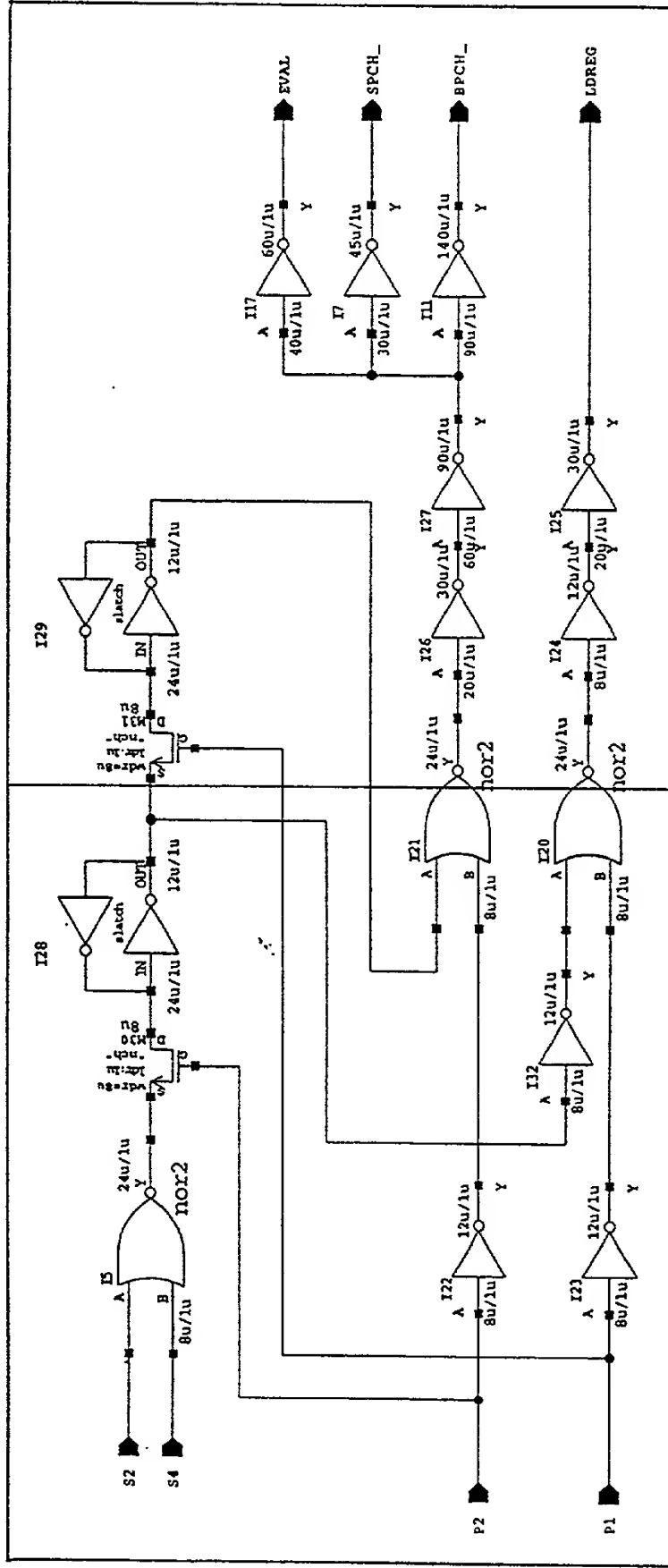


Fig. 7.0401

PRODUCT: L03		DESIGNER: Rotzoll	
TITLE: ROM Control Logic			
NAME:	103reva/ronct1	REV:	-
DATE:	Oct 3 13:16:28 1993	SIZE:	A
CONFIDENTIAL INFORMATION		SHEET:	

7.0402AA

7.0402AB

EX-100-1000

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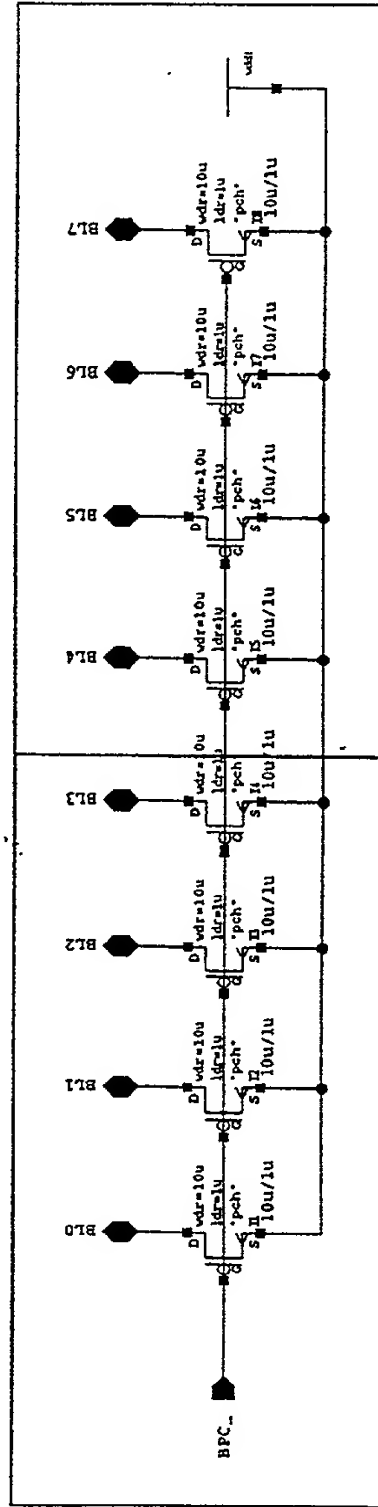


FIG. 7.0402

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: ROM Bit Line Precharge			
NAME: 103reva/rompach		REV: -	SIZE: A
DATE: Oct 7 18:09:48 1993		SHEET:	

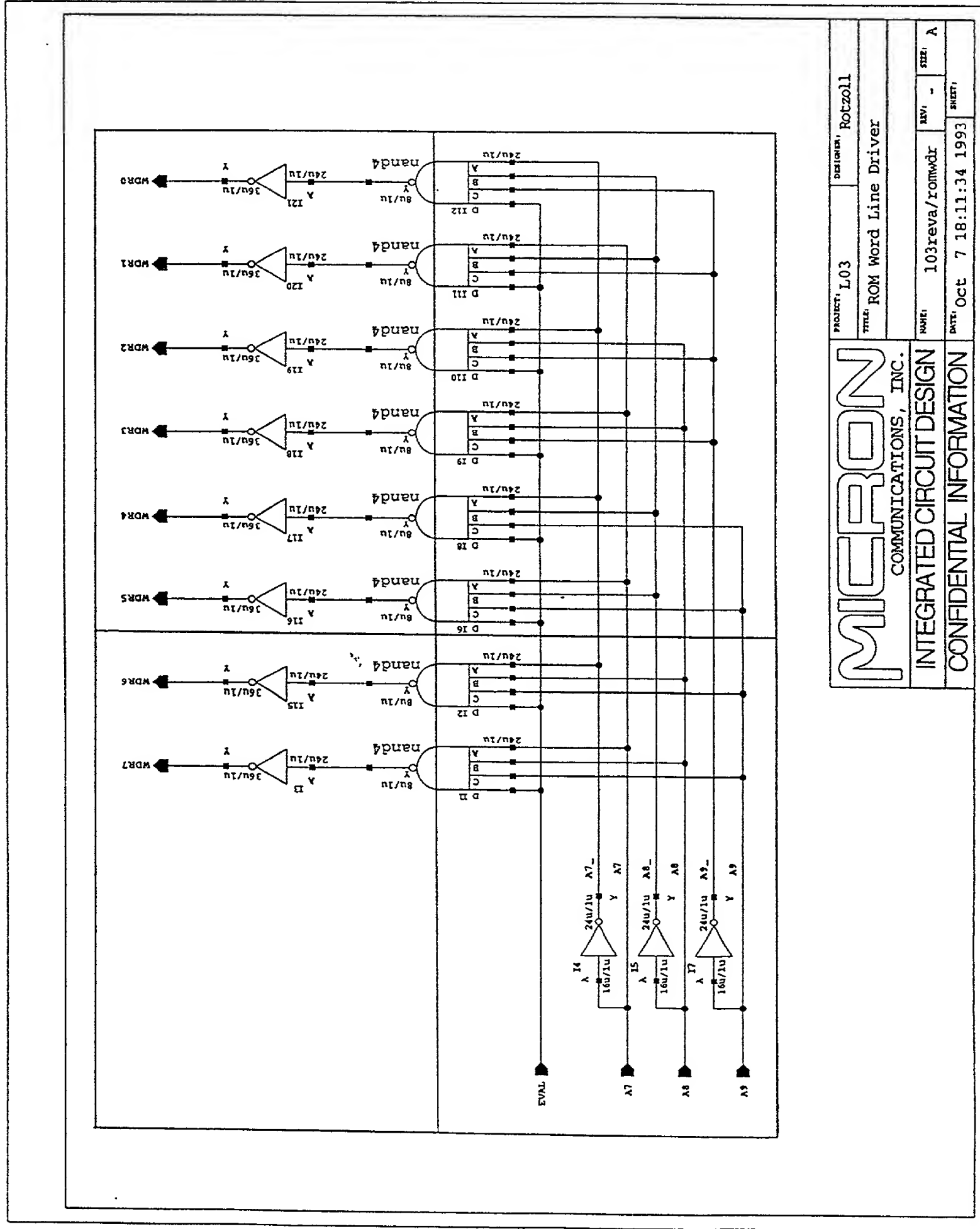
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

7.0403AA	7.0403AB
7.0403BA	7.0403BB

EE MI40-030

FIG. 7.0903

FIG. 7.0903



	7.0404AB	7.0404AC
7.0404BA	7.0404BB	7.0404BC
	7.0404CB	7.0404CC
	7.0404DB	7.0404DC

II II II 7.0404 0404

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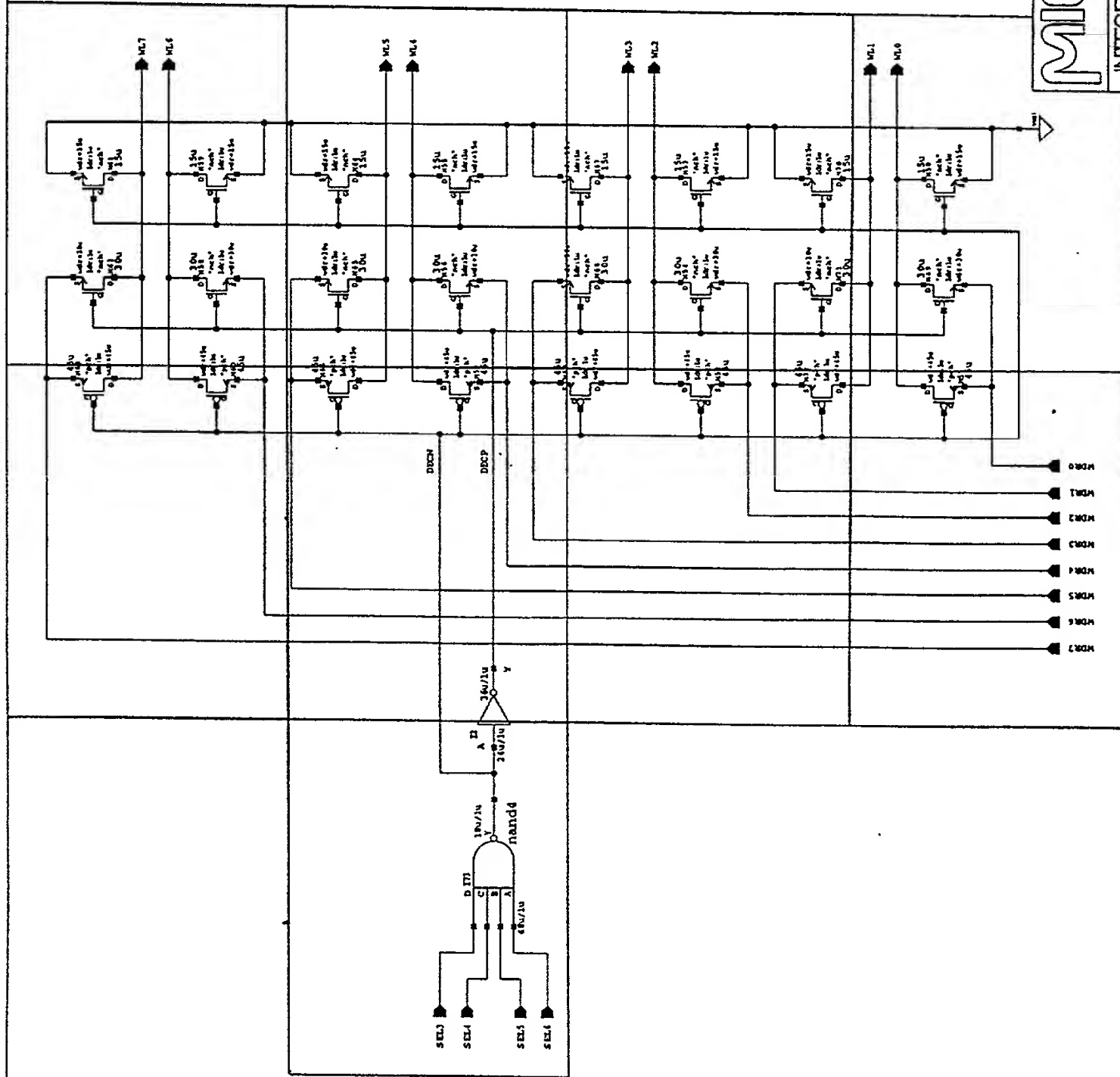


FIG. 7.0A04

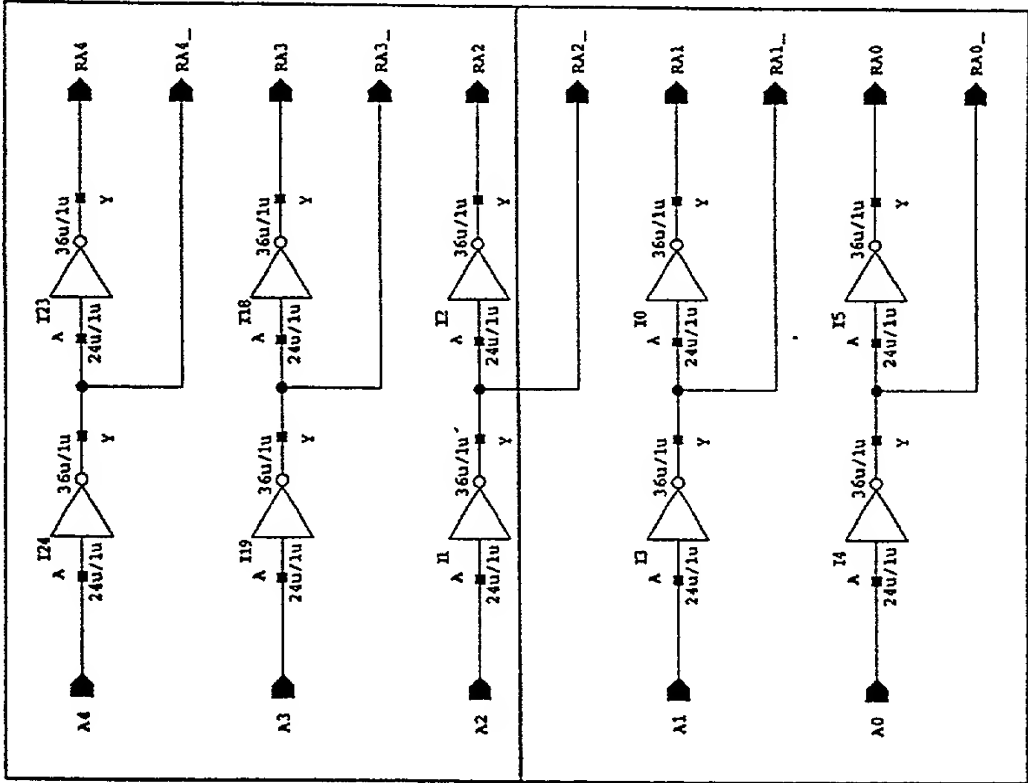
MICRON		PROJECT: L03	DESIGNER: ROZZOLI
COMMUNICATIONS, INC.		TITLE: Word Block Decoder	
INTEGRATED CIRCUIT DESIGN		REV: 103revA/romwdec_rev	DATE: Nov 5 17:38:09 1993
CONFIDENTIAL INFORMATION		NOV -	REL

7.0405AA

7.0405BA

7.0405

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DATE 08-01-2001 BY 60322 UCBAW/SJS



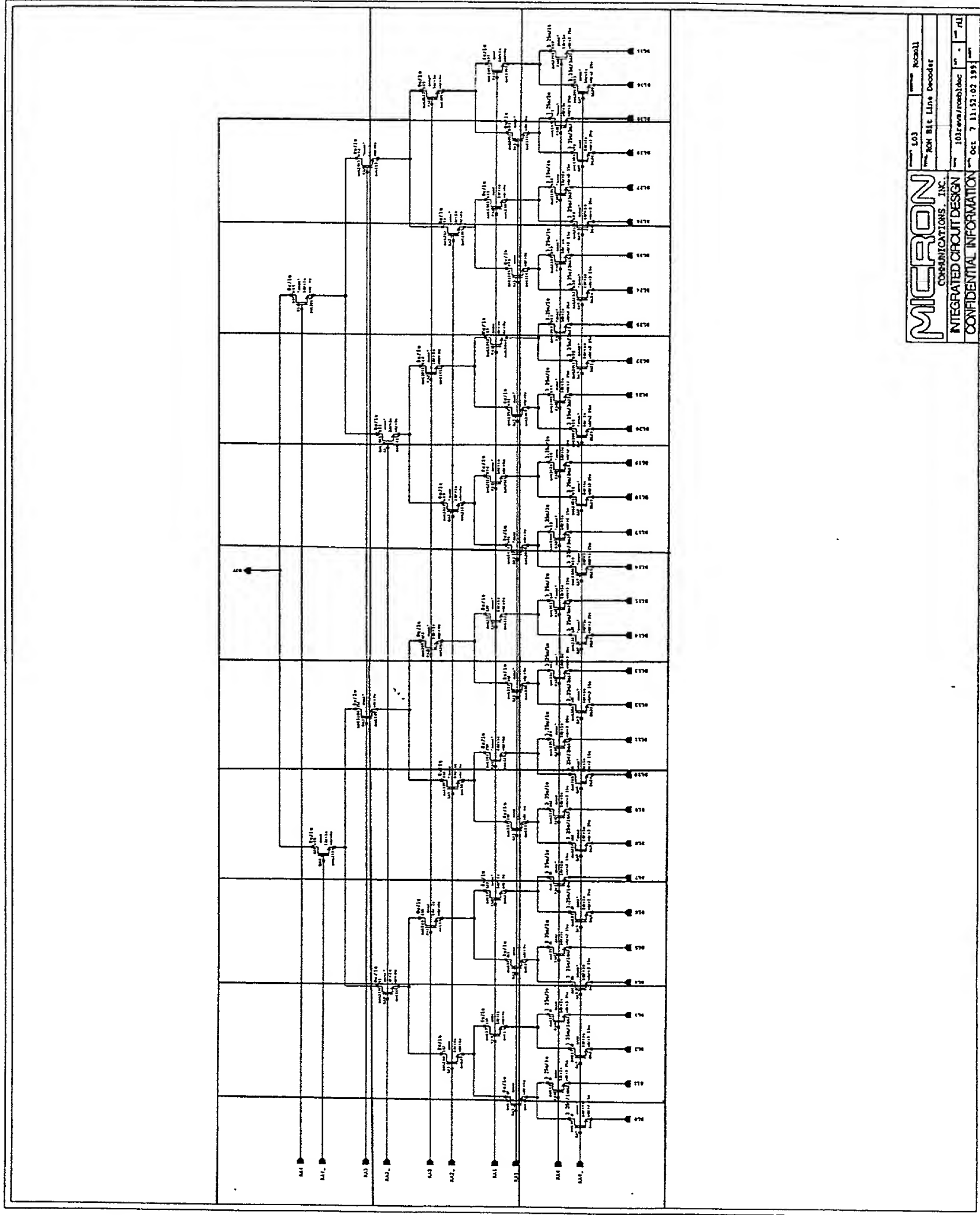
MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ROM Bit Line Address Driver	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/rombldr	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 7 12:08:42 1993	SHEET: A

FIG. 7.0405

7.0406AA	7.0406AB	7.0406AC	7.0406AD	7.0406AE	7.0406AF	7.0406AG	7.0406AH	7.0406AI	7.0406AJ	
7.0406BA	7.0406BB	7.0406BC	7.0406BD	7.0406BE	7.0406BF	7.0406BG	7.0406BH	7.0406BI	7.0406BJ	7.0406BK
7.0406CA	7.0406CB	7.0406CC	7.0406CD	7.0406CE	7.0406CF	7.0406CG	7.0406CH	7.0406CI	7.0406CJ	7.0406CK

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101

FIG. 7.0406

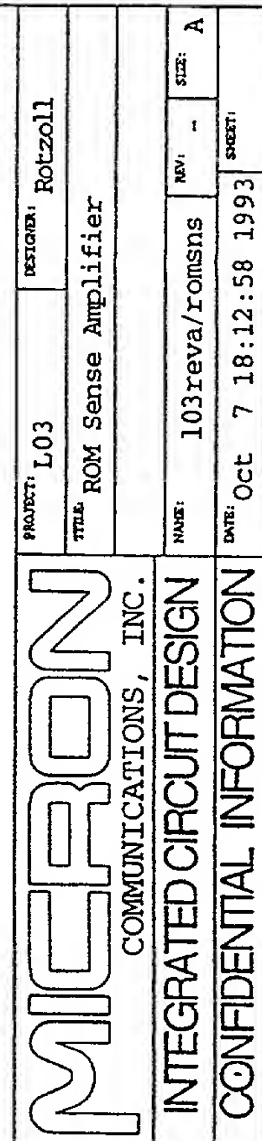
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Oct 7 11:52:03 1993

7.0407AB

LETT. E. E.

FIG. 7.0407



PROJECT: 1.03	DESIGNER: Rotzoll
---------------	-------------------

TITLE	ROM Sense Amplifier
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NAME:	103reva/romsns	REV:	--	SIZE:	A
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DATE: Oct 7 18:12:58 1993

7.05AA	7.05AB
7.05BA	7.05BB
7.05CA	7.05CB

7.0501AB

7.0501AA

EX 11.0501

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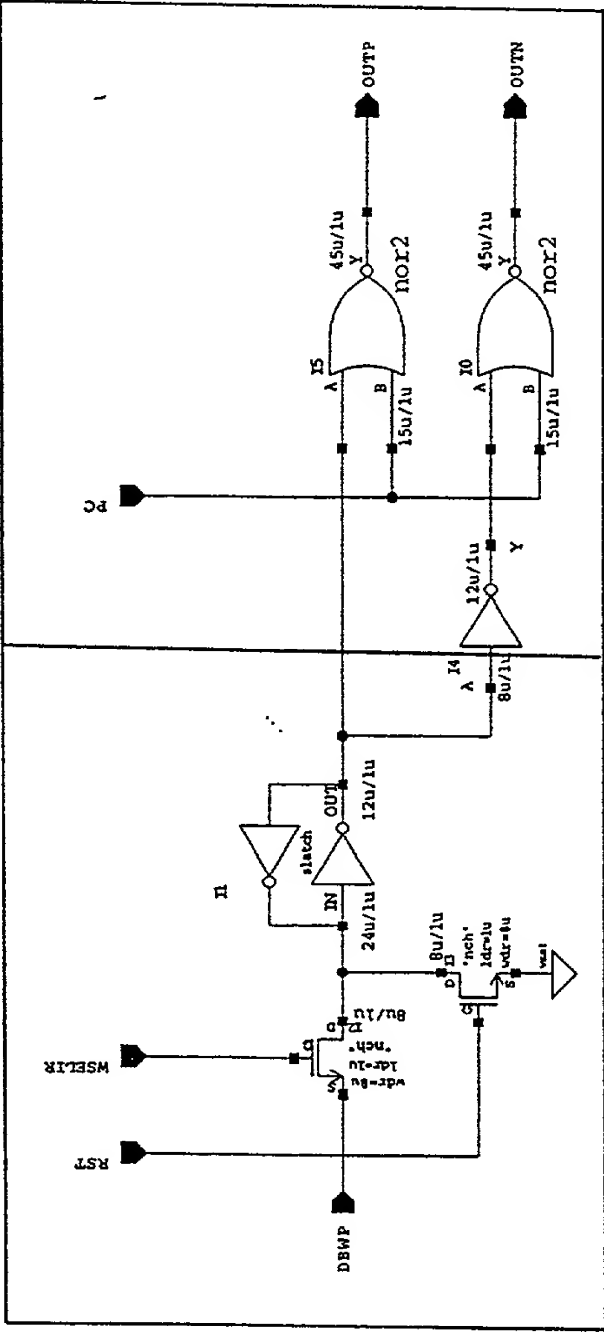


FIG. 7.0501

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Instruction Register Cell			
NAME: 103reva/insrcel		REV: -	SIZE: A
DATE: Oct 5 20:12:49 1993		SHEET: 1	

7.06AA	7.06AB	7.06AC	7.06AD	7.06AE	7.06AF	7.06AG	7.06AH	7.06AI	7.06AJ	7.06AK	7.06AL	7.06AM	7.06AN
	7.06BB	7.06BC	7.06BD	7.06BE	7.06BF	7.06BG	7.06BH	7.06BI	7.06BJ	7.06BK	7.06BL	7.06BM	7.06BN
7.06CA	7.06CB	7.06CC	7.06CD	7.06CE	7.06CF	7.06CG	7.06CH	7.06CI	7.06CJ	7.06CK	7.06CL	7.06CM	7.06CN

IL 11 037 11.0016

Illegible text at the bottom of the page.

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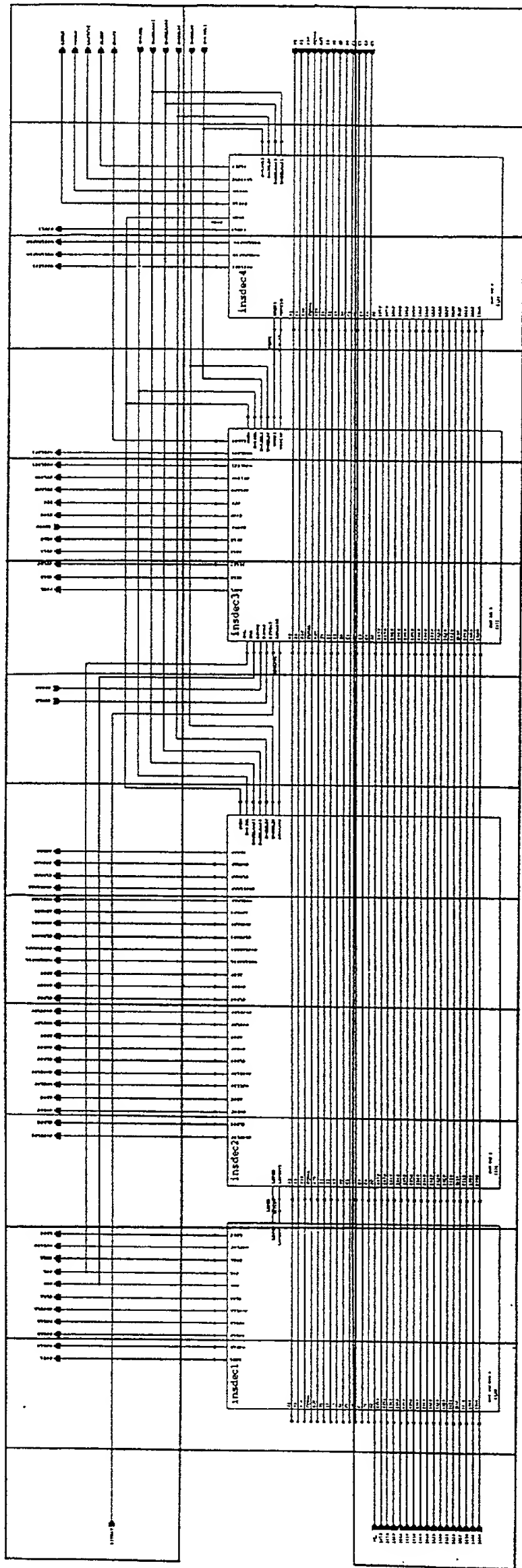


Fig. 7.06

7.0601AA	7.0601AB	7.0601AC	7.0601AD	7.0601AE	7.0601AF	7.0601AG	7.0601AH	7.0601AI
7.0601BA	7.0601BB	7.0601BC	7.0601BD	7.0601BE	7.0601BF	7.0601BG	7.0601BH	7.0601BI
7.0601CA	7.0601CB	7.0601CC	7.0601CD	7.0601CE	7.0601CF	7.0601CG	7.0601CH	7.0601CI
7.0601DA	7.0601DB	7.0601DC	7.0601DD	7.0601DE	7.0601DF	7.0601DG	7.0601DH	7.0601DI
7.0601EA	7.0601EB	7.0601EC	7.0601ED	7.0601EE	7.0601EF	7.0601EG	7.0601EH	7.0601EI
7.0601FA	7.0601FB	7.0601FC	7.0601FD	7.0601FE	7.0601FF	7.0601FG	7.0601FH	7.0601FI
7.0601GA	7.0601GB	7.0601GC	7.0601GD	7.0601GE	7.0601GF	7.0601GG	7.0601GH	7.0601GI
7.0601HA	7.0601HB	7.0601HC	7.0601HD	7.0601HE	7.0601HF	7.0601HG	7.0601HH	7.0601HI

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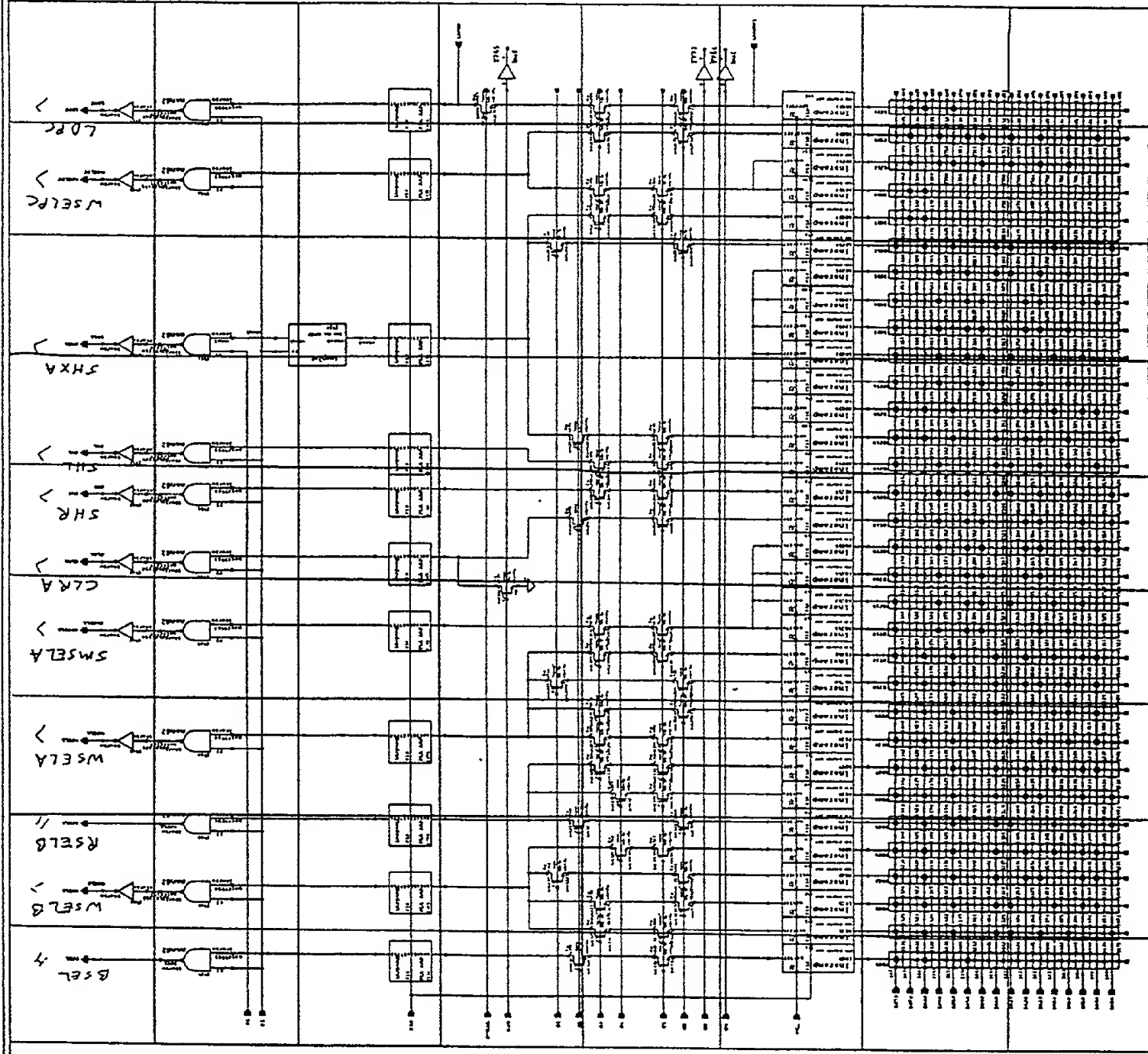
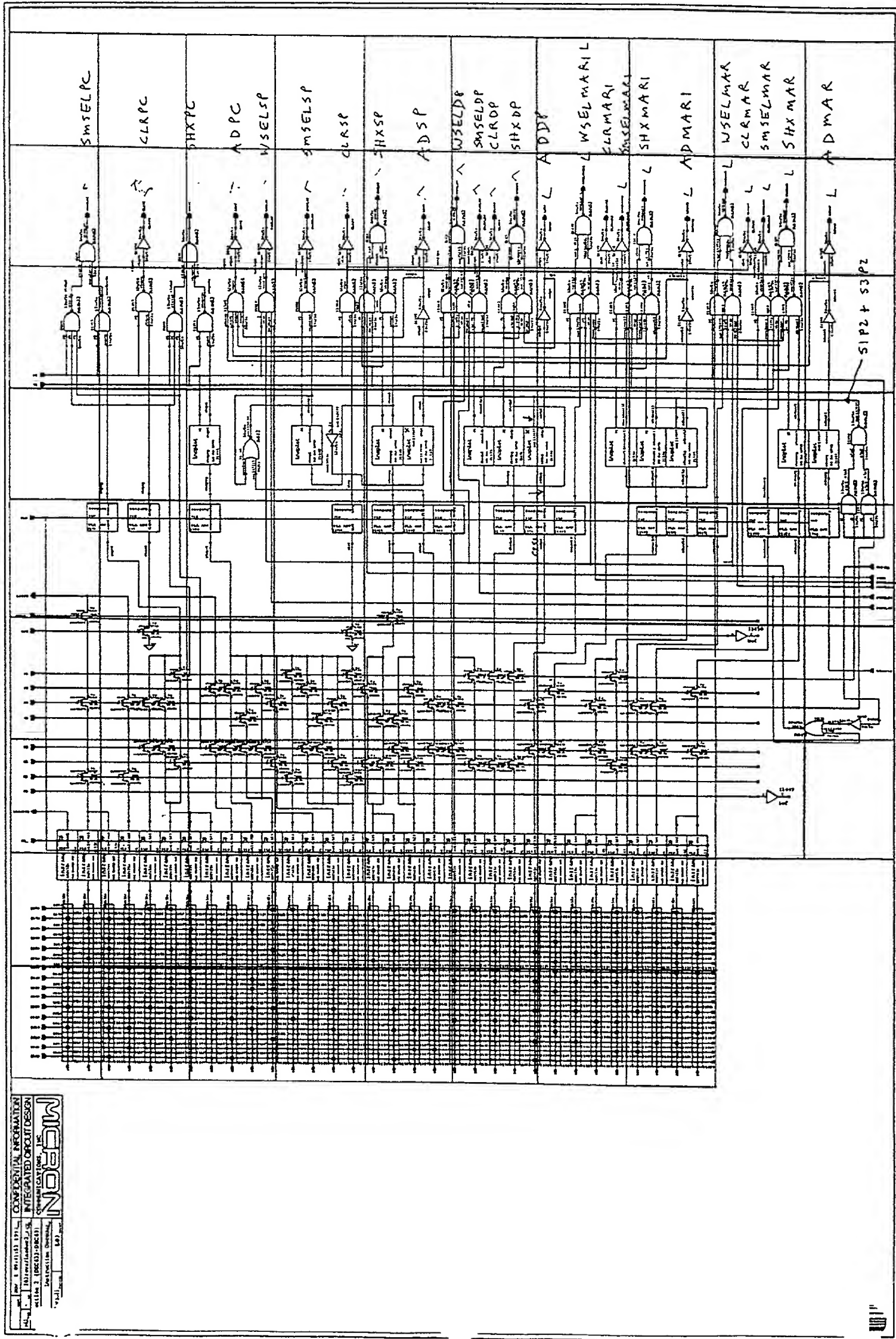


FIG. 7.0601

7.0602AA	7.0602AB	7.0602AC	7.0602AD	7.0602AE	7.0602AF	7.0602AG	7.0602AH
7.0602BA	7.0602BB	7.0602BC	7.0602BD	7.0602BE	7.0602BF	7.0602BG	7.0602BH
7.0602CA	7.0602CB	7.0602CC	7.0602CD	7.0602CE	7.0602CF	7.0602CG	7.0602CH
7.0602DA	7.0602DB	7.0602DC	7.0602DD	7.0602DE	7.0602DF	7.0602DG	7.0602DH
7.0602EA	7.0602EB	7.0602EC	7.0602ED	7.0602EE	7.0602EF	7.0602EG	7.0602EH
7.0602FA	7.0602FB	7.0602FC	7.0602FD	7.0602FE	7.0602FF	7.0602FG	7.0602FH
7.0602GA	7.0602GB	7.0602GC	7.0602GD	7.0602GE	7.0602GF	7.0602GG	7.0602GH
7.0602HA	7.0602HB	7.0602HC	7.0602HD	7.0602HE	7.0602HF	7.0602HG	7.0602HH
		7.0602IC	7.0602ID	7.0602IE	7.0602IF	7.0602IG	7.0602IH
		7.0602JC	7.0602JD	7.0602JE	7.0602JF	7.0602JG	7.0602JH

II II II 7.0602

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 one of these is added
 ADSP, ADDP, ADMARI,
 ADMAR

FIG. 7.0602

ЕОСМ. II

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FOR OFFICIAL USE ONLY	

10-10-60

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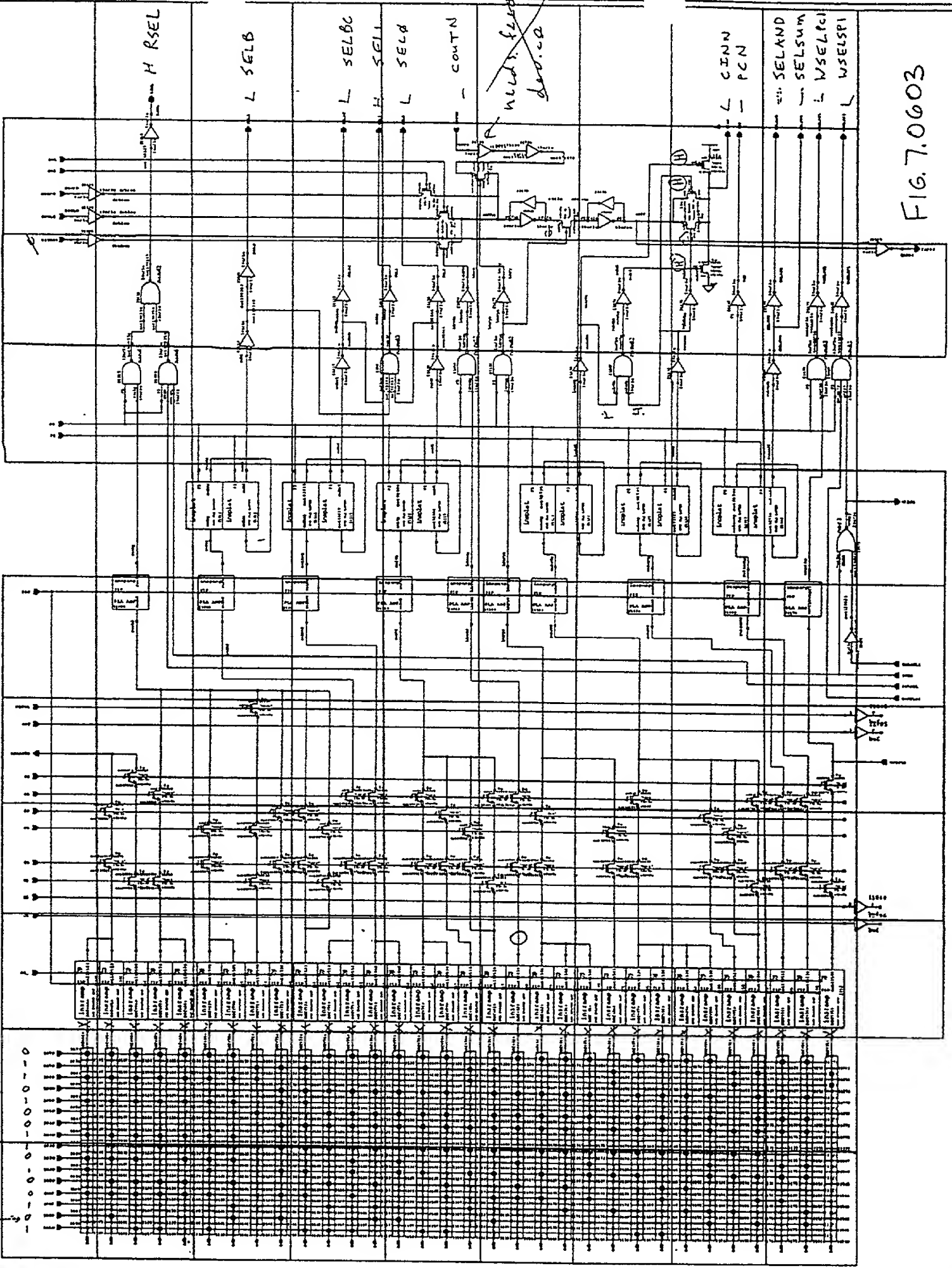


FIG. 7.0603

7.0604AA 7.0604AB 7.0604AC 7.0604AD 7.0604AE 7.0604AF 7.0604AG 7.0604AH 7.0604AI

7.0604AA	7.0604AB	7.0604AC	7.0604AD	7.0604AE	7.0604AF	7.0604AG	7.0604AH	7.0604AI
7.0604BA	7.0604BB	7.0604BC	7.0604BD	7.0604BE	7.0604BF	7.0604BG	7.0604BH	7.0604BI
7.0604CA	7.0604CB	7.0604CC	7.0604CD	7.0604CE	7.0604CF	7.0604CG	7.0604CH	7.0604CI
7.0604DA	7.0604DB	7.0604DC	7.0604DD	7.0604DE	7.0604DF	7.0604DG	7.0604DH	7.0604DI
7.0604EA	7.0604EB	7.0604EC	7.0604ED	7.0604EE	7.0604EF	7.0604EG	7.0604EH	7.0604EI
7.0604FA	7.0604FB	7.0604FC	7.0604FD	7.0604FE	7.0604FF	7.0604FG	7.0604FH	7.0604FI
7.0604GA	7.0604GB	7.0604GC	7.0604GD	7.0604GE	7.0604GF	7.0604GG	7.0604GH	7.0604GI
7.0604HA	7.0604HB	7.0604HC	7.0604HD	7.0604HE	7.0604HF	7.0604HG		
7.0604IA	7.0604IB	7.0604IC	7.0604ID	7.0604IE	7.0604IF	7.0604IG		
7.0604JA	7.0604JB	7.0604JC	7.0604JD	7.0604JE	7.0604JF	7.0604JG	7.0604JH	7.0604JI

7.0604AA 7.0604AB 7.0604AC 7.0604AD 7.0604AE 7.0604AF 7.0604AG 7.0604AH 7.0604AI

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DATE 08-01-2001 BY 60322 UCBAW/BJS

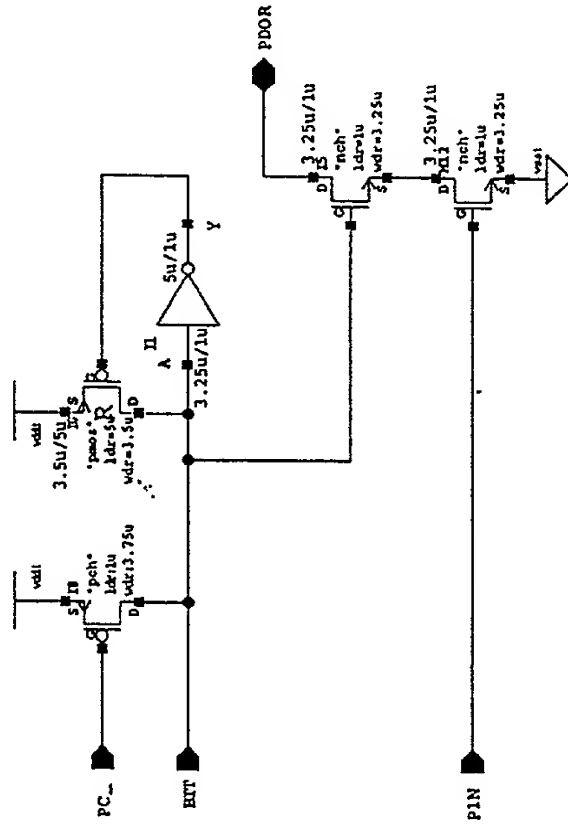


FIG. 7.060401

MICRON COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Instruction Decoder ROM Amp			
NAME:	103reva/insramp	REV: -	SIZE: A
DATE:	Oct 6 12:20:55 1993	SHEET:	

7.07AA	7.07AB
7.07BA	7.07BB

II II III III

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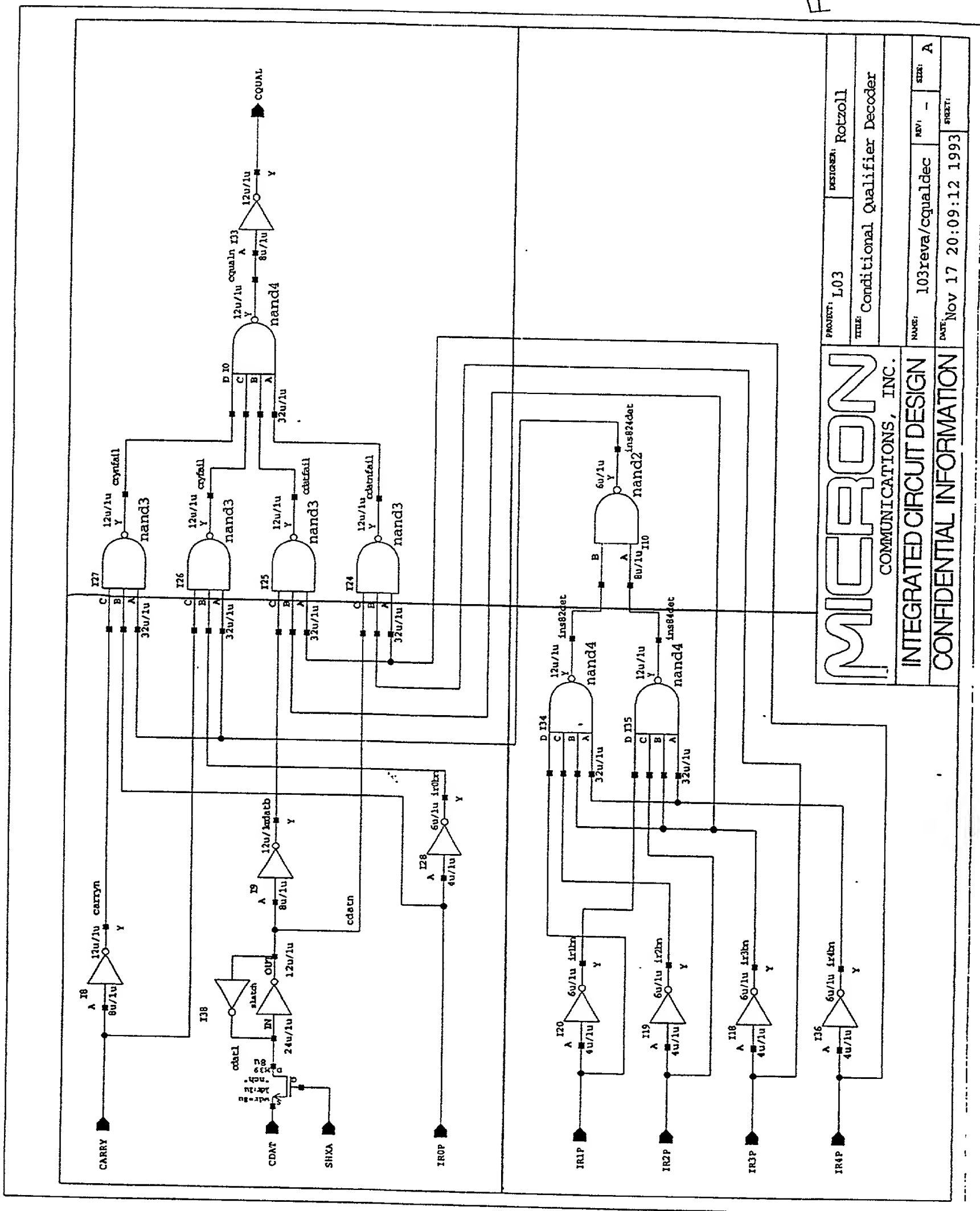


Fig. 7.07

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: Conditional Qualifier Decoder	
NAME: 103reva/cqualdec	REV: -
DATE: Nov 17 20:09:12 1993	SIZE: A
SHEET: 1	

7.08AA

7.08BA

7.08CA

7.08BB

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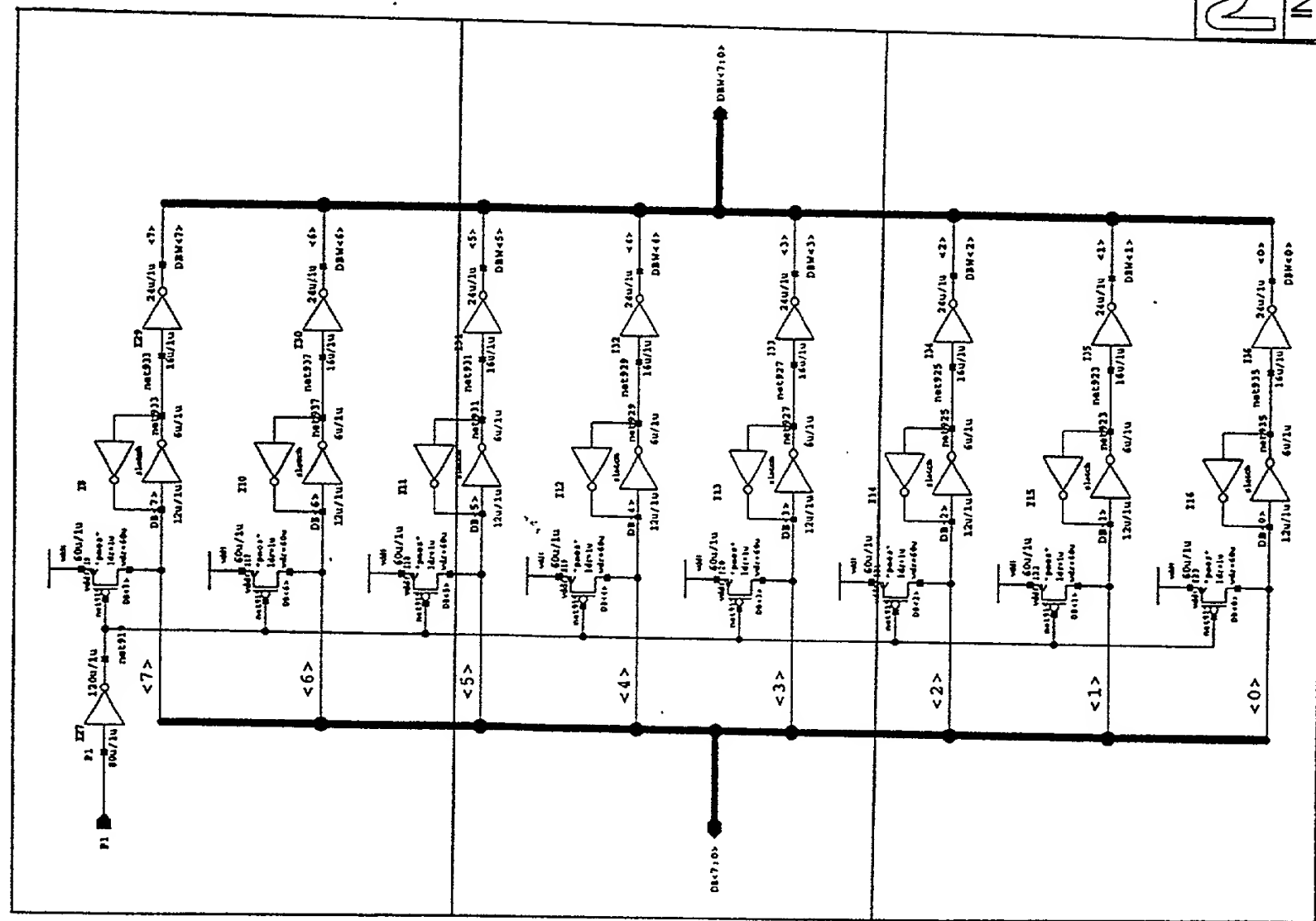


FIG. 7.08

MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		FILE: Databus Latch/Precharge	
INTEGRATED CIRCUIT DESIGN		DATE: 103revs/dblatch	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 14:51:49 1993	BY: ml

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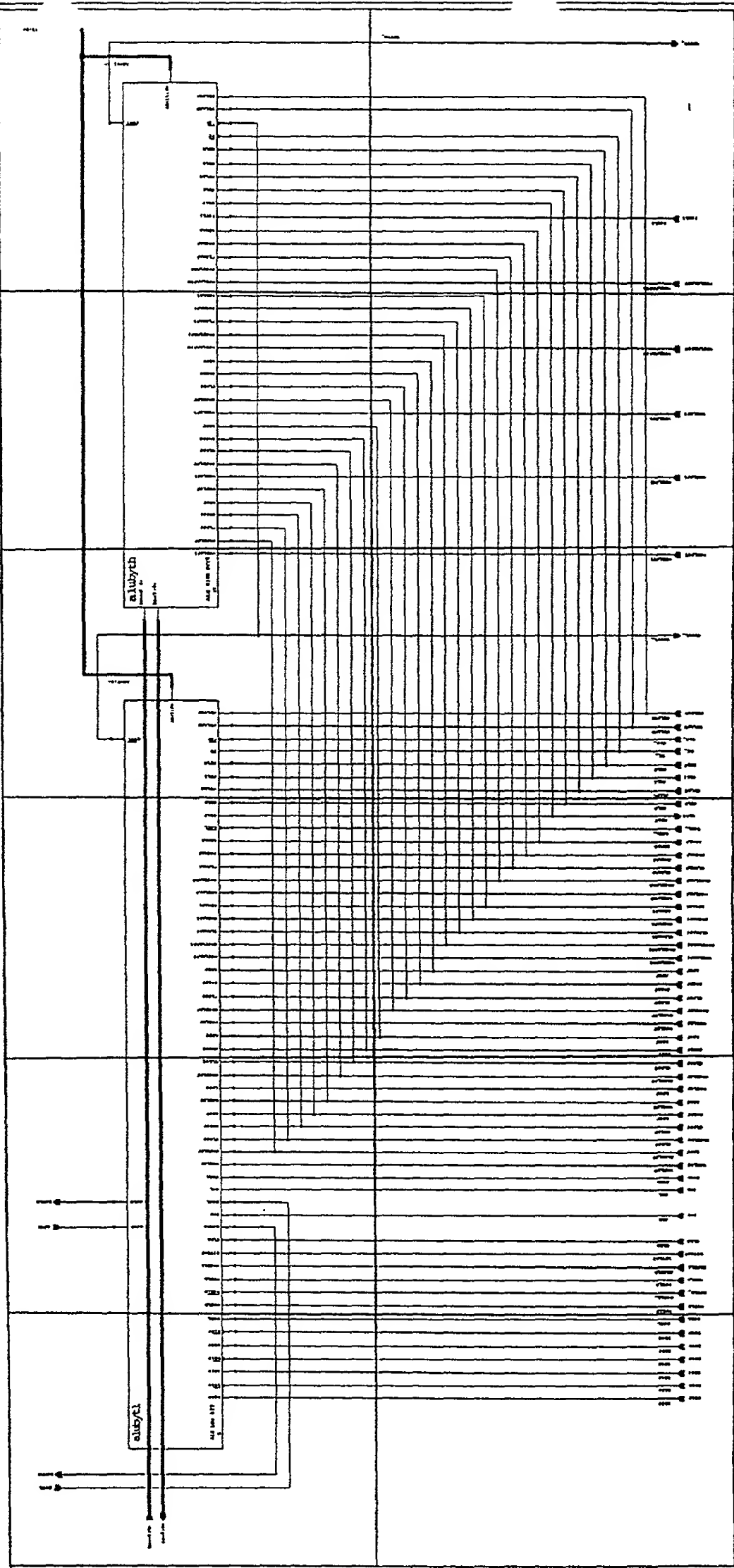
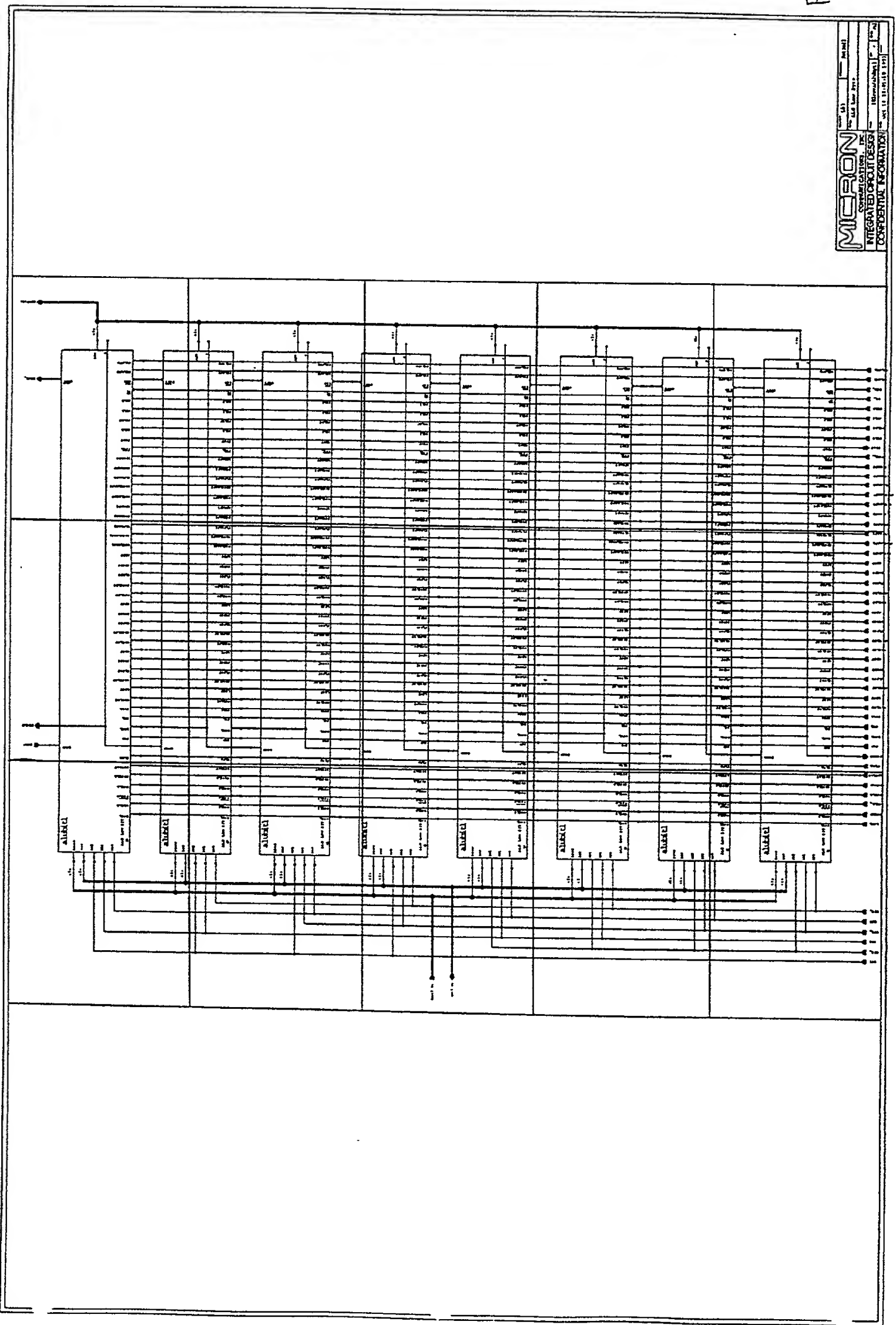


Fig. 7.09

7.0901AA	7.0901AB	7.0901AC	7.0901AD	7.0901AE
7.0901BA	7.0901BB	7.0901BC	7.0901BD	7.0901BE
7.0901CA	7.0901CB	7.0901CC	7.0901CD	7.0901CE

FIG. 7.0901



MICRON
TECHNOLOGY
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

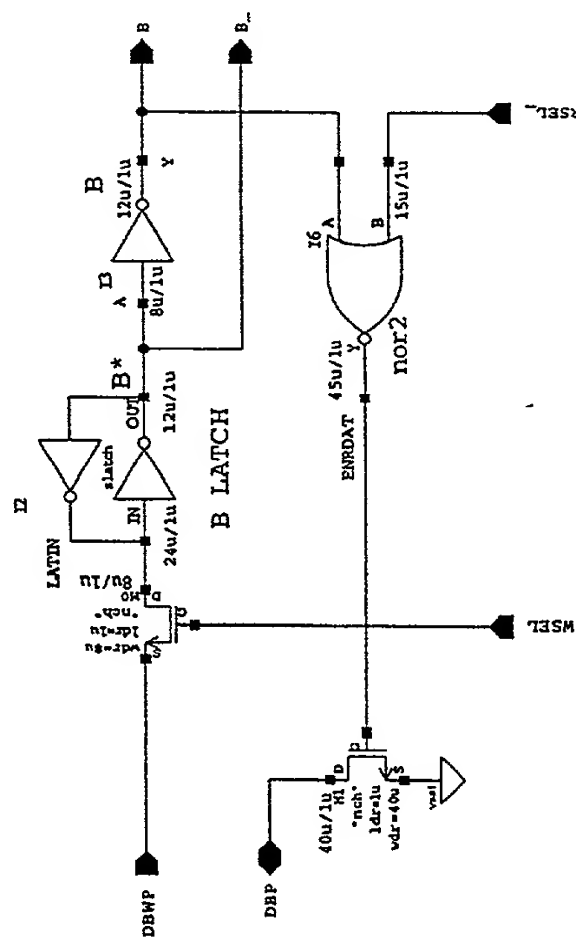
Doc. No.	7.0901
Rev.	1.0
Date	10/10/90
Author	...
Checker	...
Appr.	...

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DATE 10/10/90 BY 1045/...

Station	Time	Lat	Long	Alt	Temp	Hum	Wind	Dir	Pres	Cloud	Vis	Remarks
100000	0000	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0100	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0200	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0300	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0400	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0500	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0600	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0700	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0800	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	0900	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1000	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1100	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1200	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1300	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1400	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1500	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1600	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1700	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1800	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	1900	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	2000	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	2100	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	2200	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	2300	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000
100000	2400	12 22 22	74 12 22	1000	10.0	100	10	10	1000	100	10	1000

[illegible]

FIG. 7.09010102



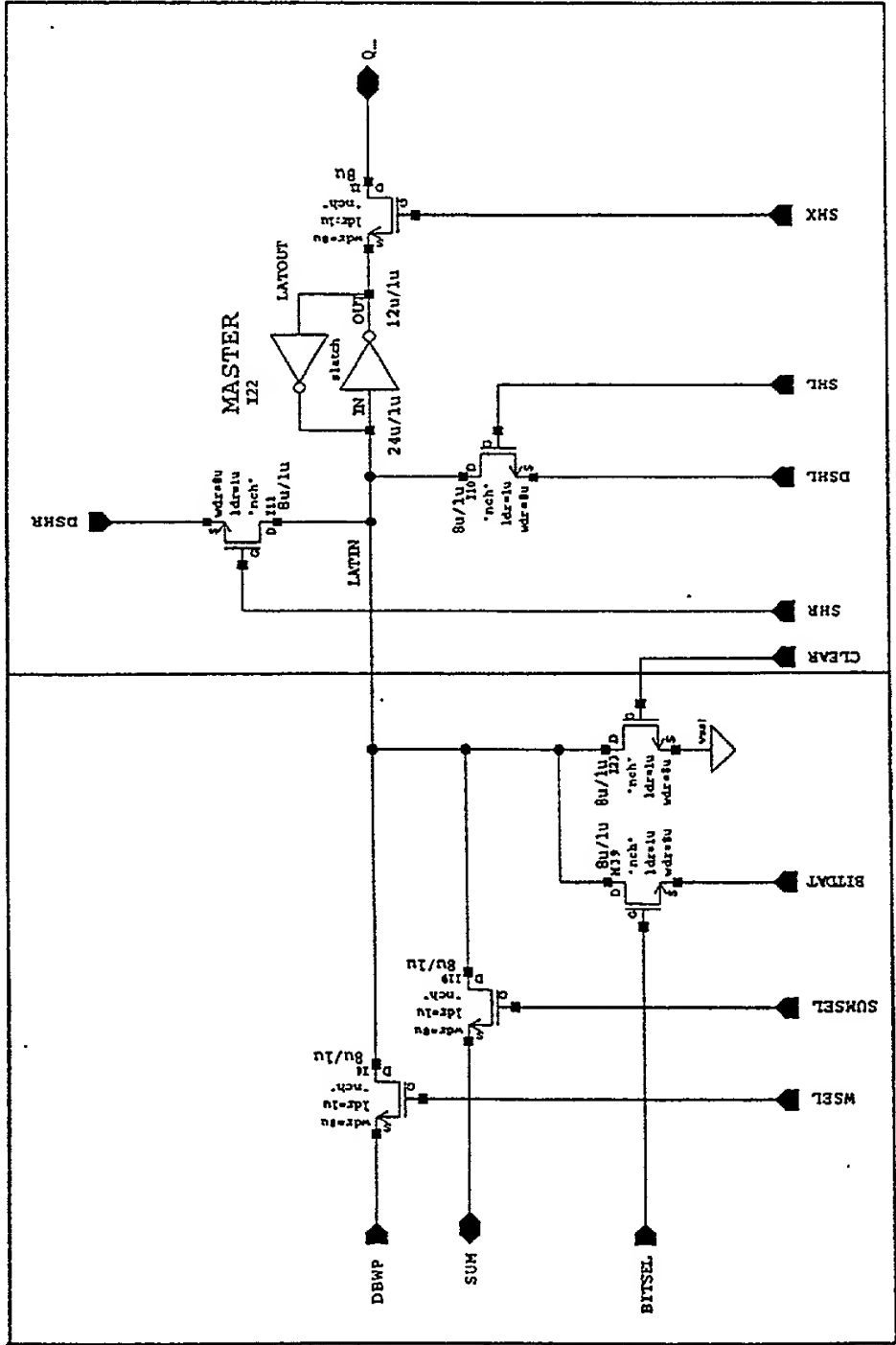
MICRON			
COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: ALU B Register Cell			
NAME: 103reva/alubcell		REV: -	SIZE: A
DATE: Oct 1 15:32:35 1993		SHEET: 1	

7.09010103AB

7.09010103AA

7.09010103

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MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ALU A Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/aluacell	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 1 15:41:37 1993	SHEET: A

FIG. 7.0901010103

7.09010104AB

7.09010104AA

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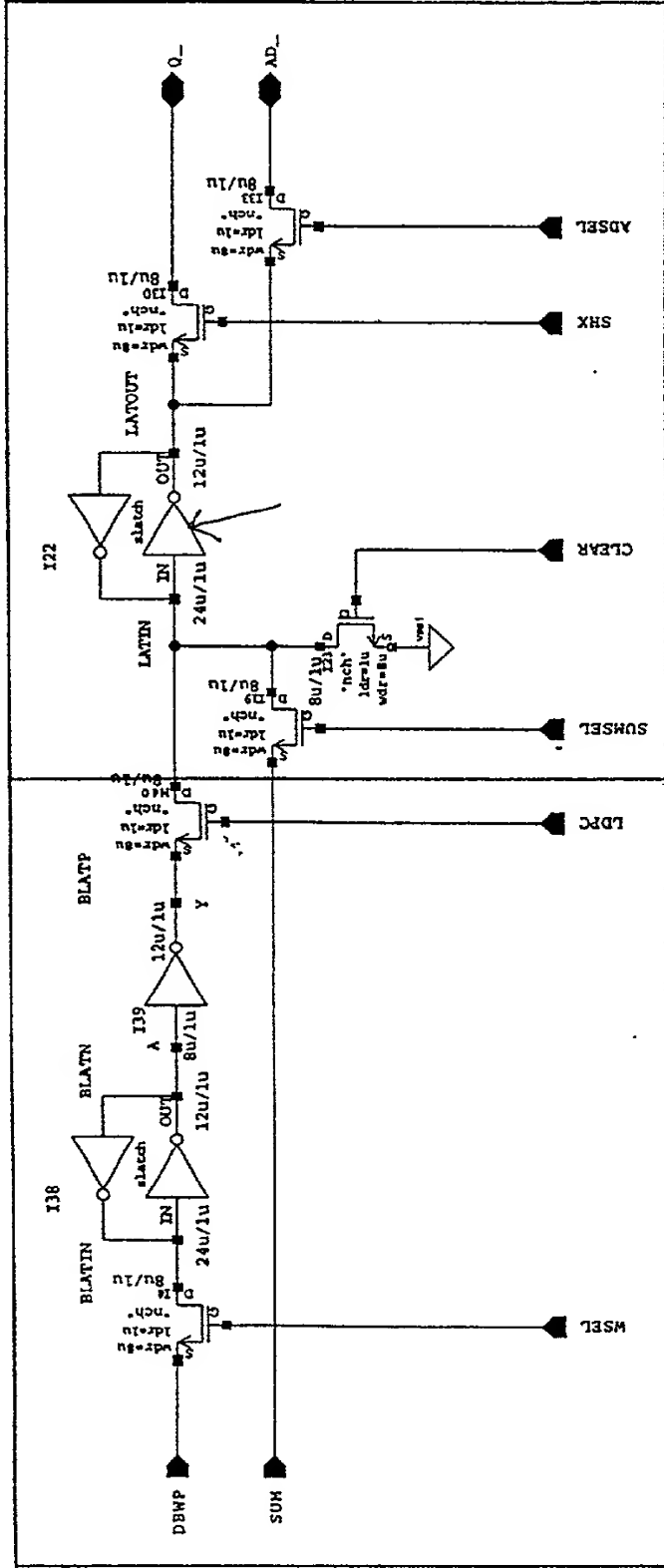
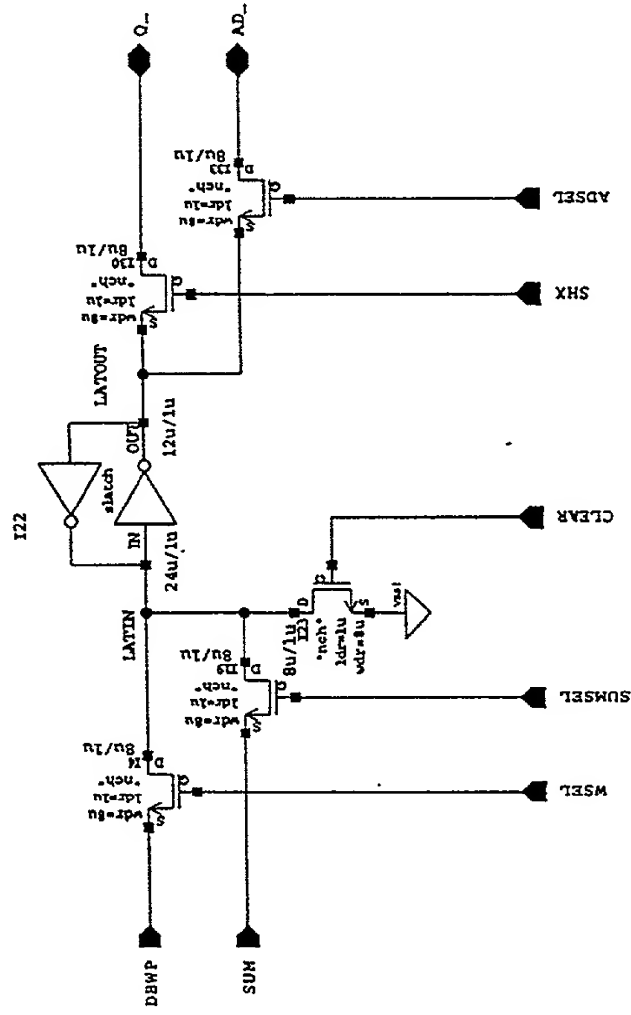


Fig. 7.09010104

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: ALU Register Cell			
NAME: 103reva/alupc		REV: -	SIZE: A
DATE: Oct 1 15:45:48 1993		SHEET: 1	

4000 2000 4000 6000 8000 10000 12000 14000 16000 18000 20000 22000 24000 26000 28000 30000 32000 34000 36000 38000 40000 42000 44000 46000 48000 50000 52000 54000 56000 58000 60000 62000 64000 66000 68000 70000 72000 74000 76000 78000 80000 82000 84000 86000 88000 90000 92000 94000 96000 98000 100000



MICRON				PROJECT: L03		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.				TITLE: ALU Register Cell			
INTEGRATED CIRCUIT DESIGN				NAME: 103reva/alurcell	REV: -	SIZE: A	
CONFIDENTIAL INFORMATION				DATE: Oct 1 15:51:03 1993		SHEET: 1	

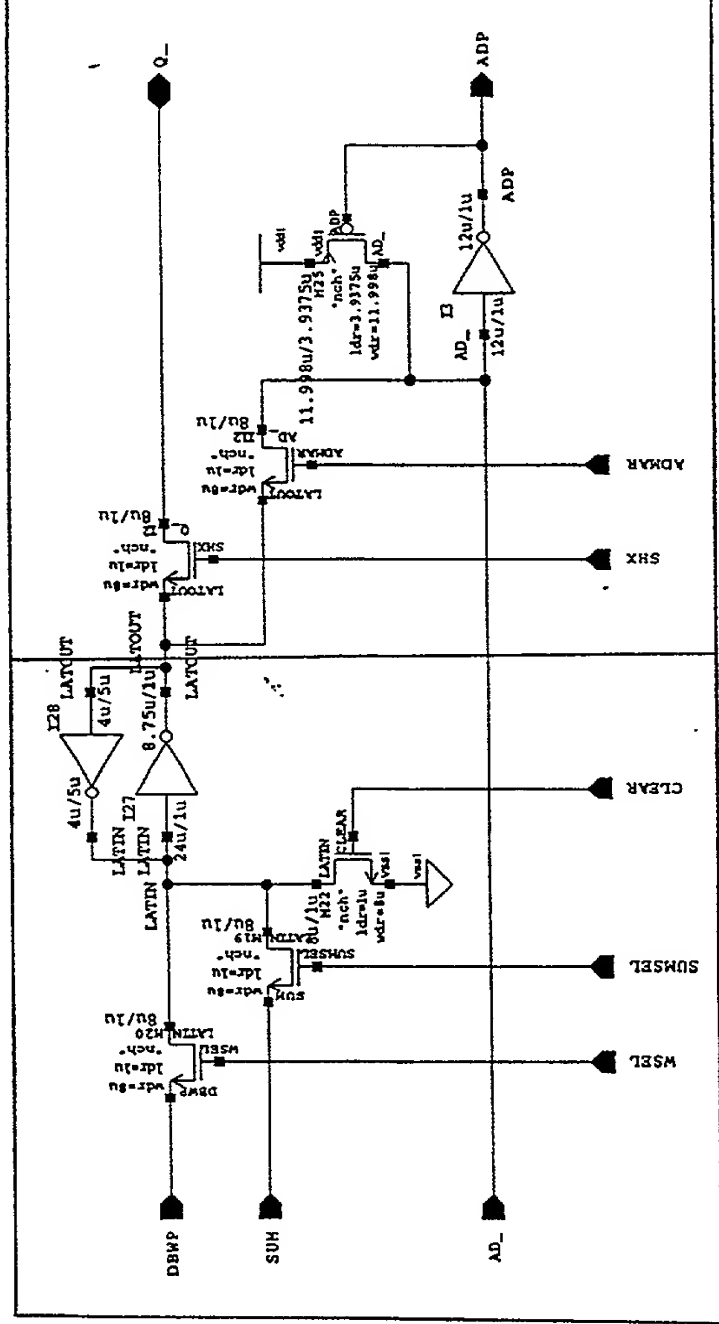
Fig. 7.09010105

7.09010106AB

7.09010106AA

ILX 09010106

FIG. 7.09010106



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: ALU Memory Address Register	
NAME: 103reva/alumar	REV: B8
DATE: Jan 4 10:27:28 1996	SHEET: A

B8: added pch feedback device

FIG. 7.09010106

;



Fig. 7.09010107

7.09010108AA	7.09010108AB	7.09010108AC
7.09010108BA	7.09010108BB	7.09010108BC

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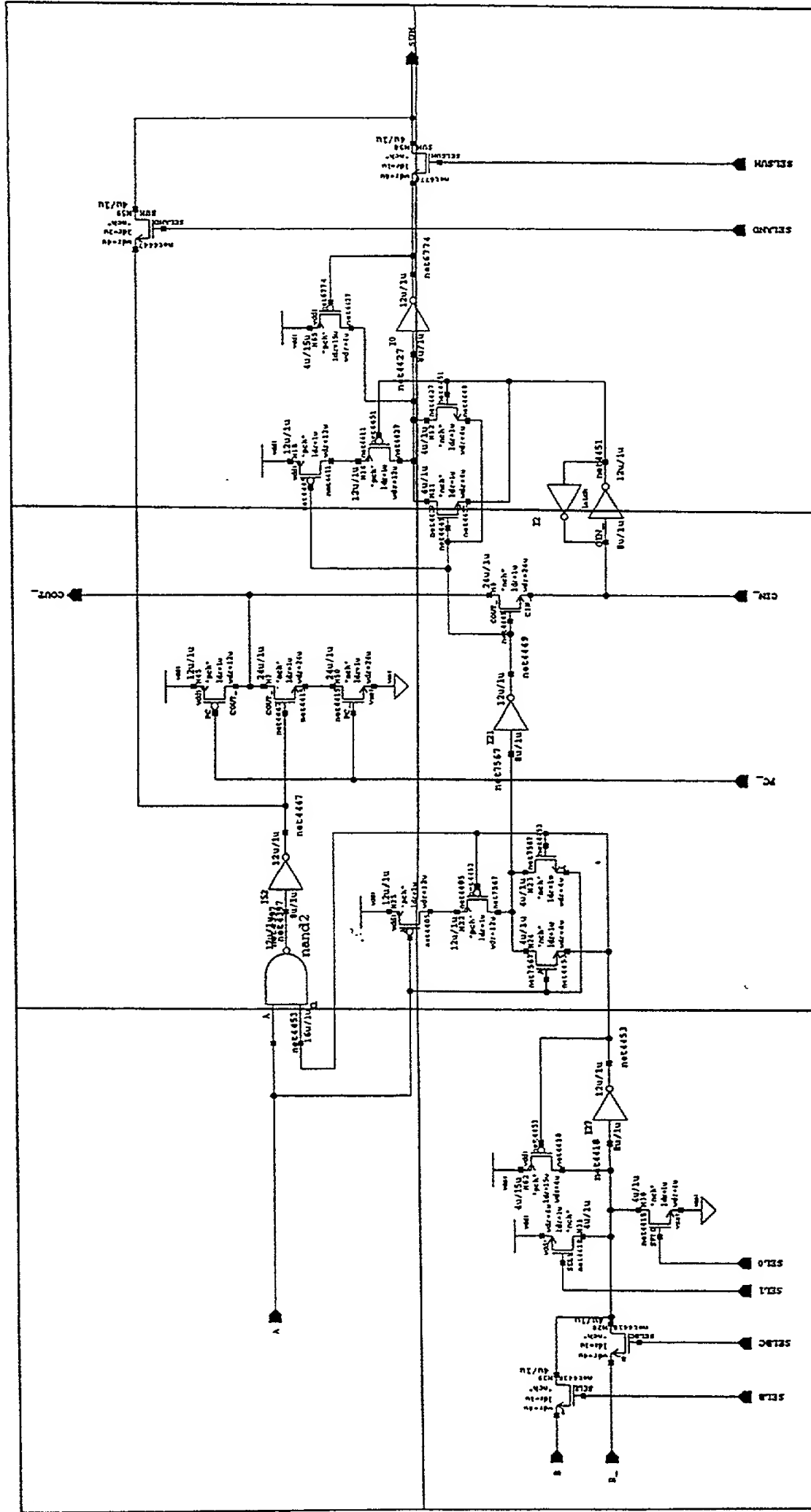
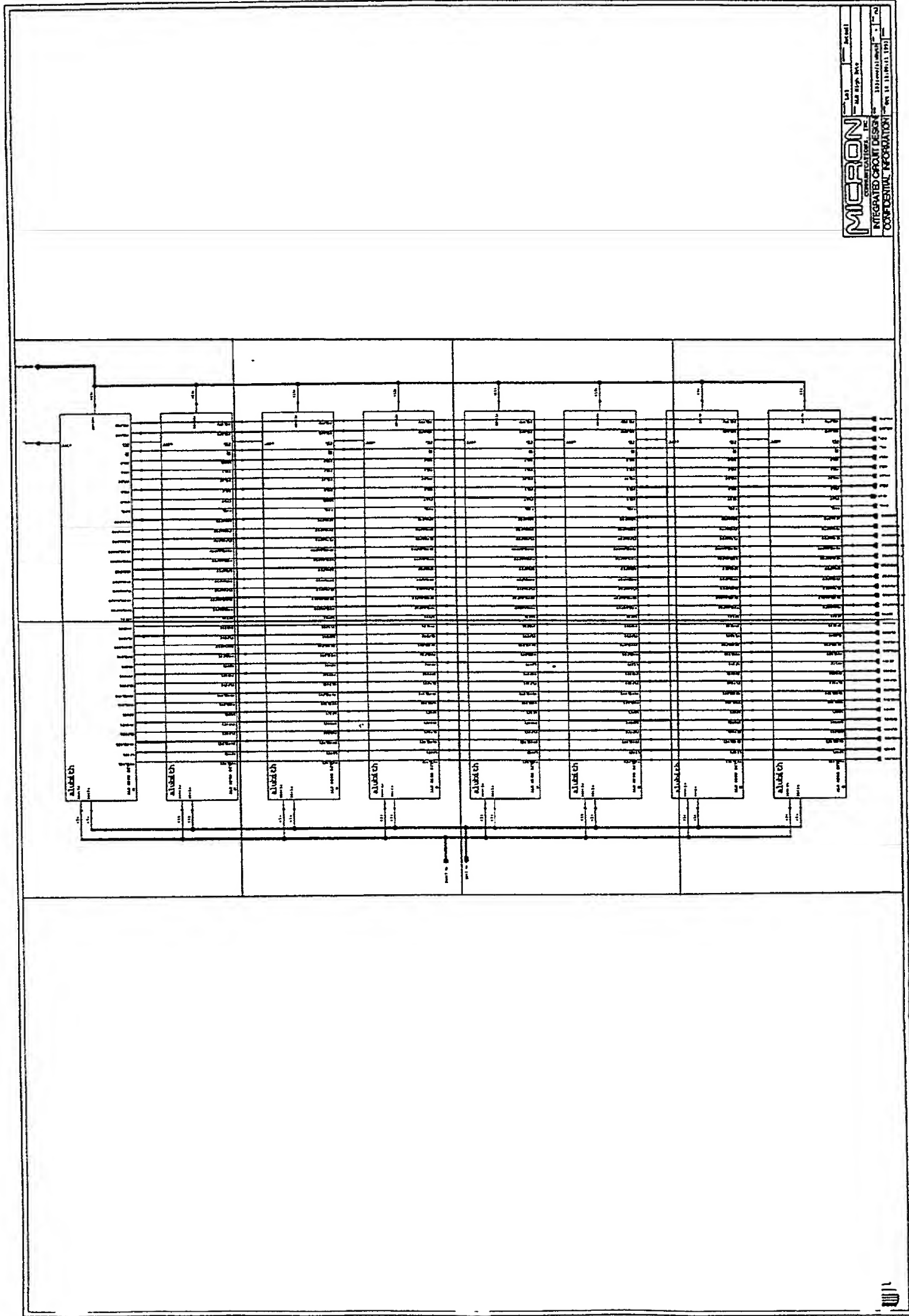


Fig. 7.09010108
 BS: move feedback device from I21 to I27

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ALU Adder	
INTEGRATED CIRCUIT DESIGN		DATE: 103revs/aluadd	REV: B5
CONFIDENTIAL INFORMATION		DATE: Sep 16 15:48:21 1995	FILE: ml

7.0902AA	7.0902AB	7.0902AC	7.0902AD
7.0902BA	7.0902BB	7.0902BC	7.0902BD

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Rev. 10/10/11 (12)

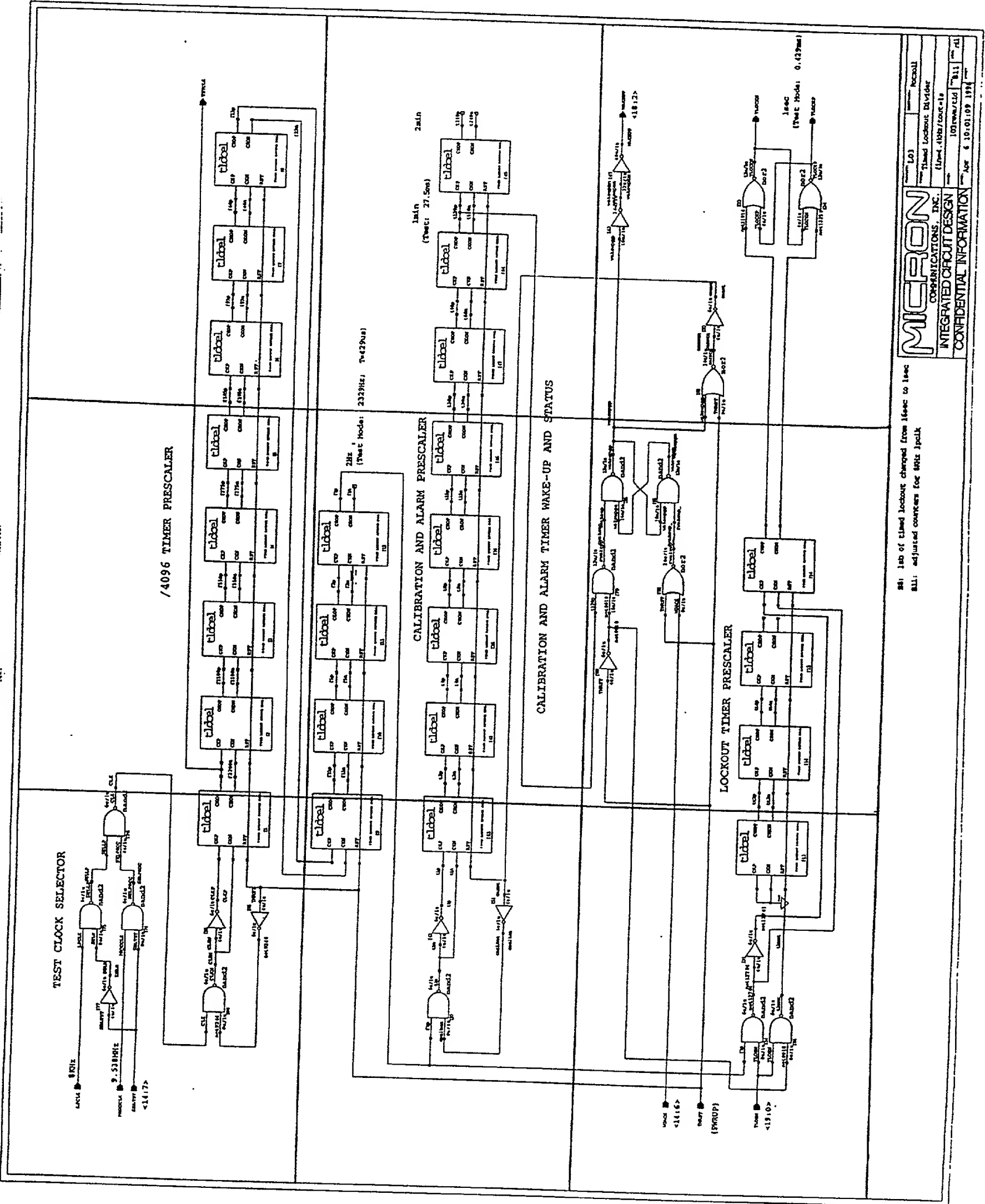
FIG. 7.0902

7.090201AA	7.090201AB	7.090201AC
------------	------------	------------

ILX 07 7.090201AA

7.10AA	7.10AB	7.10AC
7.10BA	7.10BB	7.10BC
7.10CA	7.10CB	7.10CC

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84: 1st of timed lockout changed from 16sec to 1sec
 85: adjusted counters for 4096 prescaler

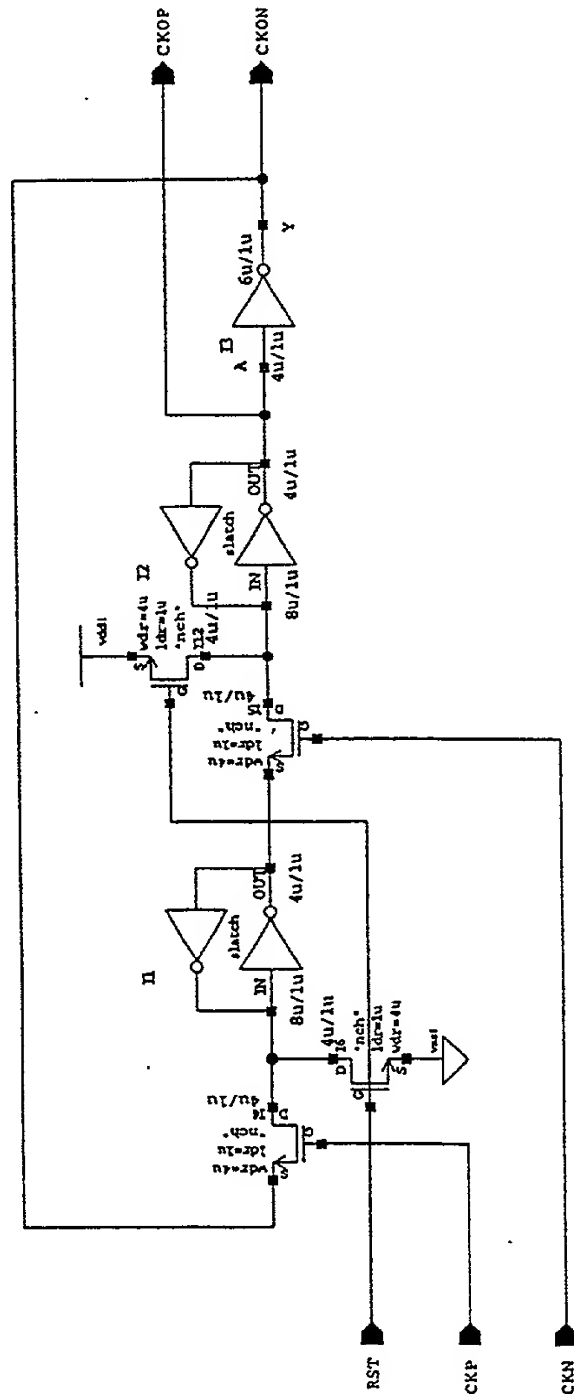
MICRON
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 INTEGRATED CIRCUIT DESIGN
 CONFIDENTIAL INFORMATION

Rev	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0
Date										
By										
Chk										
App										

Apr 6 10:01:09 1984

FIG. 7.10

12/29/92



MICRON				PROJECT: L03		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.				TITLE: Tined Lockout Divider Cell			
INTEGRATED CIRCUIT DESIGN				NAME: 103reva/tlôcel		REV: A	
CONFIDENTIAL INFORMATION				DATE: Sep 22 15:26:56 1994		SHEET: 1	

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Fig. 7.1001

7.11AB

7.11AA

II II II II II

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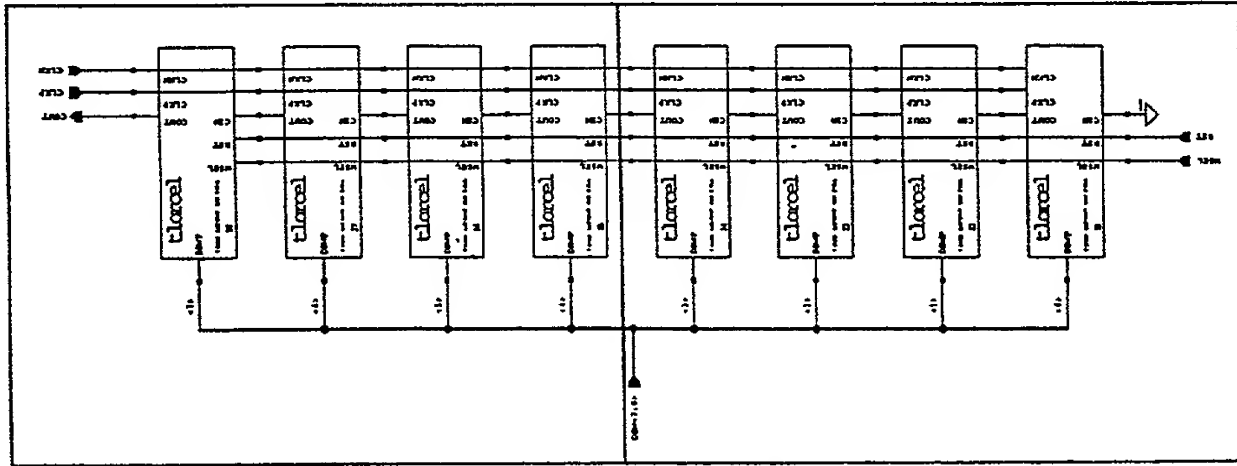


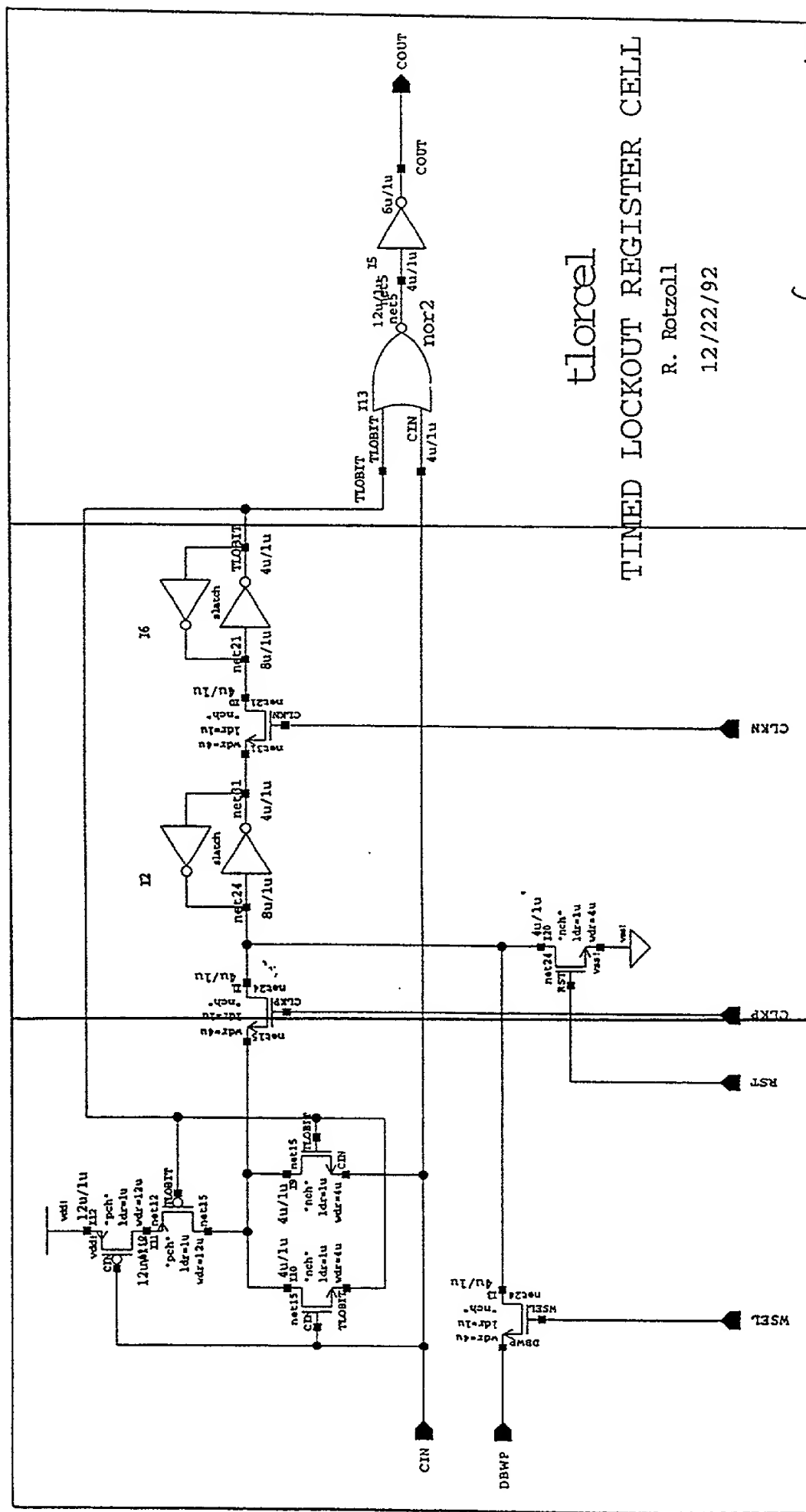
FIG. 7.11

MICRON		1.03	Rev. 1.03
COMMUNICATIONS, INC.		Timed Lockout Register	
INTEGRATED CIRCUIT DESIGN		101rev/1009	Rev. 1.03
CONFIDENTIAL INFORMATION		Oct 1 12:05:17 1991	

7.1101AA	7.1101AB	7.1101AC
----------	----------	----------

II. II. II. II. II. II. II. II.

63



TlOrCel
TIMED LOCKOUT REGISTER CELL

R. Rotzoll

12/22/92

down counter

FIG. 7.1101

FIG. 7.12 is a schematic diagram of a register file structure. The register file consists of eight registers, labeled regcell1 through regcell8. Each register is a 16-bit register with a data input (D) and a data output (Q). The registers are connected to a common data bus (DBW<7:0> and DBW<7:10>). The registers are also connected to a common control bus (RSEL, RST, MSEL, and MSELN). The registers are connected to a common clock signal (BU/BU).

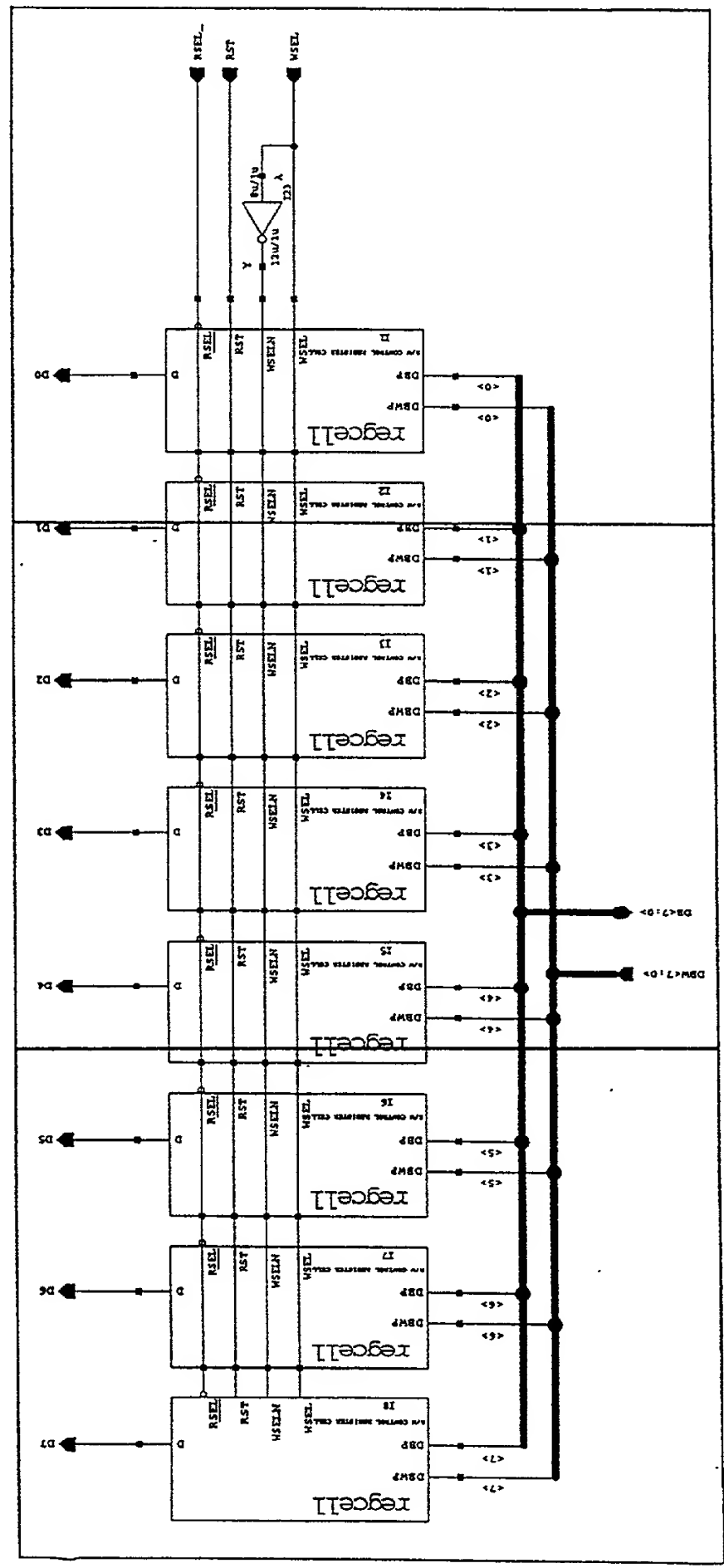
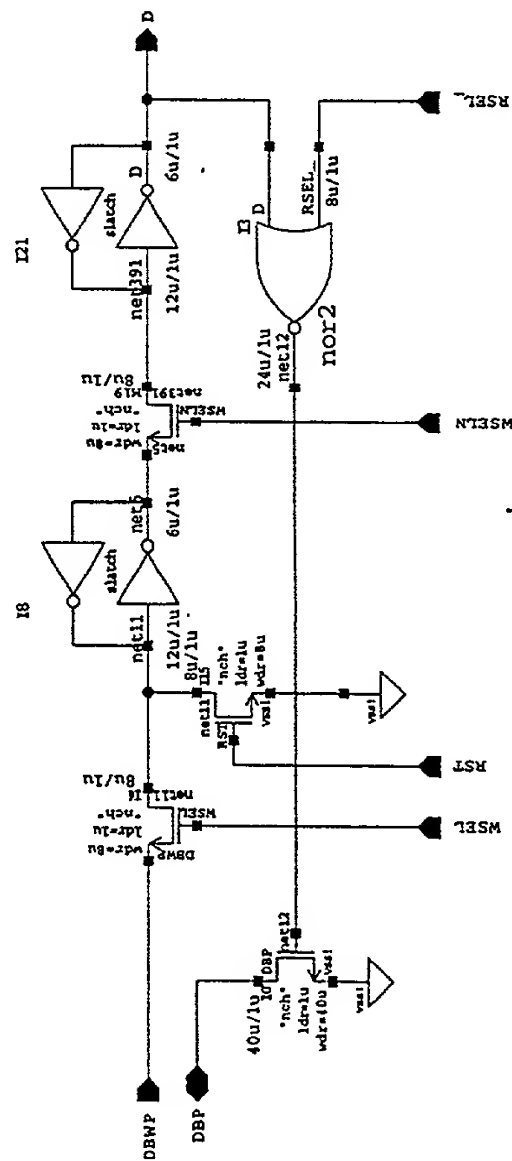


Fig. 7.12

MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: R/W Control Register	
INTEGRATED CIRCUIT DESIGN		DATE: 103rev0/oreg	REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 12 09:44:40 1993	REVISION: ml

Fig. 7. 201



MICRON		PROJECT: L03		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.		TITLE: R/W Control Register Cell			
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/regcell		REV: -	
CONFIDENTIAL INFORMATION		DATE: Nov 12 09:41:36 1993		SHEET: A	

7.13AA

7.13BA

7.13 7.13

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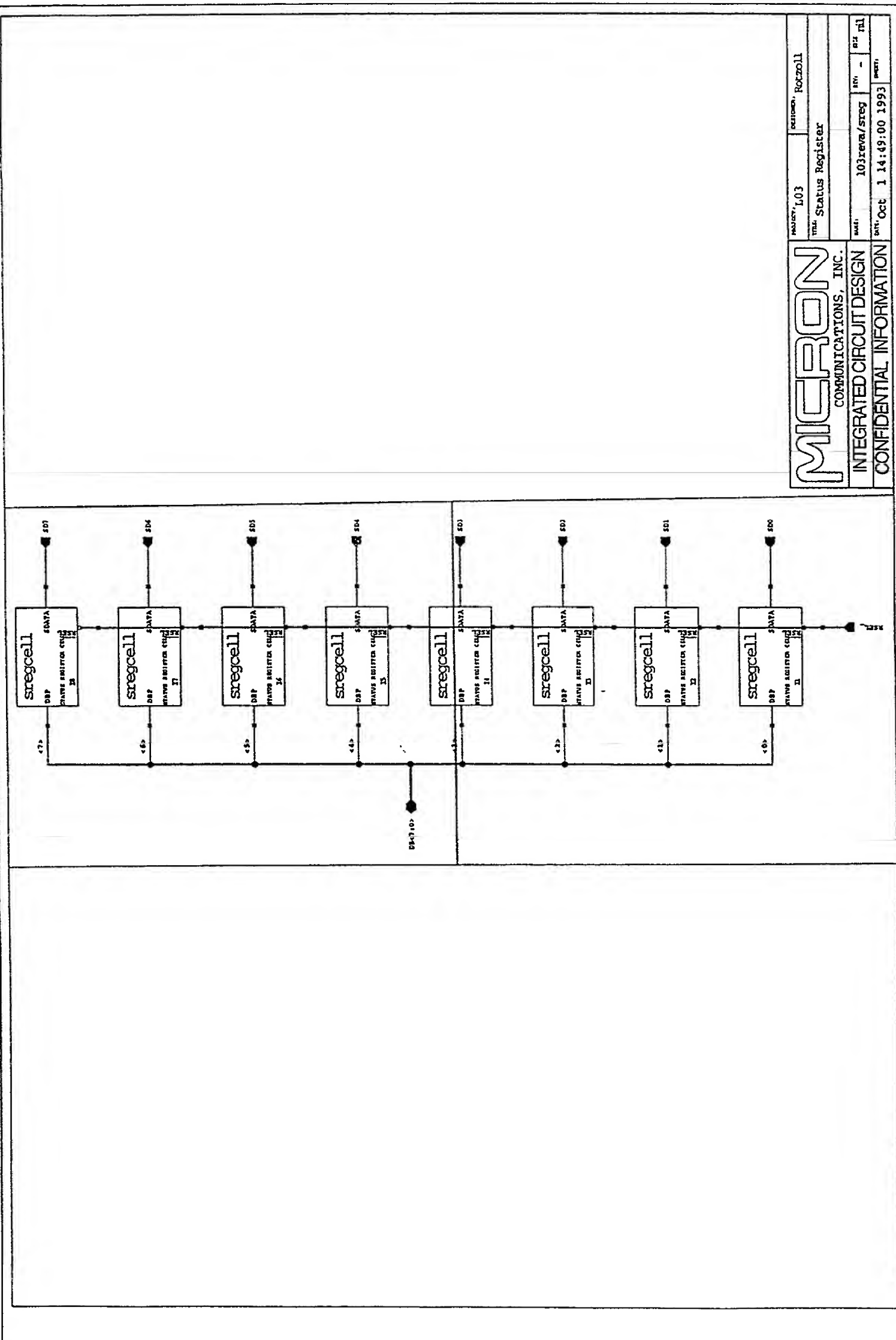
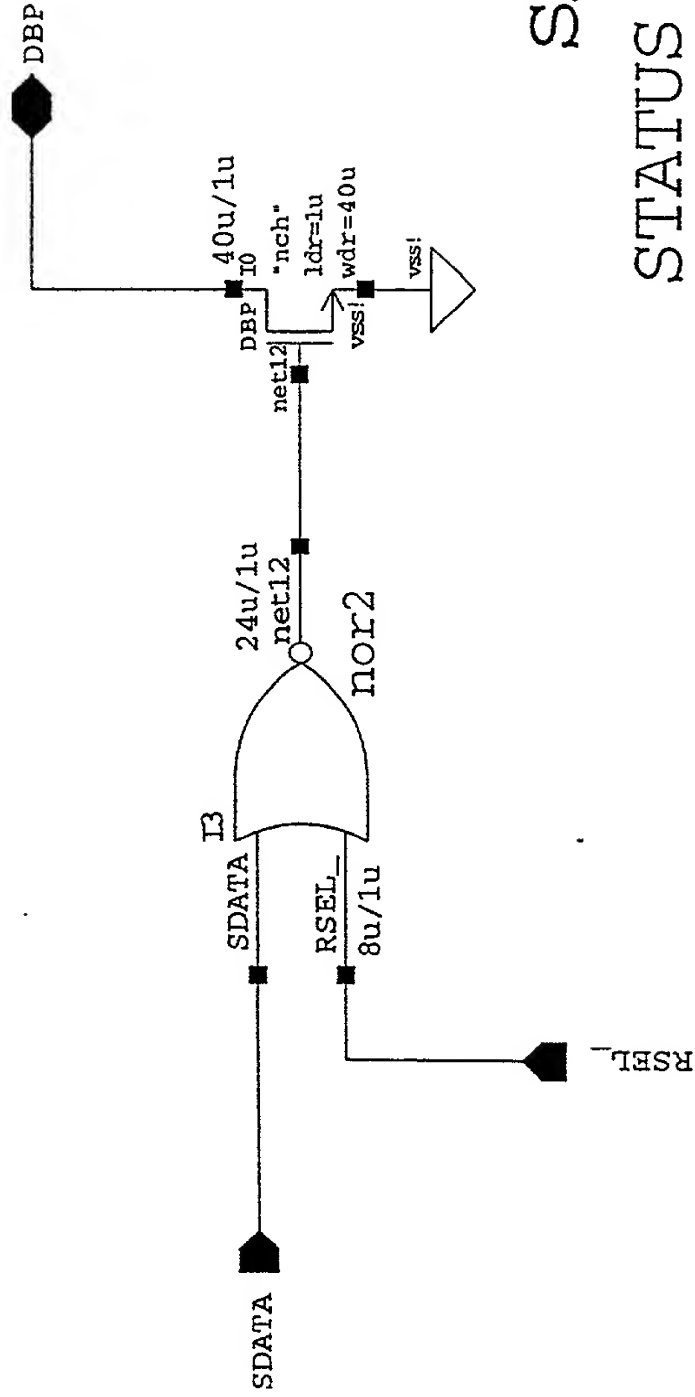


FIG. 7.13

DBP I3 SDATA RSEL_



sregcell

STATUS REGISTER CELL

R. Rotzoll

12/8/92

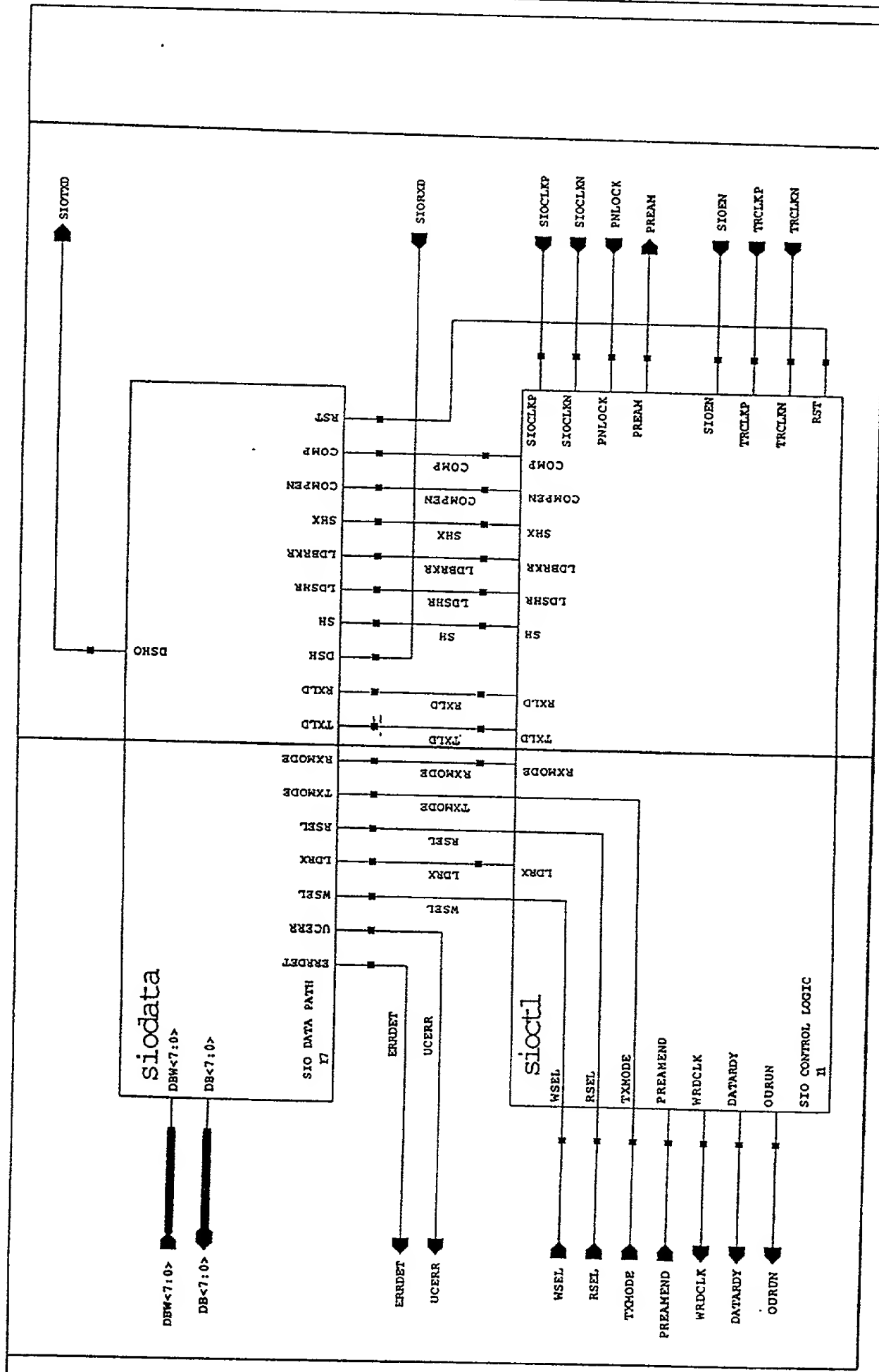
FIG. 7.1301

7.14AB

7.14AA

Exhibit No. 11

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MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Serial I/O	
INTEGRATED CIRCUIT DESIGN		Serial/Block Enc/Dec	
CONFIDENTIAL INFORMATION		NAME: 103reva/sio	REV: B11
		DATE: Apr 4 10:16:14 1996	SIZE: A
		SHEET:	

B8: deleted BRKREN
B11: added non-overlapping clocks

Fig. 7.14

7.1401AA	7.1401AB	7.1401AC	7.1401AD	7.1401AE	7.1401AF
7.1401BA	7.1401BB	7.1401BC	7.1401BD	7.1401BE	7.1401BF
7.1401CA	7.1401CB	7.1401CC	7.1401CD	7.1401CE	7.1401CF
7.1401DA	7.1401DB	7.1401DC	7.1401DD	7.1401DE	7.1401DF
7.1401EA	7.1401EB	7.1401EC	7.1401ED	7.1401EE	7.1401EF
7.1401FA	7.1401FB	7.1401FC	7.1401FD	7.1401FE	7.1401FF
7.1401GA	7.1401GB	7.1401GC	7.1401GD	7.1401GE	7.1401GF

Fig. 7.1401

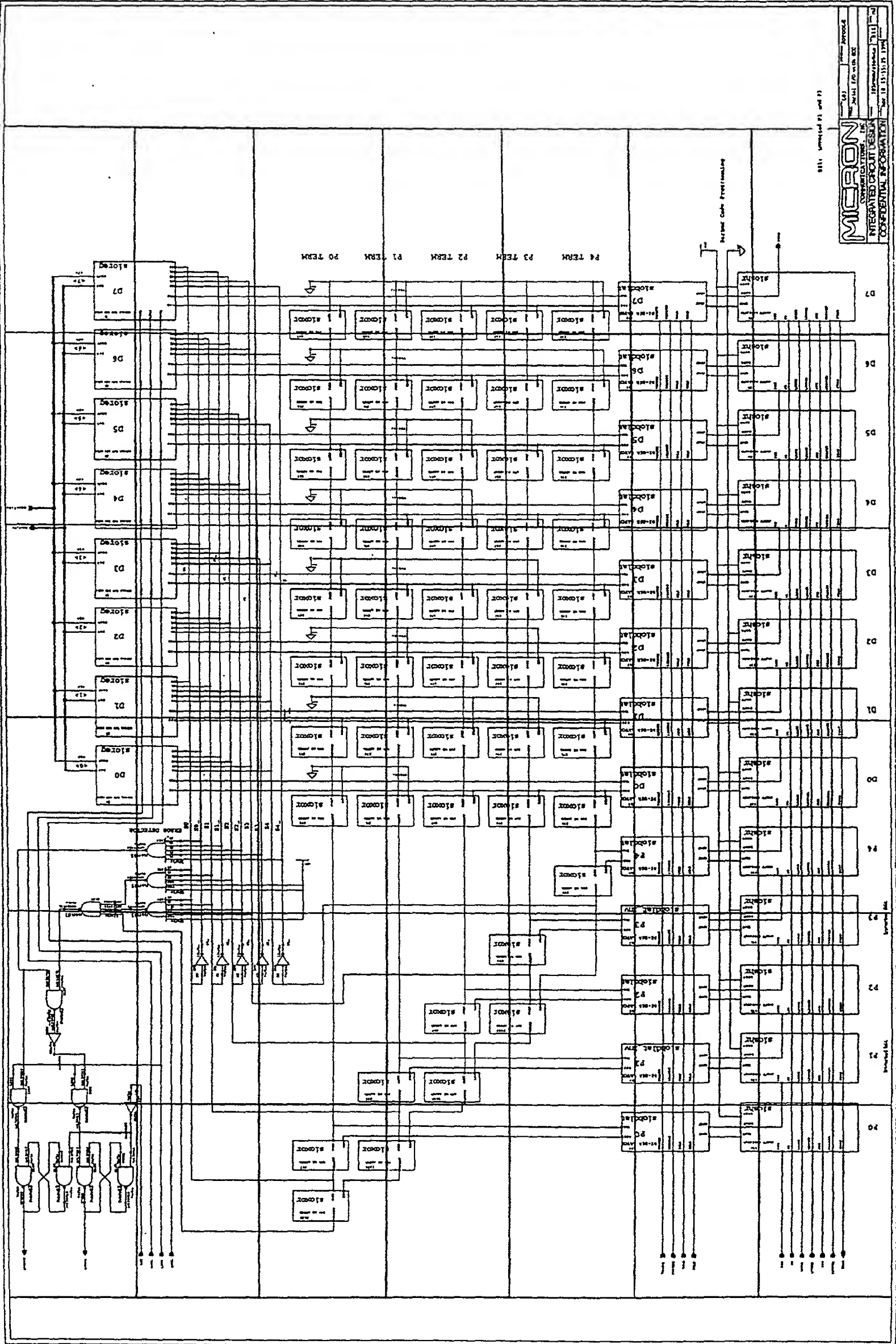
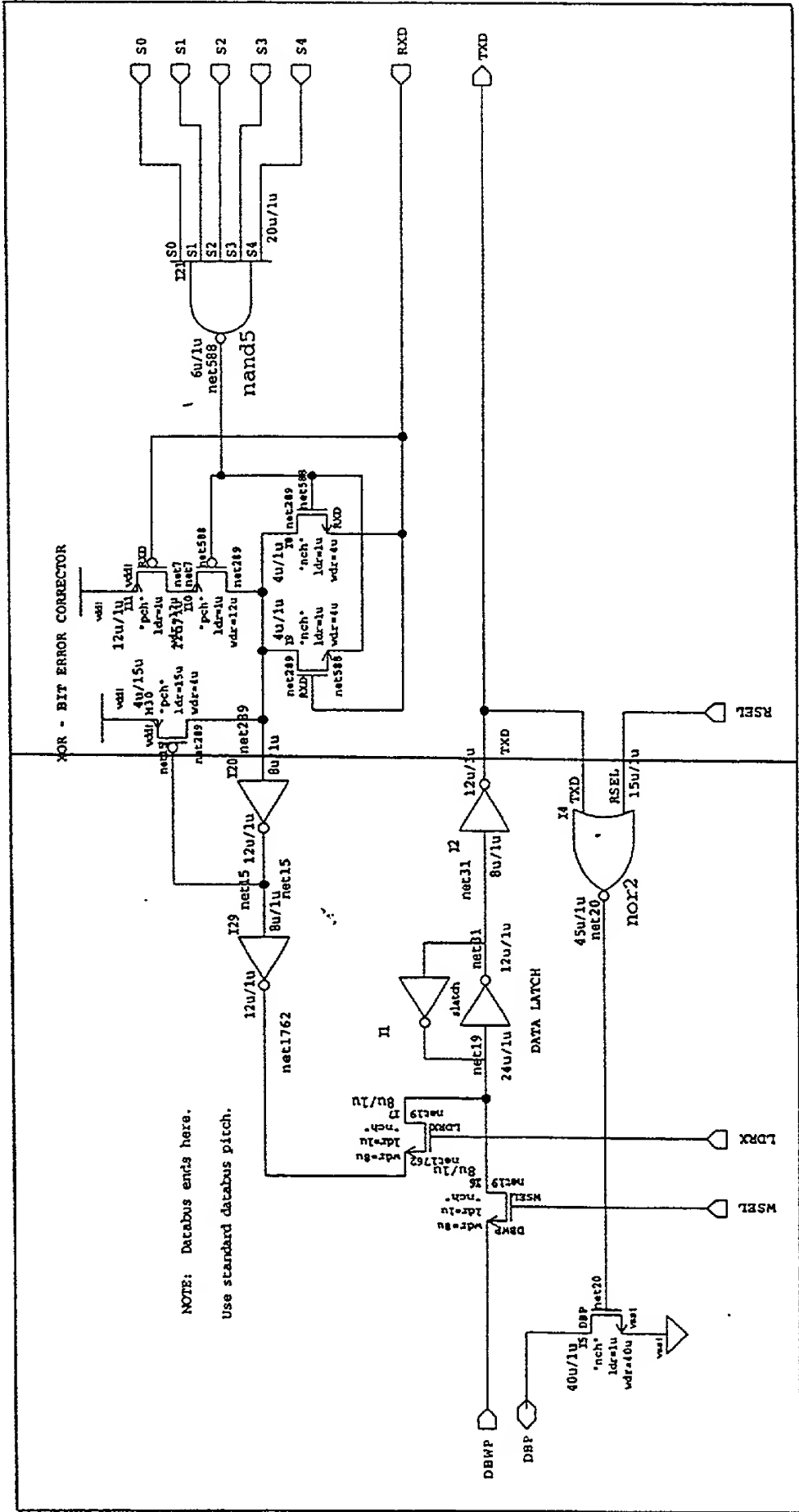


Fig. 7.1401 is a schematic diagram of a Micron integrated circuit. It shows a grid of data and address lines, storage elements, and control logic. The data lines are labeled D0 through D7, and the address lines are labeled A0 through A7. The circuit includes several storage elements, represented by rectangular blocks labeled "storage". These are organized into a grid structure. Control logic is shown at the bottom, including a "control logic" block and a "data detector" block. The diagram is labeled "Fig. 7.1401" in the top right corner. The Micron logo is visible in the bottom right corner, along with the text "MICRON TECHNOLOGY CORPORATION" and "INTEGRATED CIRCUIT DESIGN".

7.140101AA	7.140101AB
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MICRON		PRODUCT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Serial I/O Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/sioreg	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 1 18:03:52 1994	SHEET: A

Fig. 7.140101

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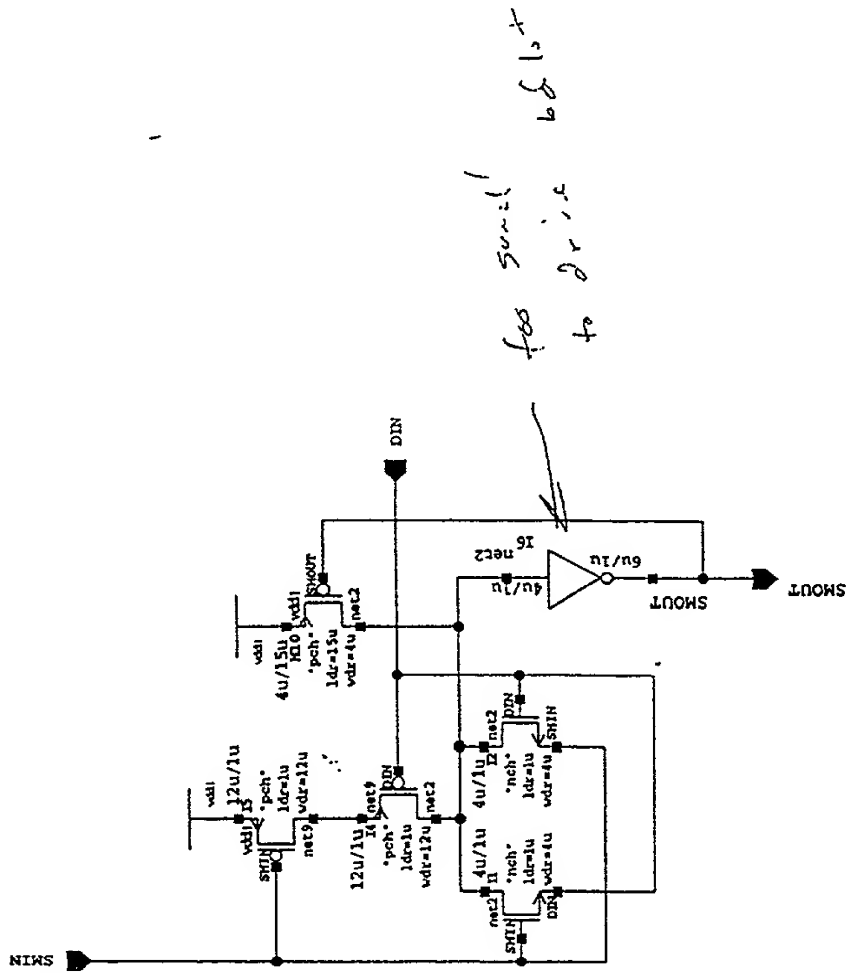


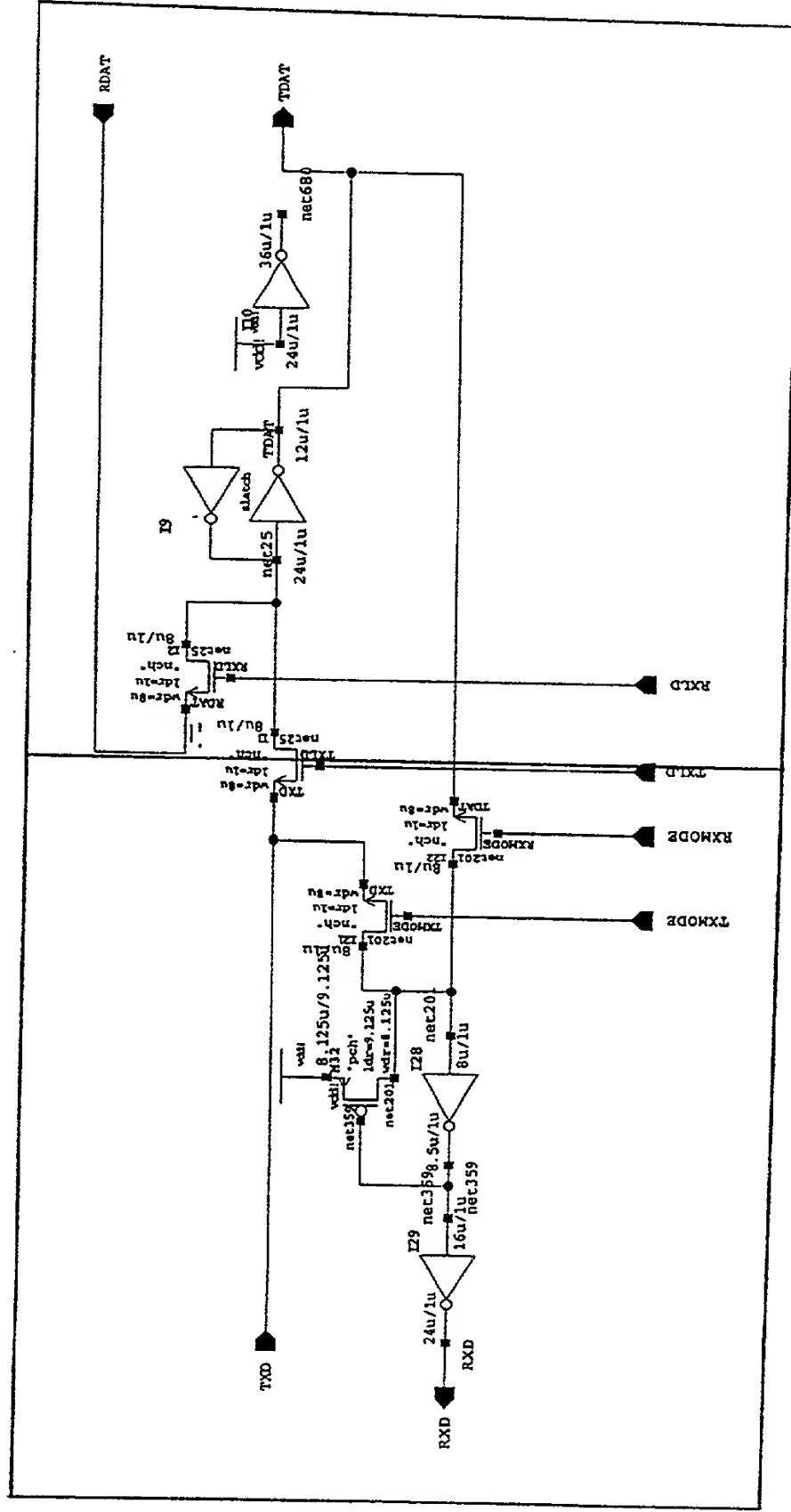
Fig. 7.140102

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: SIO XOR	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/sioxor	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 1 18:07:22 1994	SHEET: A

7.140103AB

ЕДИНЪОТЪ ЛЪХЪ

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DATE 08-01-2001 BY 60322 UCBAW/BJS



B11: inverted bit

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: SIO Bidirectional Latch			
NAME: 103reva/siobdlat_inv		REV: B11	SIZE: A
DATE: Apr 10 15:13:59 1996		SHEET:	

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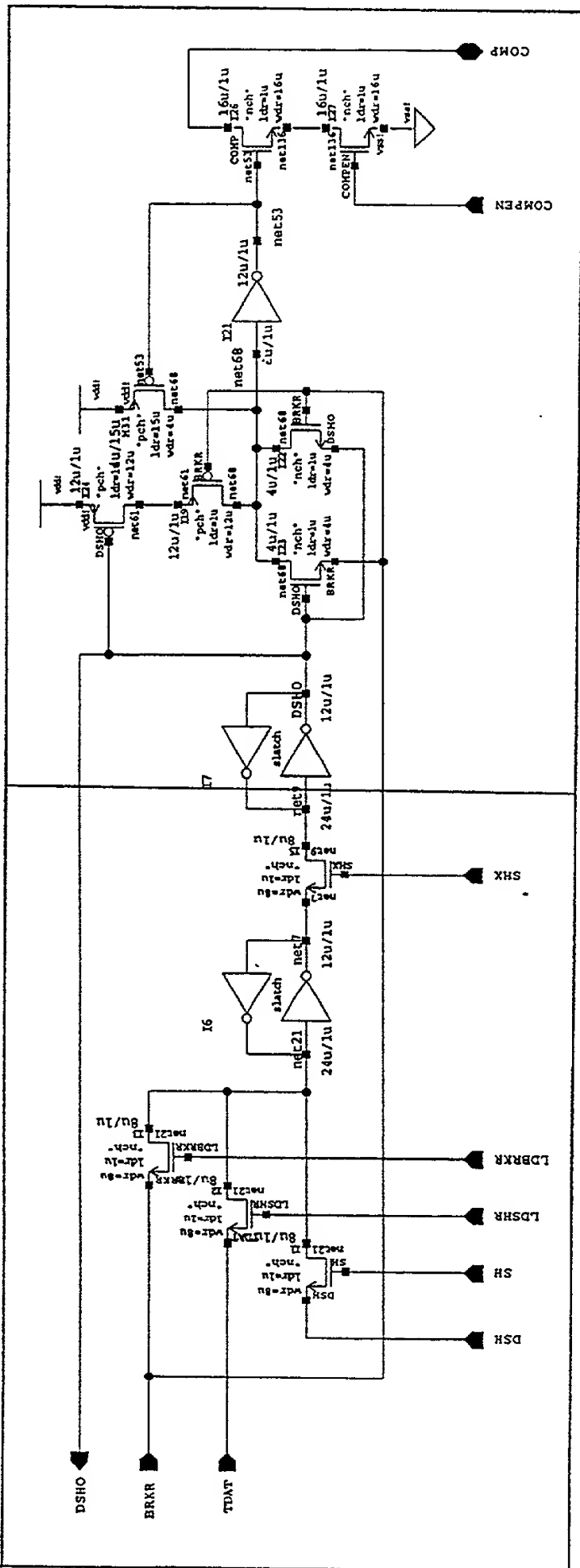
Fig. 7.140103

7.140104AB

7.140104AA

II II II II II II II II

7.140104

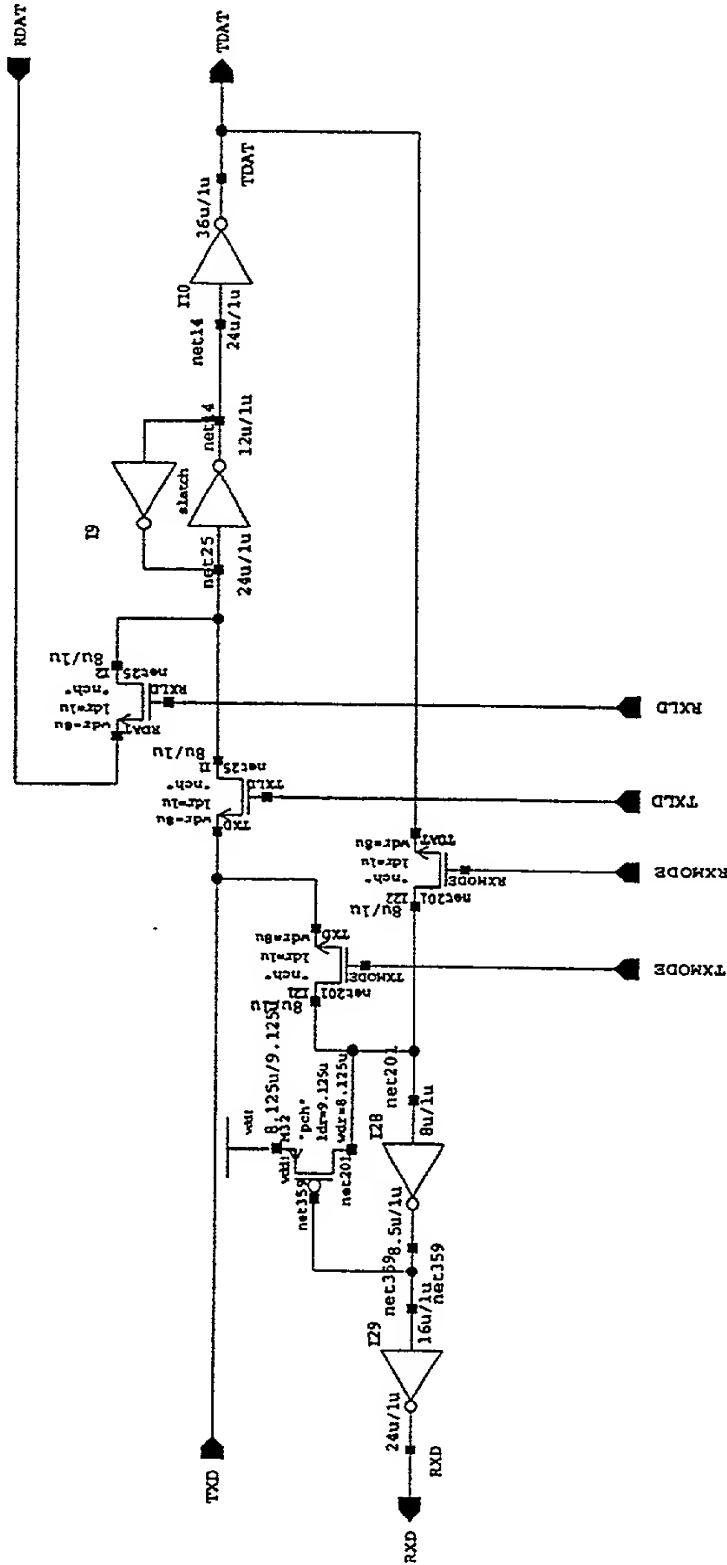


7.140104
FIG. 7.140104

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: SIO Shift Register			
NAME: 103reva/sioshr		REV: B1	SIZE: A
DATE: Sep 2 08:06:26 1994		SHEET: 1	

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PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: SIO Bidirectional Latch			
NAME: 103reva/siobdlat		REV: B8	
DATE: Jan 8 11:04:57 1996		SHEET: A	

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 COMMUNICATIONS, INC.
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B8: added feedback device

Fig. 7.140105

	7.1402AC	7.1402AD	7.1402AE	7.1402AF	7.1402AG	7.1402AH	7.1402AI
7.1402BA	7.1402BB	7.1402BC	7.1402BD	7.1402BE	7.1402BF	7.1402BH	7.1402BI
7.1402CA	7.1402CB	7.1402CC	7.1402CD	7.1402CE	7.1402CF	7.1402CH	7.1402CI
7.1402DA	7.1402DB	7.1402DC	7.1402DD	7.1402DE	7.1402DF	7.1402DH	7.1402DI
7.1402EA	7.1402EB	7.1402EC	7.1402ED	7.1402EE	7.1402EF	7.1402EH	7.1402EI

FIG. 7.1402

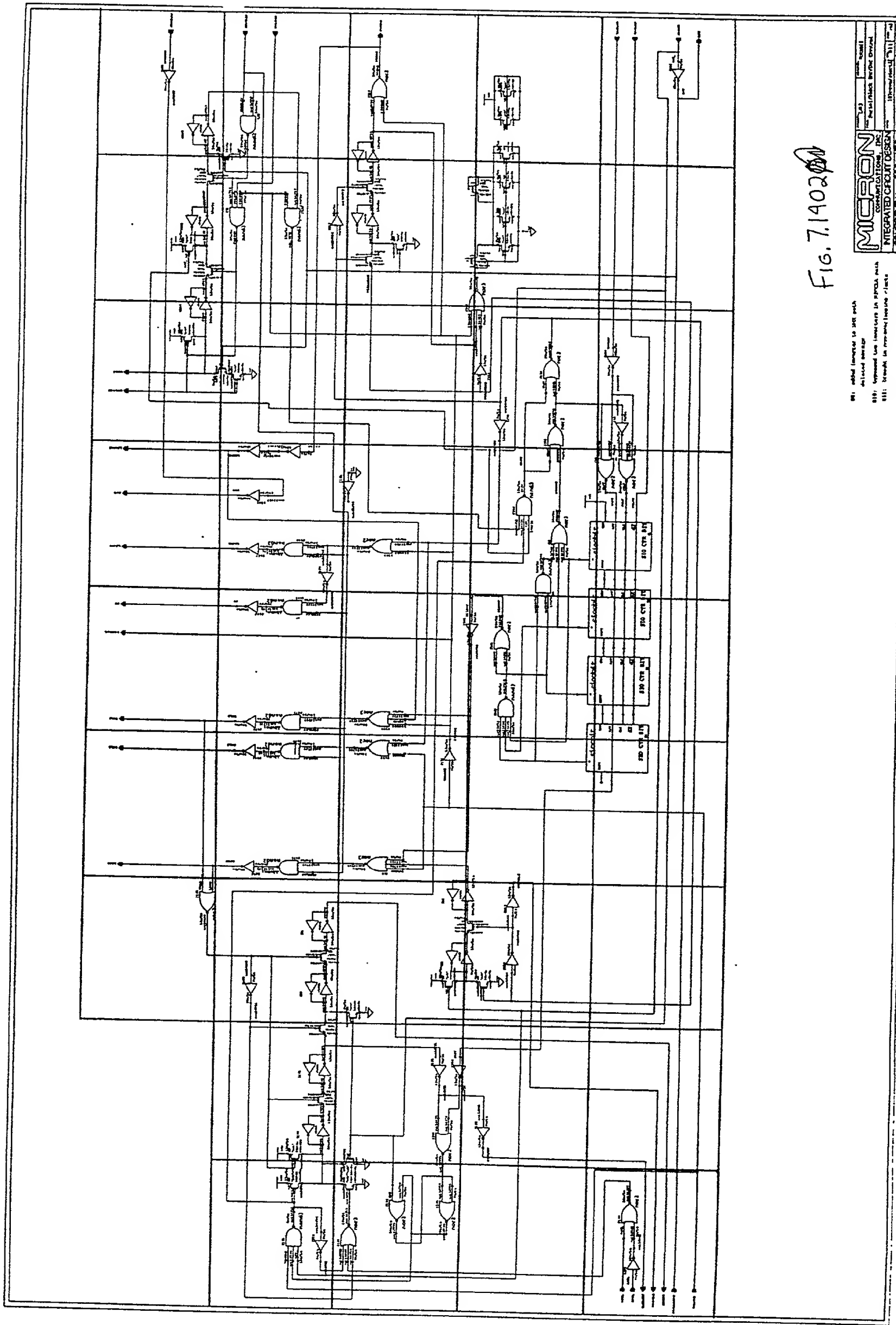


FIG. 7.1402

801: added (sample to set pin)
 802: added (sample to set pin)
 803: updated the (sample to set pin)
 804: changed in (sample to set pin)

MICRON	
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DATE: 10/11/81	BY: [signature]

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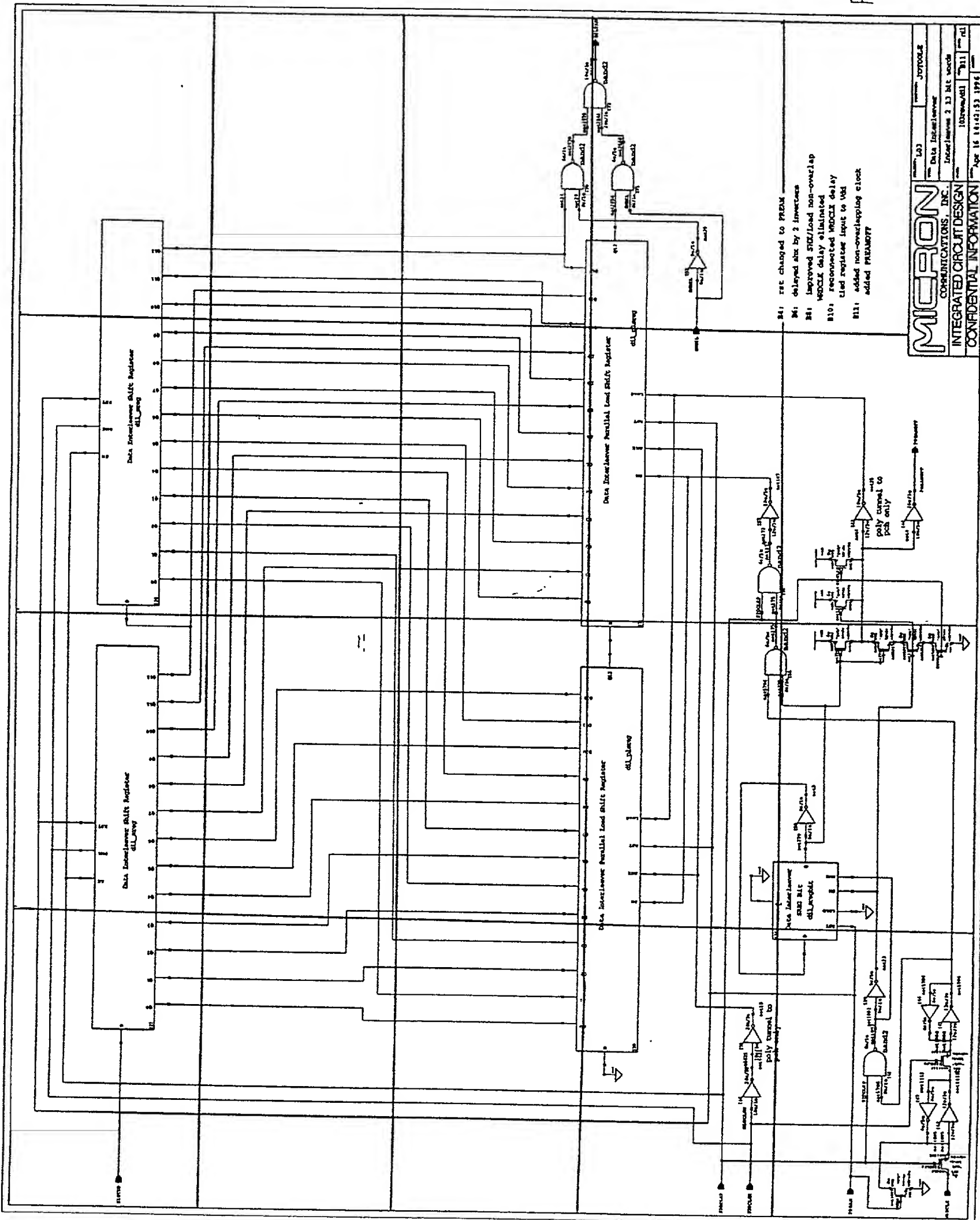


Fig. 7.15

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Part No.	100000000
Rev.	1.0
Date	10/20/96
Drawn by	100000000
Checked by	100000000
Approved by	100000000

- 24: TSC changed to PREAM
- 25: delayed shift by 2 inverters
- 26: improved STC/load non-overlap
- 27: WDCX delay eliminated
- 28: reconnected WDCX delay
- 29: added non-overlapping clock
- 30: added PREAM077

7.1501AA

7.1501BA

7.1501CA

II II II 7.1501

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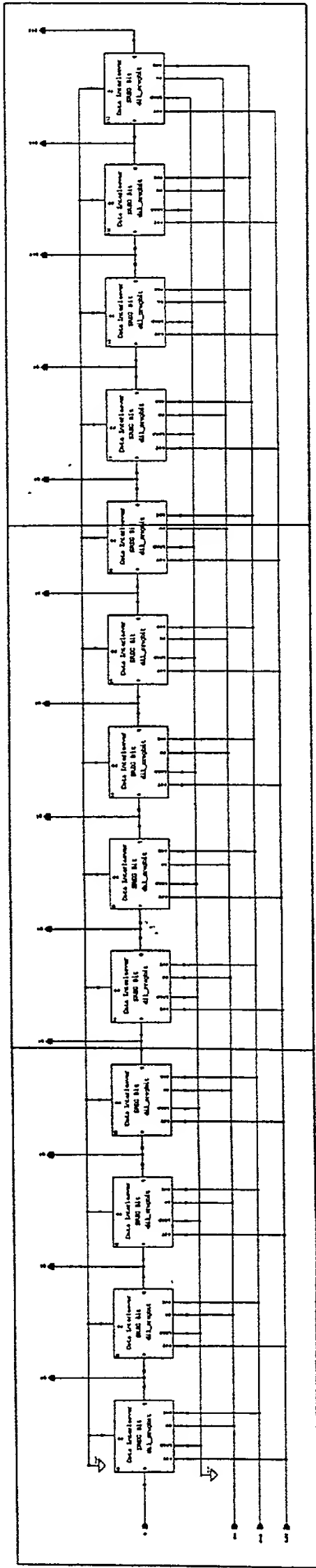


Fig. 7.1501

7.1502AA

7.1502BA

7.1502CA

See 7.1502

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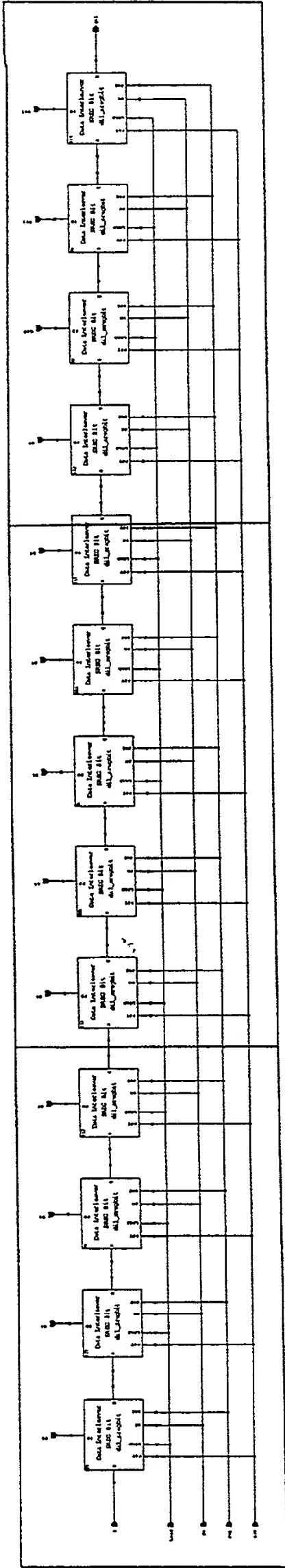


FIG. 7.1502

III

FIG. 7.150201

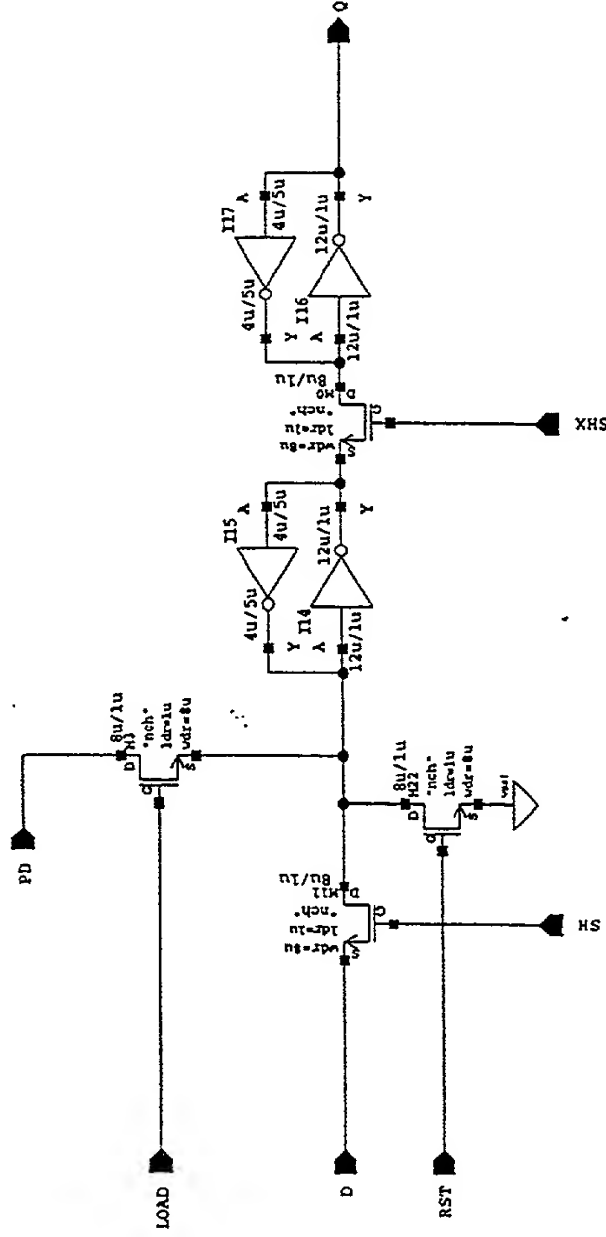
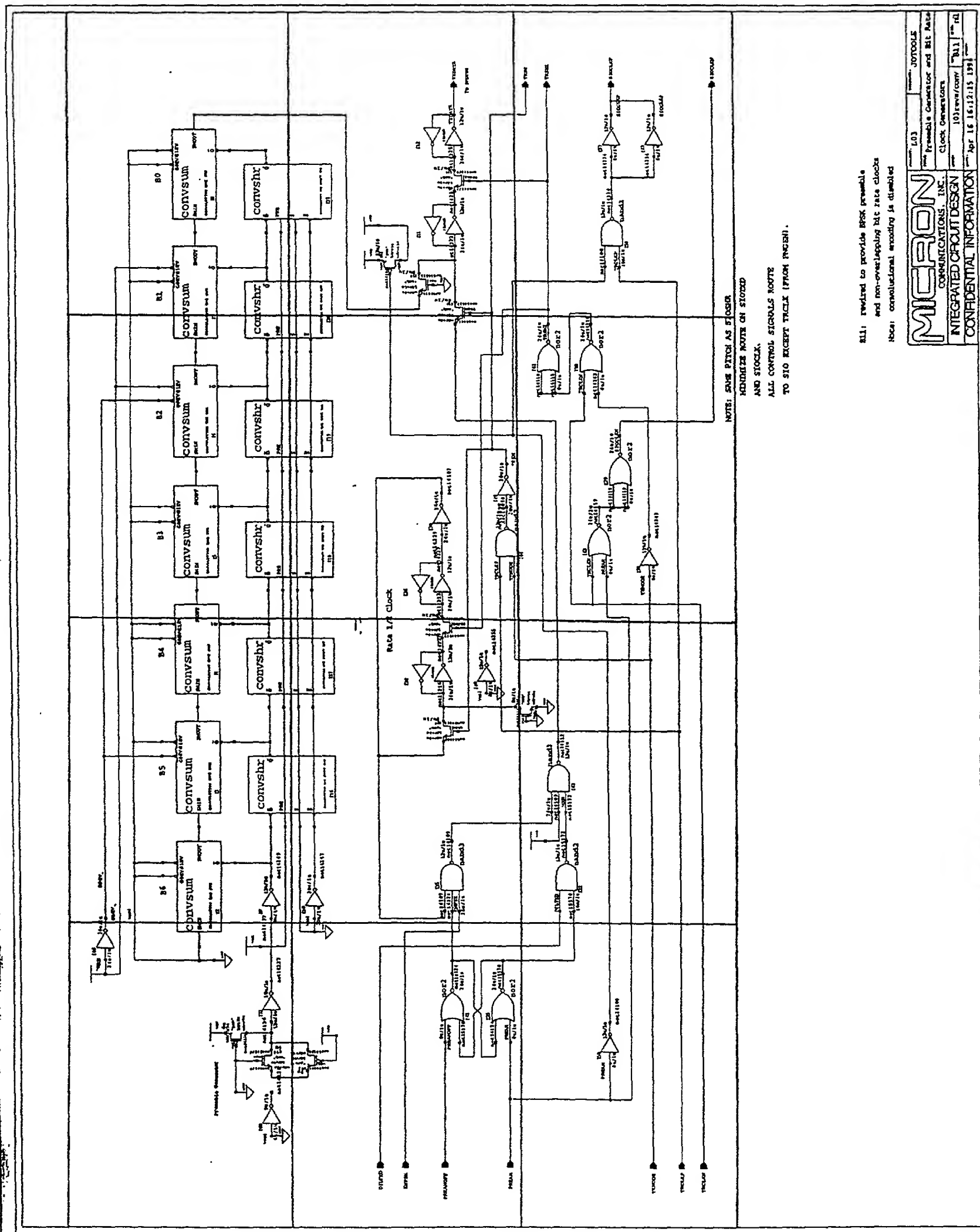


Fig. 7.150201

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Data Interleaver Shift		Register Bit	
NAME: 103reva/dil_sregbit		REV: B1	SIZE: A
DATE: Sep 27 10:25:07 1994		SHEET: 1	

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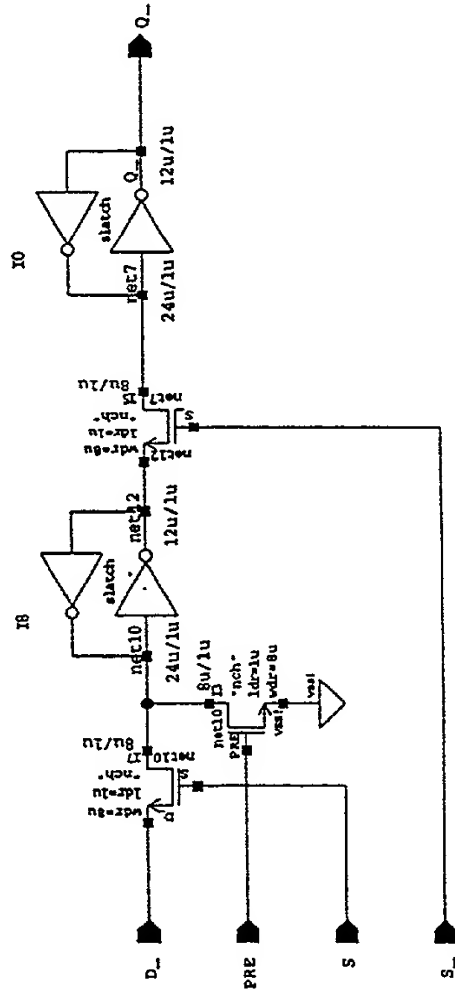


Fig. 7.1601

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Convolutional Encoder Shift		Register Cell	
NAME: 103reva/convshr	REV: A	SIZE: A	
DATE: Sep 2 10:34:27 1994		SHEET: 1	

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

7.17AA	7.17AB
7.17BA	7.17BB

FIG. 7.17

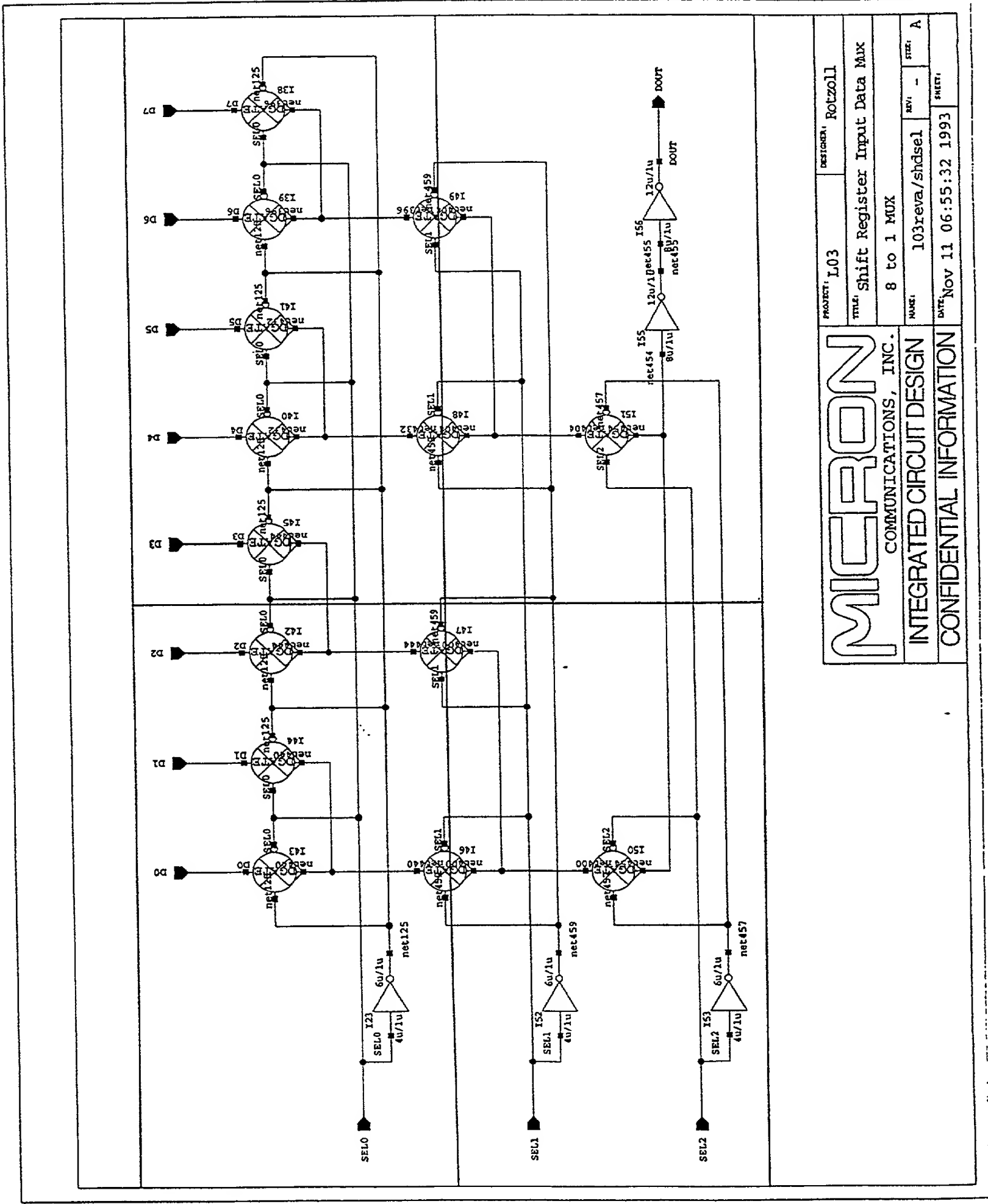


Fig. 7.17

7.18AA	7.18AB	7.18AC
7.18BA	7.18BB	7.18BC
7.18CA	7.18CB	7.18CC

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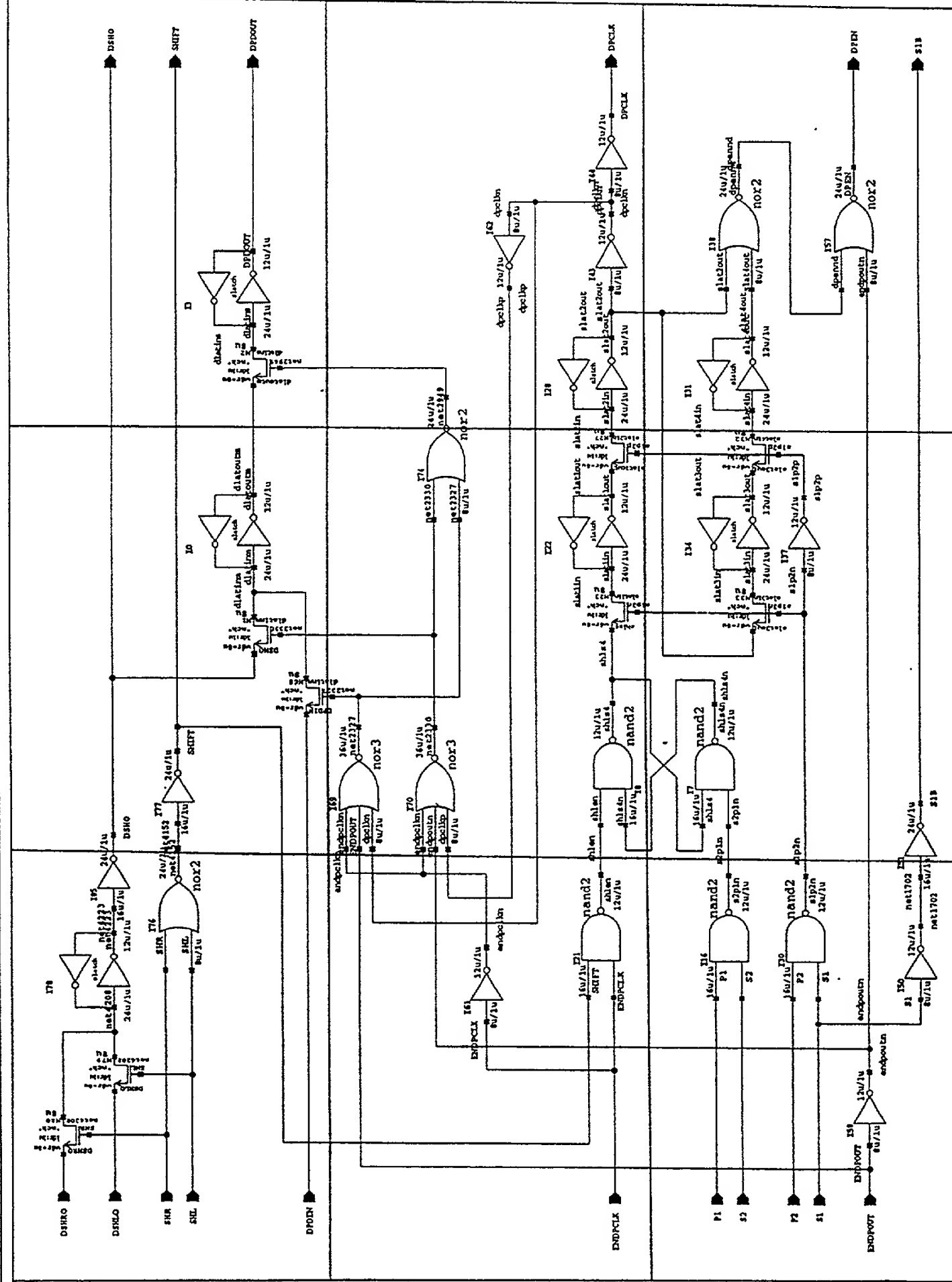
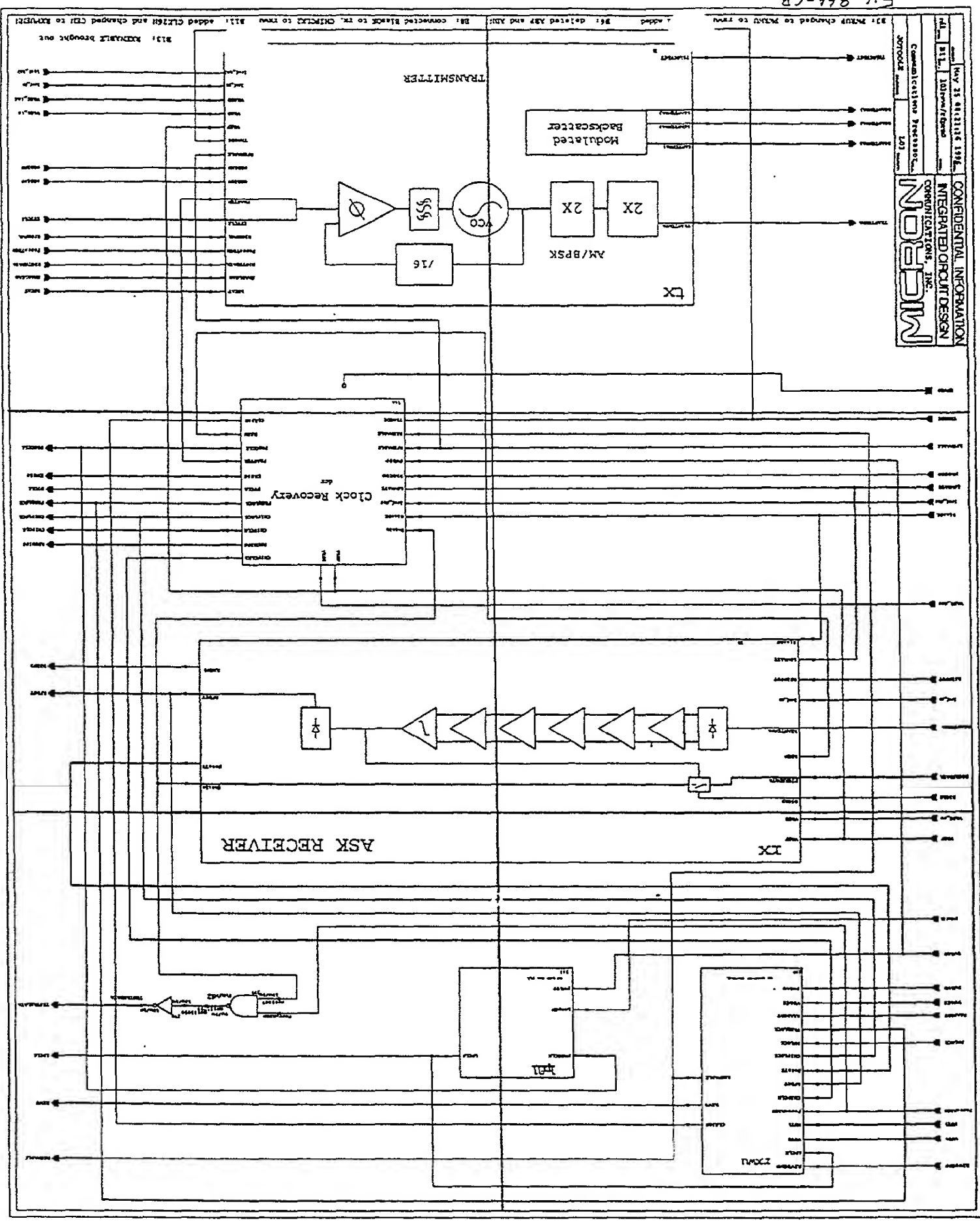


Fig. 7.18

PROJECT: L03		DESIGN: Rotzoll	
TITLE: Digital Port Output Controller			
NAME: 103reva/doutport		REV: -	DATE: nil
CONFIDENTIAL INFORMATION		Nov 12 10:05:40 1993	

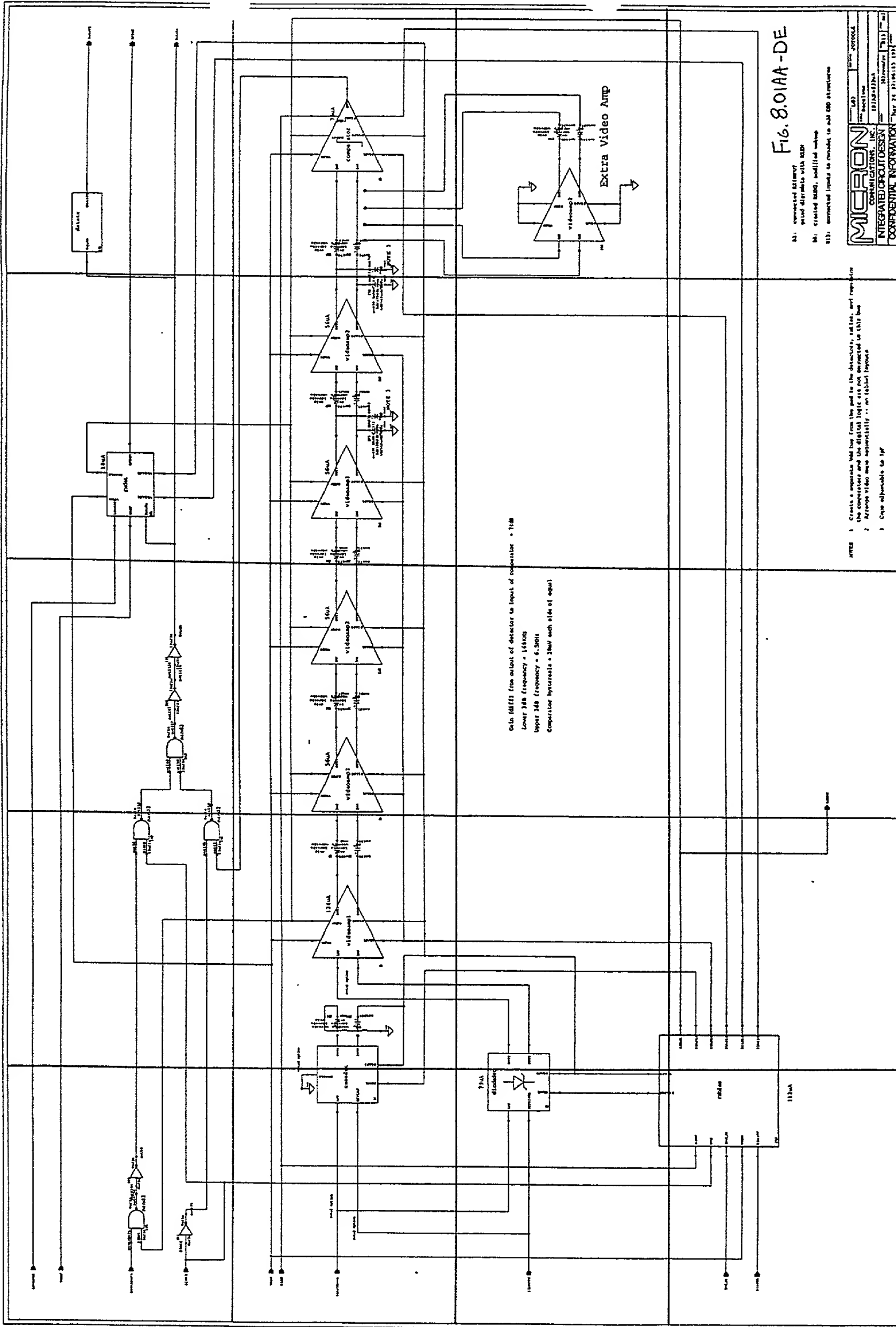
8AA	8AB
8BA	8BB
8CA	8CB



16.84A-CB

8.01AA	8.01AB	8.01AC	8.01AD	8.01AE
8.01BA	8.01BB	8.01BC	8.01BD	8.01BE
8.01CA	8.01CB	8.01CC	8.01CD	8.01CE
8.01DA	8.01DB	8.01DC	8.01DD	8.01DE

1. Connect the output of the detector to the input of the comparator.
 2. Connect the output of the comparator to the input of the video amplifier.
 3. Connect the output of the video amplifier to the input of the extra video amplifier.
 4. Connect the output of the extra video amplifier to the output of the circuit.



Gain (diff) from output of detector to input of comparator = 110k
 Lower 3dB frequency = 1.6kHz
 Upper 3dB frequency = 6.5kHz
 Capacitor hysteresis = 2mV each side of equal

Fig. 8.01AA-DE

- 1. Connect the output of the detector to the input of the comparator.
- 2. Connect the output of the comparator to the input of the video amplifier.
- 3. Connect the output of the video amplifier to the input of the extra video amplifier.
- 4. Connect the output of the extra video amplifier to the output of the circuit.

MICRON	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
DATE	1971-01-15
DESIGNED BY	1011
CHECKED BY	1011
APPROVED BY	1011

NOTES: 1. Circuit requires VDD from the pad to the detector, video, and comparator.
 2. The comparator and the digital logic are not connected to this bus.
 3. Across video bus approximately 100k resistor.
 4. Caps adjustable to 10pF.

MI40-030

8.0101AA	8.0101AB
8.0101BA	8.0101BB
8.0101CA	8.0101CB

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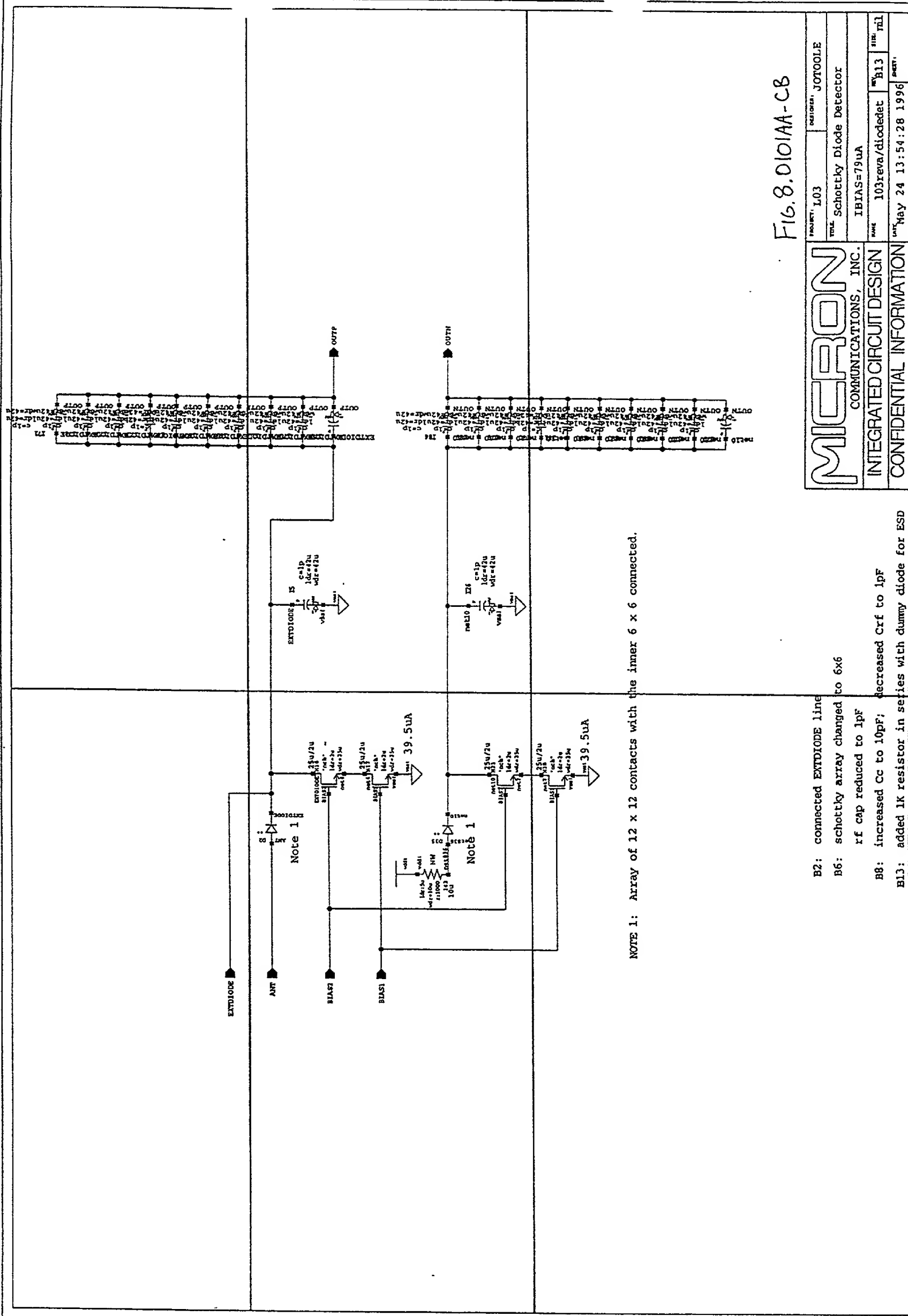


FIG. 8.0101AA-CB

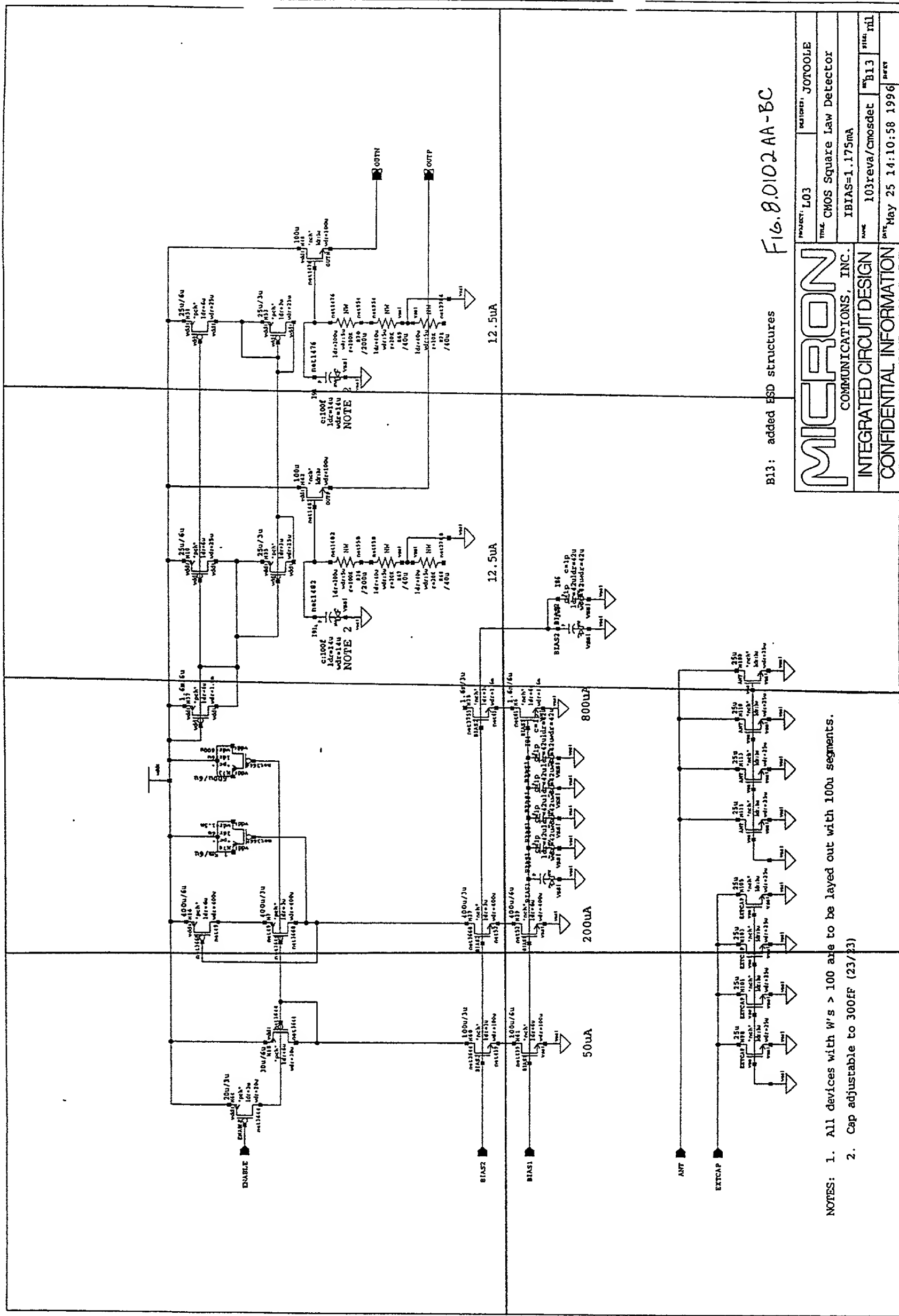
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Schottky Diode Detector	
INTEGRATED CIRCUIT DESIGN		IBIAS=79uA	
CONFIDENTIAL INFORMATION		NAME: 103reva/diodedet	REV: B13
		DATE: May 24 13:54:28 1996	BY: ml

MI40-030

8.0102AA	8.0102AB	8.0102AC	8.0102AD
8.0102BA	8.0102BB	8.0102BC	

MI40-030

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MICRON		PROJECT: J0700LE
COMMUNICATIONS, INC.		TIME: CMOS Square Law Detector
INTEGRATED CIRCUIT DESIGN		YBIAS=1.175mA
CONFIDENTIAL INFORMATION		NAME: 103reva/cmosdet
		DATE: May 25 14:10:58 1996

1. resistors are to be layed out at 50/10 and
adjusted down to 39/10 with n+

2. p-channels are adjustable up to 5/100;
adjustment is on source side

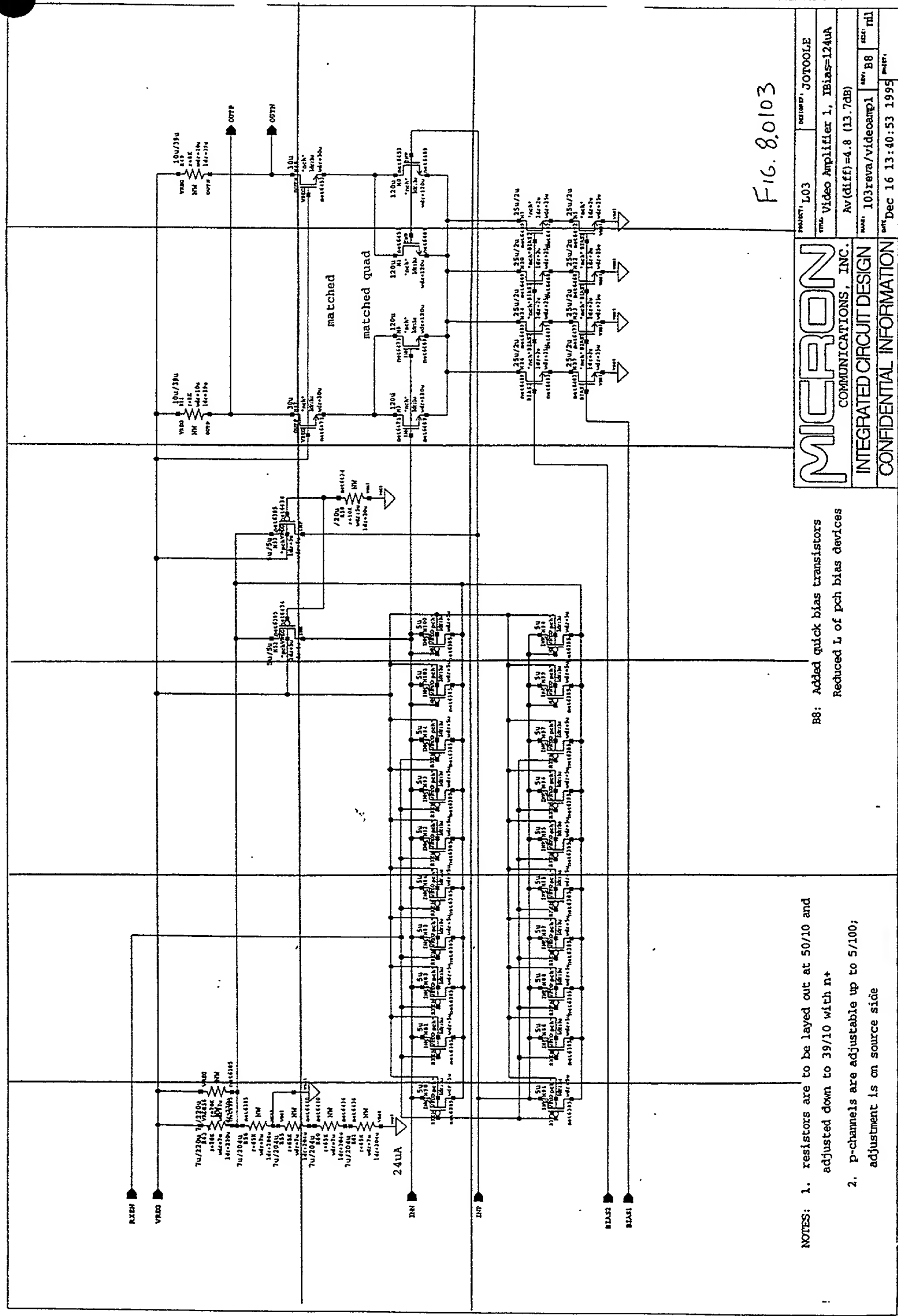


FIG. 8.0103

PROJECT L03		DESIGNED: JOT001LE	
TITLE: Video Amplifier 1, IBias=124uA		AV(dB)=4.8 (13.7dB)	
DATE: 103revA/videoamp1		REV: B8	
DATE: Dec 16 13:40:53 1995		BY: rdl	

NOTES: 1. resistors are to be layed out at 50/10 and
adjusted down to 39/10 with n+

2. p-channels are adjustable up to 5/100;
adjustment is on source side

B8: Added quick bias transistors
Reduced L of pch bias devices

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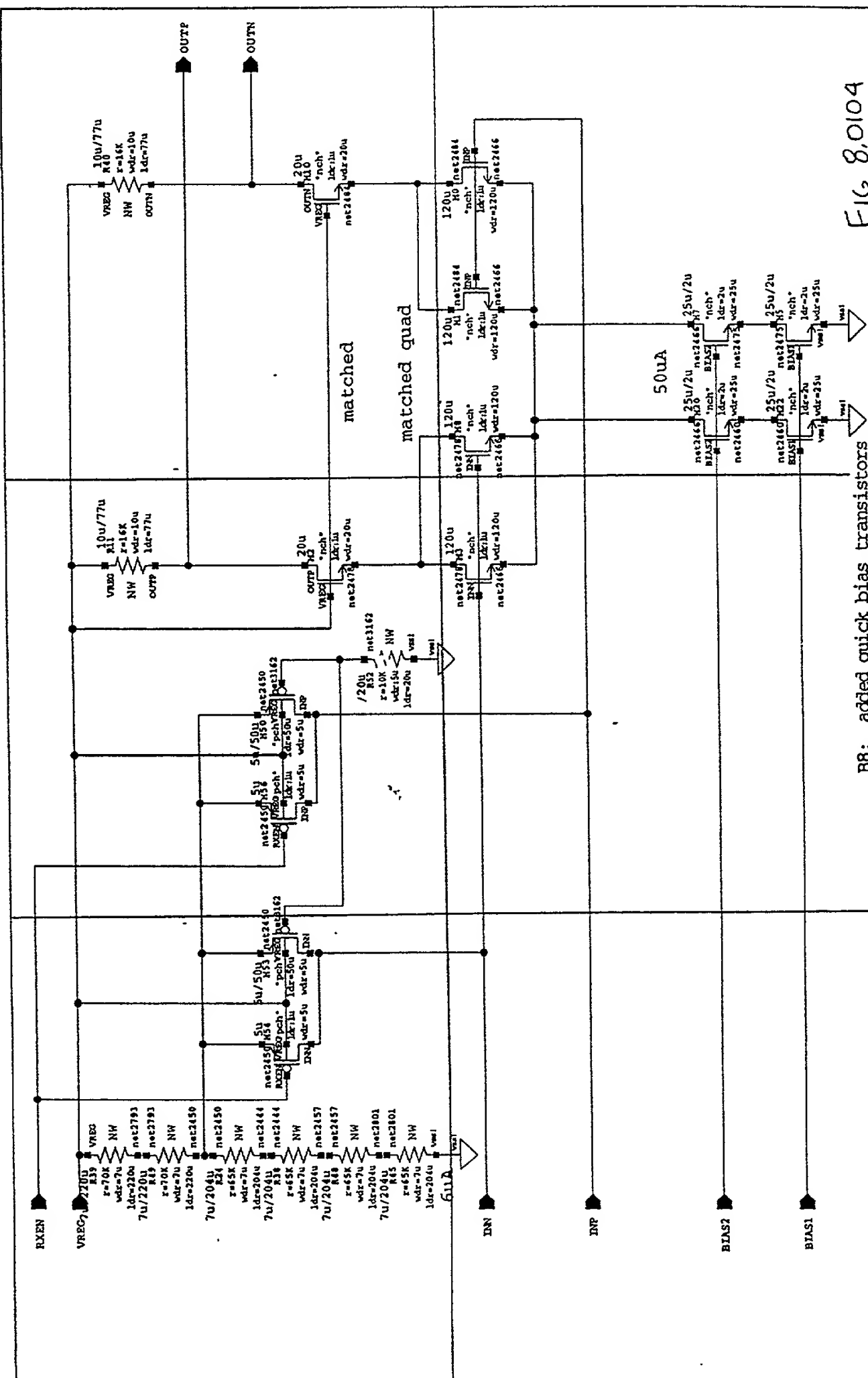


Fig 8.0104

B8: added quick bias transistors

- NOTES:
1. resistors are to be layed out at 100/10 and adjusted down to 77/10 with n+
 2. p-channels are adjustable up to 5/100; adjustment is on the source side.

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Video Amplifier 2, IBias=56uA	
INTEGRATED CIRCUIT DESIGN		AV(diff)=5.6 (15dB)	REV: B8
CONFIDENTIAL INFORMATION		DATE: Dec 16 13:42:25 1995	SIZE: A

8.0105AA	8.0105AB	8.0105AC	8.0105AD	
8.0105BA	8.0105BB	8.0105BC	8.0105BD	
8.0105CA	8.0105CB	8.0105CC	8.0105CD	8.0105CE
8.0105DA	8.0105DB	8.0105DC	8.0105DD	8.0105DE
8.0105EA	8.0105EB	8.0105EC	8.0105ED	

8.0106AA	8.0106AB	8.0106AC	8.0106AD
8.0106BA	8.0106BB	8.0106BC	8.0106BD
8.0106CA	8.0106CB	8.0106CC	8.0106CD

EE 88.00.11.00.15

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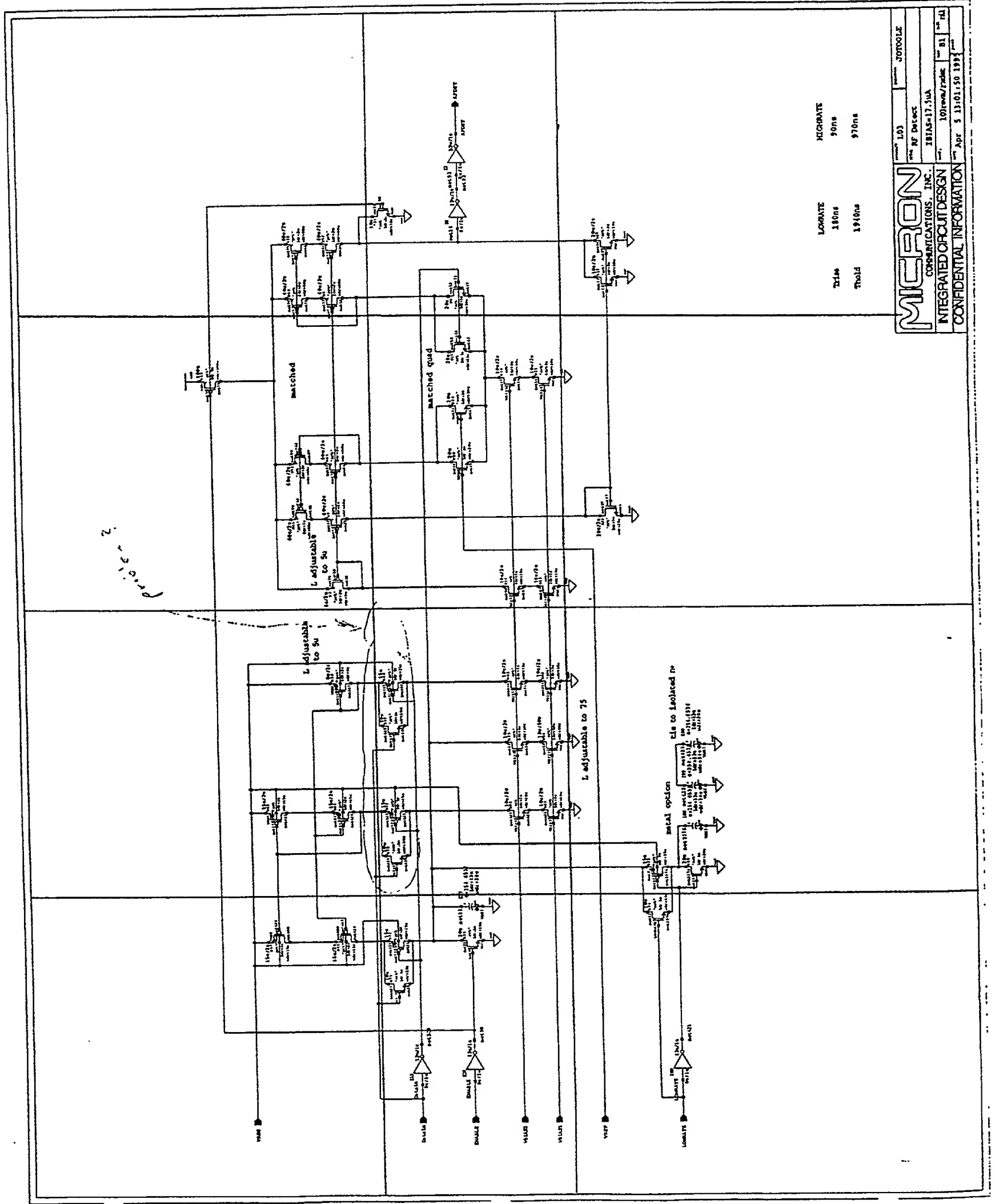


FIG. 8.0106

8.0107AA 8.0107AB 8.0107AC 8.0107AD 8.0107AE 8.0107AF 8.0107AG 8.0107AH 8.0107AI 8.0107AJ 8.0107AK 8.0107AL 8.0107AM

8.0107AA	8.0107AB	8.0107AC	8.0107AD	8.0107AE	8.0107AF	8.0107AG	8.0107AH	8.0107AI	8.0107AJ	8.0107AK	8.0107AL	8.0107AM
8.0107BA	8.0107BB	8.0107BC	8.0107BD	8.0107BE	8.0107BF	8.0107BG	8.0107BH	8.0107BI	8.0107BJ	8.0701BK	8.0107BL	8.0107BM
8.0107CA	8.0107CB	8.0107CC	8.0107CD	8.0107CE	8.0107CF	8.0107CG	8.0107CH	8.0107CI	8.0107CJ	8.0107CK	8.0107CL	8.0107CM
8.0107DA	8.0107DB	8.0107DC	8.0107DD	8.0107DE	8.0107DF	8.0107DG	8.0107DH	8.0107DI	8.0107DJ	8.0107DK	8.0107DL	8.0107DM
8.0107EA	8.0107EB	8.0107EC	8.0107ED	8.0107EE	8.0107EF	8.0107EG	8.0107EH	8.0107EI	8.0107EJ	8.0107EK	8.0107EL	8.0107EM
8.0107FA	8.0107FB	8.0107FC	8.0107FD	8.0107FE	8.0107FF	8.0107FG	8.0107FH	8.0107FI	8.0107FJ	8.0107FK	8.0107FL	8.0107FM
8.0107GA	8.0107GB	8.0107GC	8.0107GD	8.0107GE	8.0107GF	8.0107GG	8.0107GH	8.0107GI	8.0107GJ	8.0107GK	8.0107GL	8.0107GM
												8.0107GN

8.0107HN 8.0107HO 8.0107HP 8.0107HQ 8.0107HR 8.0107HS 8.0107HT 8.0107HU 8.0107HV 8.0107HW 8.0107HX 8.0107HY 8.0107HZ

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED

8.0108AA	8.0108AB	8.0108AC
----------	----------	----------

8.02AA	8.02AB	8.02AC
8.02BA	8.02BB	8.02BC

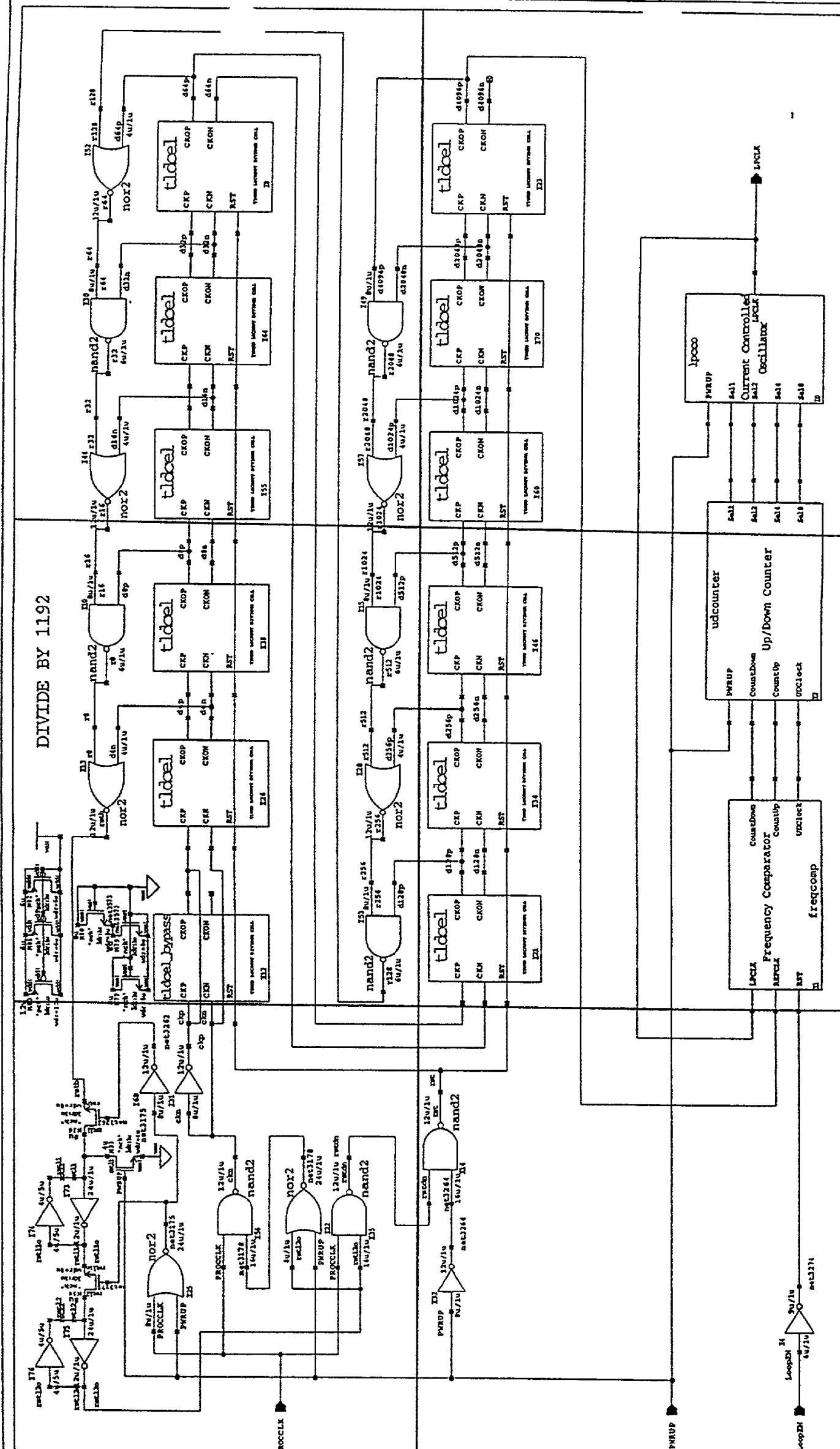


Fig. 8.02

H10: first divider stage bypassed

MICRON		PRODUCT: L03	DESIGNER: JOTCOOLE
COMMUNICATIONS, INC.		TITLE: Low Power FLL (1sb=55na typ)	
INTEGRATED CIRCUIT DESIGN		fin=9.5375MHz/fout=8000Hz	
CONFIDENTIAL INFORMATION		DATE: 103rev-a/lpfl	REV: B10
		DATE: Mar 26 16:14:18 1996	

CONFIDENTIAL

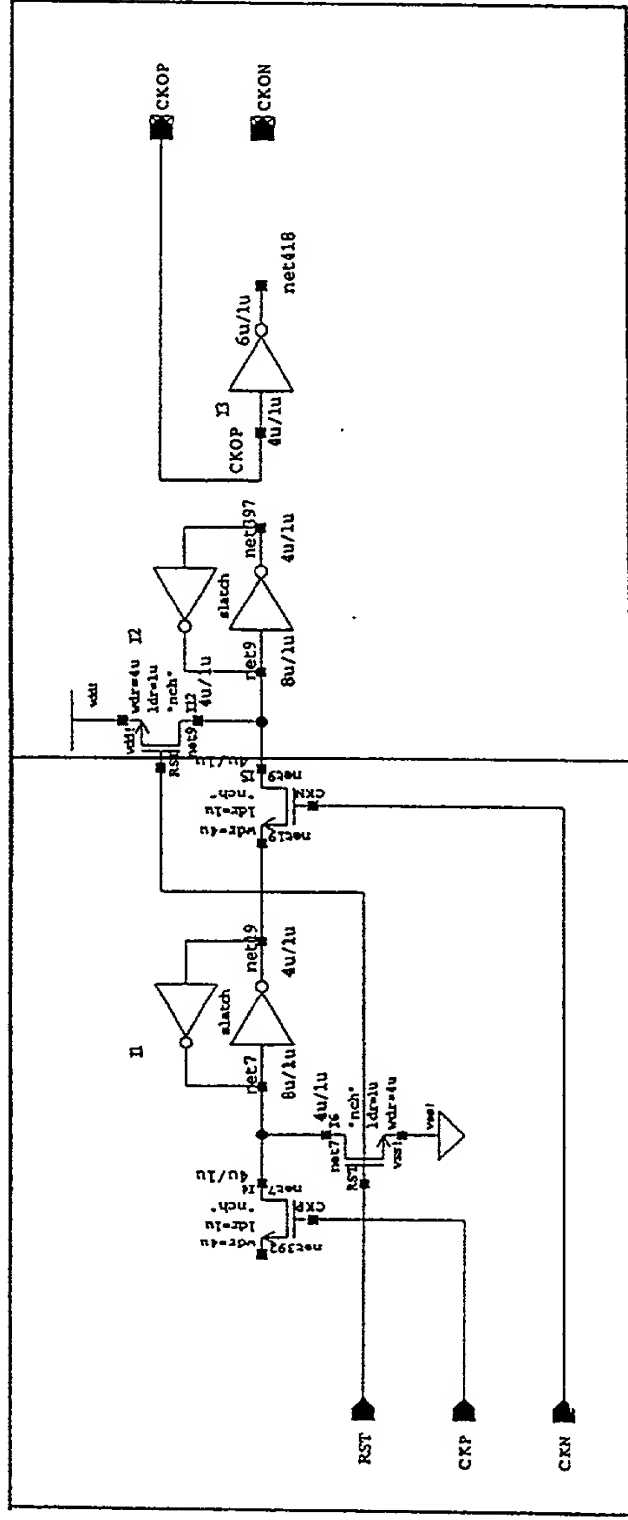


Fig. 8.0201

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Timed Lockout Divider Cell	
INTEGRATED CIRCUIT DESIGN		REV: I03reva/tldcel_bypass	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Mar 26 13:54:47 1996	SHEET: B10

B10: new cell to bypass 1st counter stage



Fig. 8.0202

[illegible]

8.0203AA	8.0203AB	8.0203AC
8.0203BA	8.0203BB	8.0203BC

8.020301AA 8.020301AB 8.020301BA 8.020301BB

MI40-030

8.020301AA	8.020301AB
8.020301BA	8.020301BB

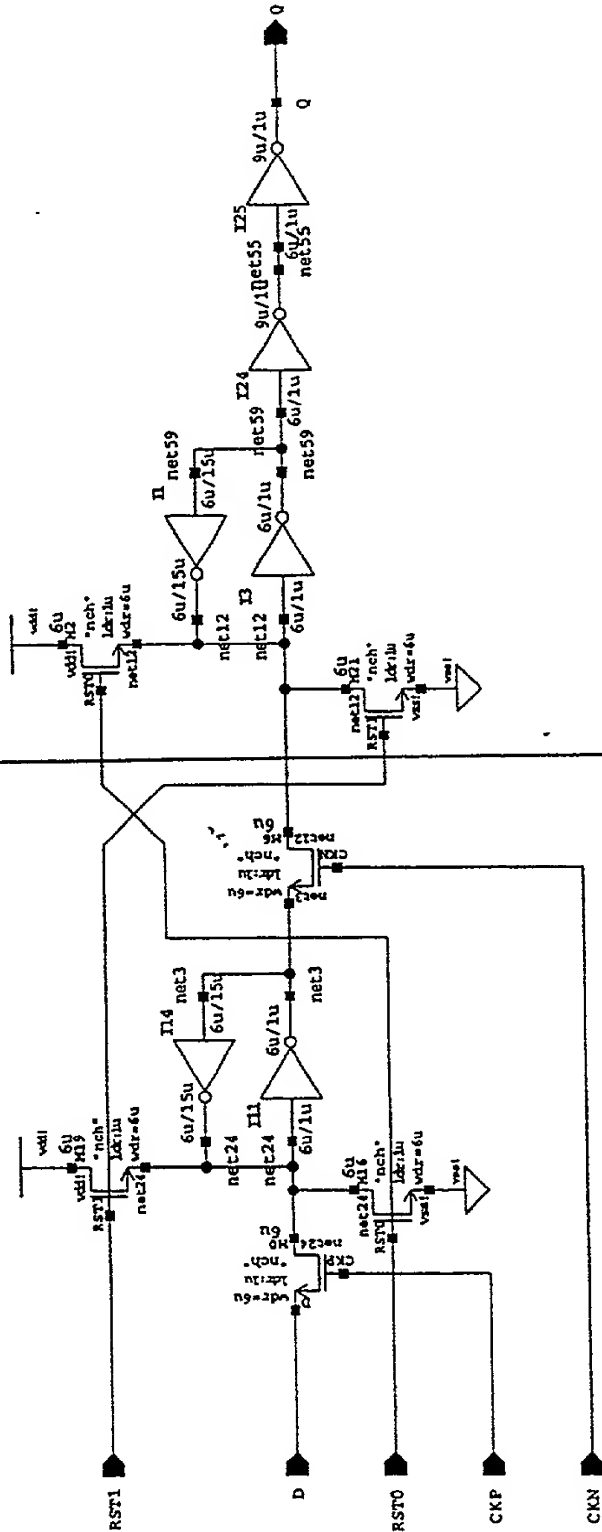
8.020301AA 8.020301AB 8.020301BA 8.020301BB

8.020302AB

8.020302AA

8.020302

100% Design Rule Check (DRC) Passed
100% LVS (Layout Versus Schematic) Check Passed
100% Timing Analysis Passed
100% Power Analysis Passed
100% Signal Integrity Analysis Passed
100% Parasitic Extraction Passed
100% Fabrication Tolerances Checked
100% Manufacturing Constraints Checked
100% Assembly Constraints Checked
100% Test Constraints Checked
100% Documentation Checked
100% Final Review Passed
100% Release to Manufacturing Passed



MICRON		PROJECT: L03		DESIGNER: JOTOOLE	
COMMUNICATIONS, INC.		TITLE: LPFLL U/D Counter D Flip Flop			
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/udcounter_dff		REV: B1	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:09:40 1994		SHEET: 1	

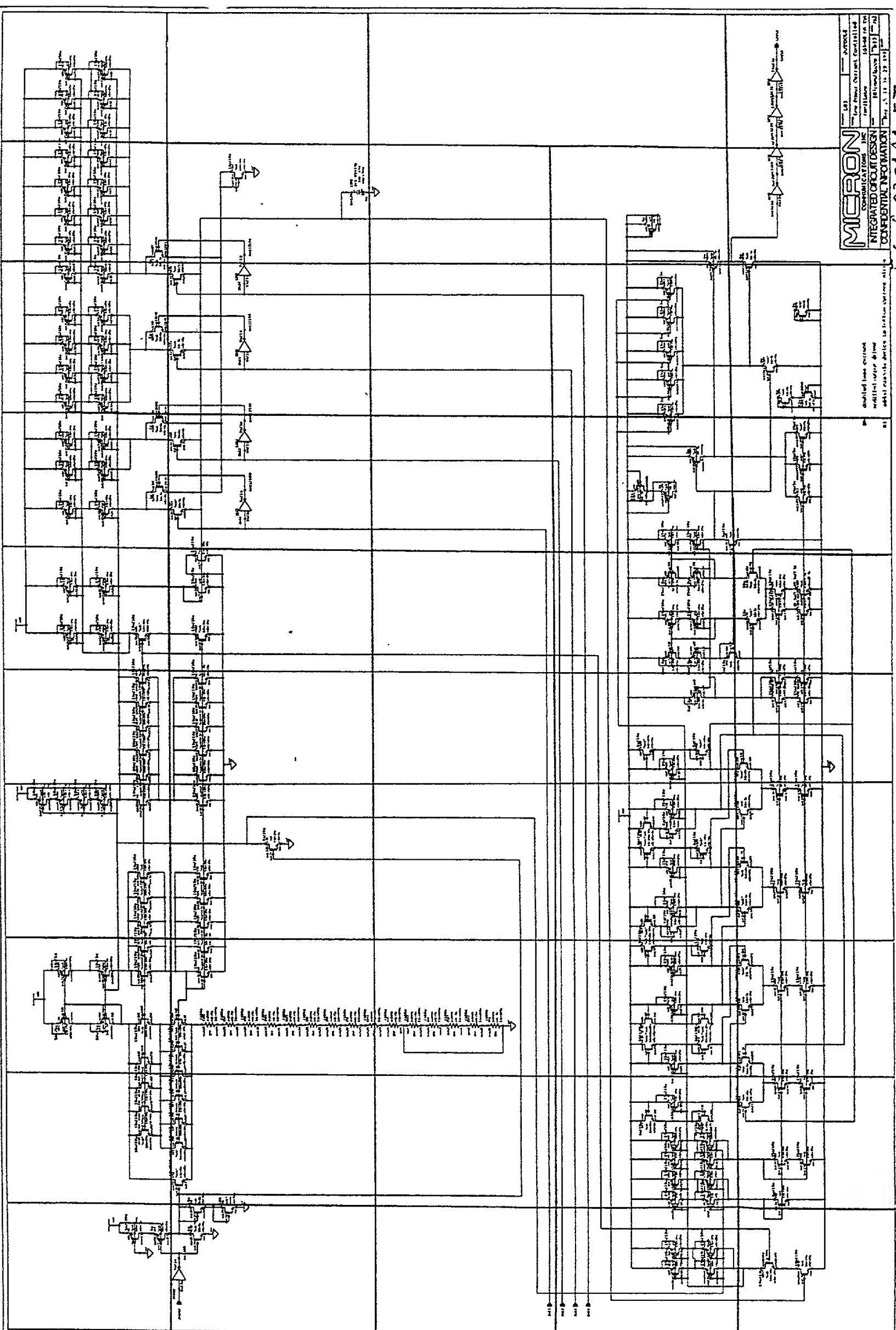
Fig. 8.020302

8.0204AA 8.0204AB 8.0204AC 8.0204AD 8.0204AE 8.0204AF 8.0204AG 8.0204AH 8.0204AI 8.0204AJ

8.0204AA	8.0204AB	8.0204AC	8.0204AD	8.0204AE	8.0204AF	8.0204AG	8.0204AH	8.0204AI	8.0204AJ
8.0204BA	8.0204BB	8.0204BC	8.0204BD	8.0204BE	8.0204BF	8.0204BG	8.0204BH	8.0204BI	8.0204BJ
8.0204CA	8.0204CB	8.0204CC	8.0204CD	8.0204CE	8.0204CF	8.0204CG	8.0204CH	8.0204CI	
8.0204DA	8.0204DB	8.0204DC	8.0204DD	8.0204DE	8.0204DF	8.0204DG	8.0204DH	8.0204DI	
8.0204EA	8.0204EB	8.0204EC	8.0204ED	8.0204EE	8.0204EF	8.0204EG	8.0204EH	8.0204EI	8.0204EJ

8.0204FA 8.0204FB 8.0204FC 8.0204FD 8.0204FE 8.0204FF 8.0204FG 8.0204FH 8.0204FI 8.0204FJ

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MICRON
COMMUNICATIONS
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

DESIGNED BY	DATE
DESIGNED BY	DATE
DESIGNED BY	DATE
DESIGNED BY	DATE

doublet line circuit
with input delay
added variable device in location system

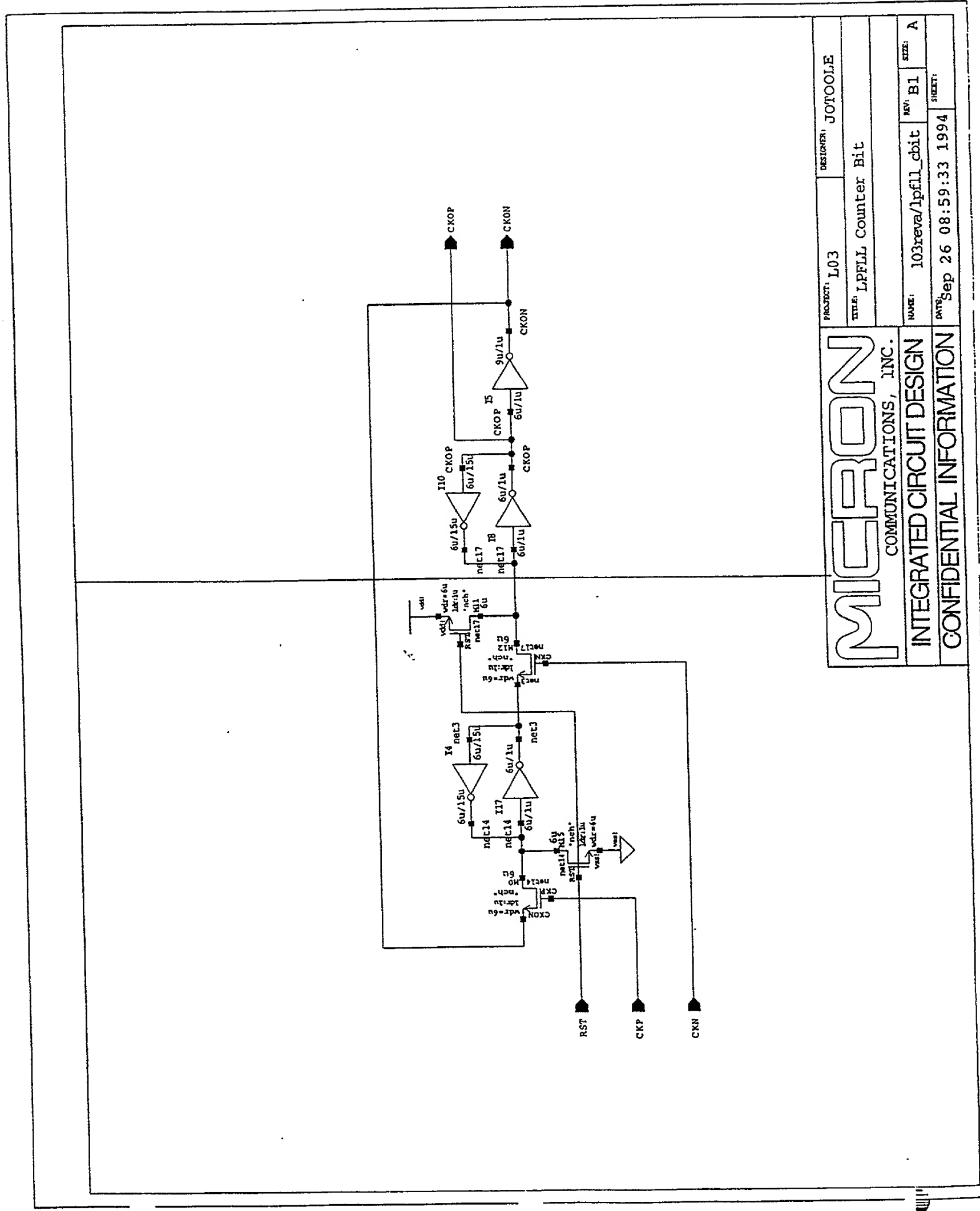
F.9. 8.020AA-EJ

8.03AB

8.03AA

LEWIS & CLARK

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DATE 08-09-2001 BY 60322 UCBAW/BJS



MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: LPFLL Counter Bit	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/lpfll_cbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 26 08:59:33 1994	SIZE: A

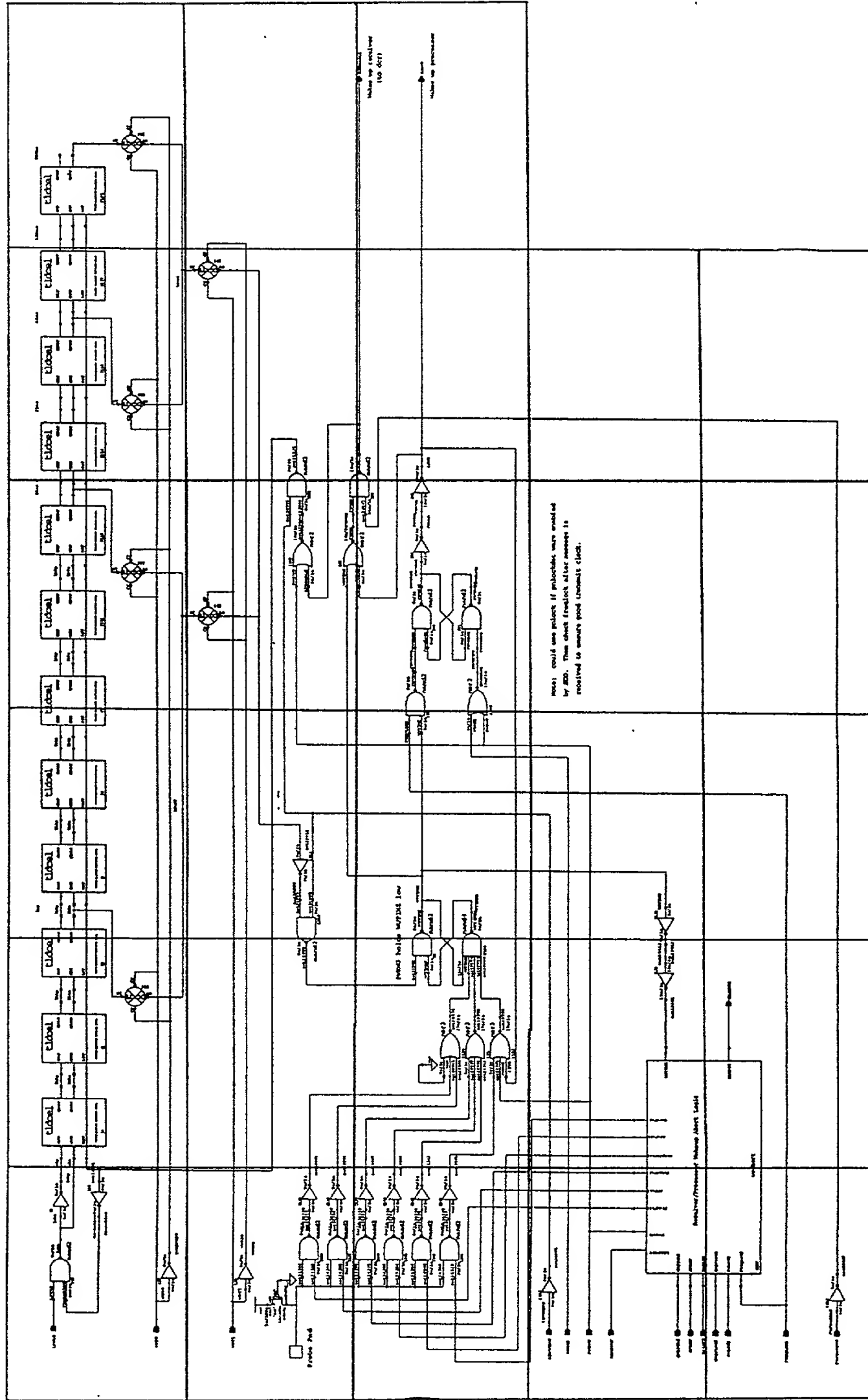
FIG. 8.03

2025 RELEASE UNDER E.O. 14176

8.04AA	8.04AB	8.04AC	8.04AD	8.04AE	8.04AF
8.04BA	8.04BB	8.04BC	8.04BD	8.04BE	8.04BF
8.04CA	8.04CB	8.04CC	8.04CD	8.04CE	8.04CF
8.04DA	8.04DB	8.04DC	8.04DD	8.04DE	
8.04EA	8.04EB	8.04EC	8.04ED	8.04EE	

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any other type of data in any of the other data fields of the data structure.



Notes: could use select if subblocks were enabled by RD0. Then check feedback after message is received to ensure good transmit clock.

FIG. 804

B1: redesign changed to power

B11: adjusted output time to compensate for data loss

added output

changed CTR input to storage input of hard processor

MICRON		DATE	10/10/80
INTEGRATED CIRCUIT DESIGN		DESIGNER	10/10/80
CONFIDENTIAL INFORMATION		DATE	10/10/80

RF Detect Timer

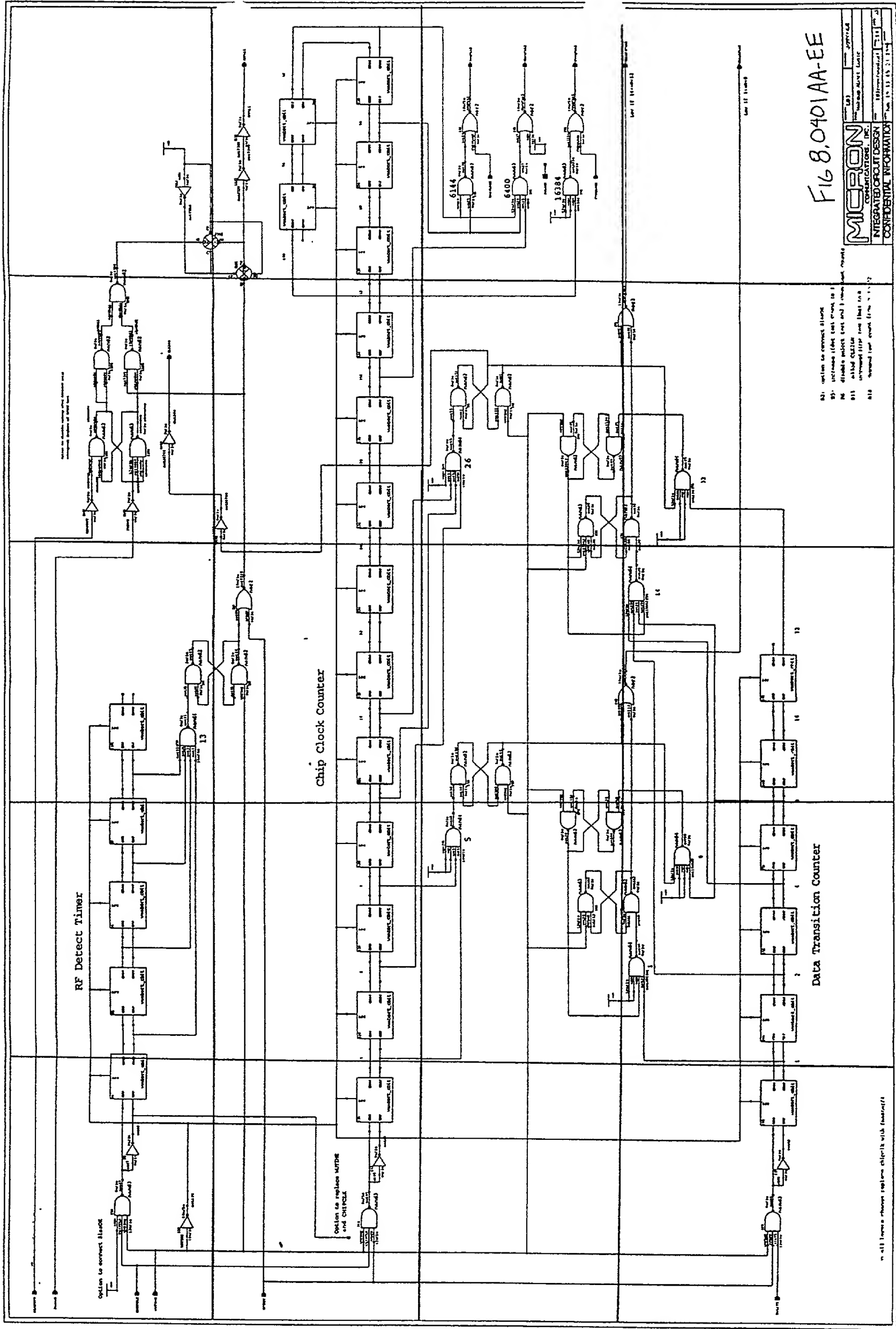
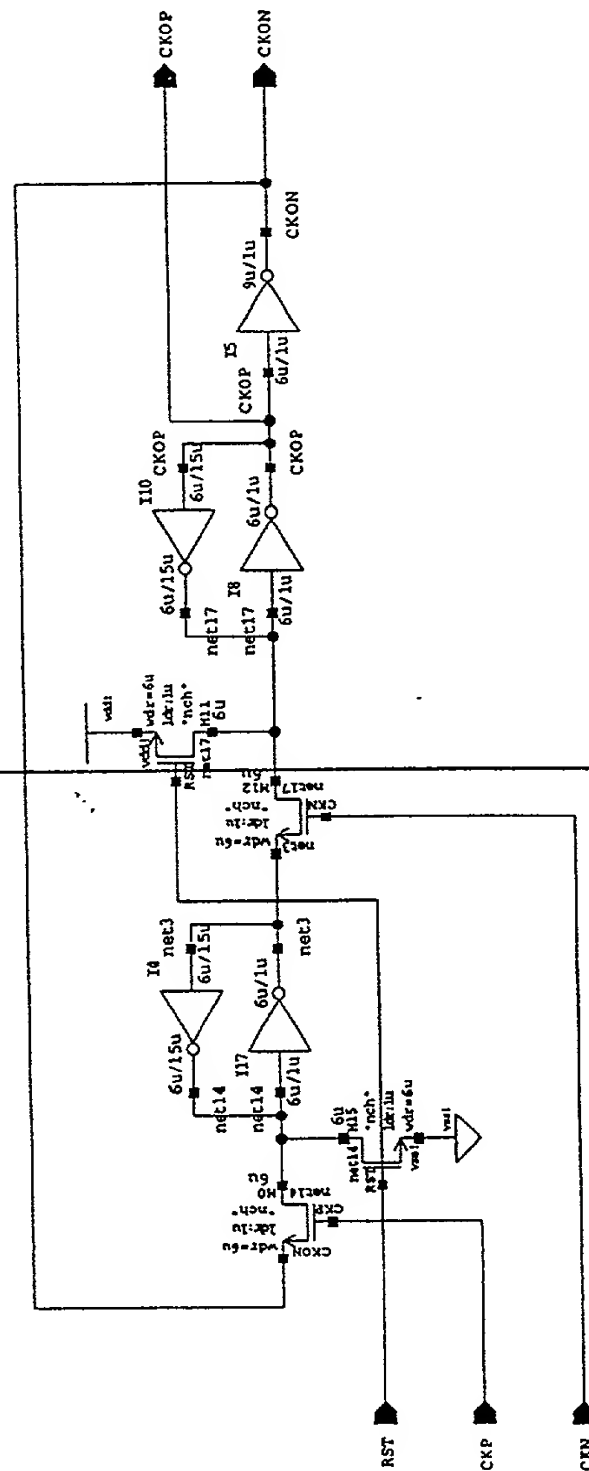


Fig 8.0401AA-EE

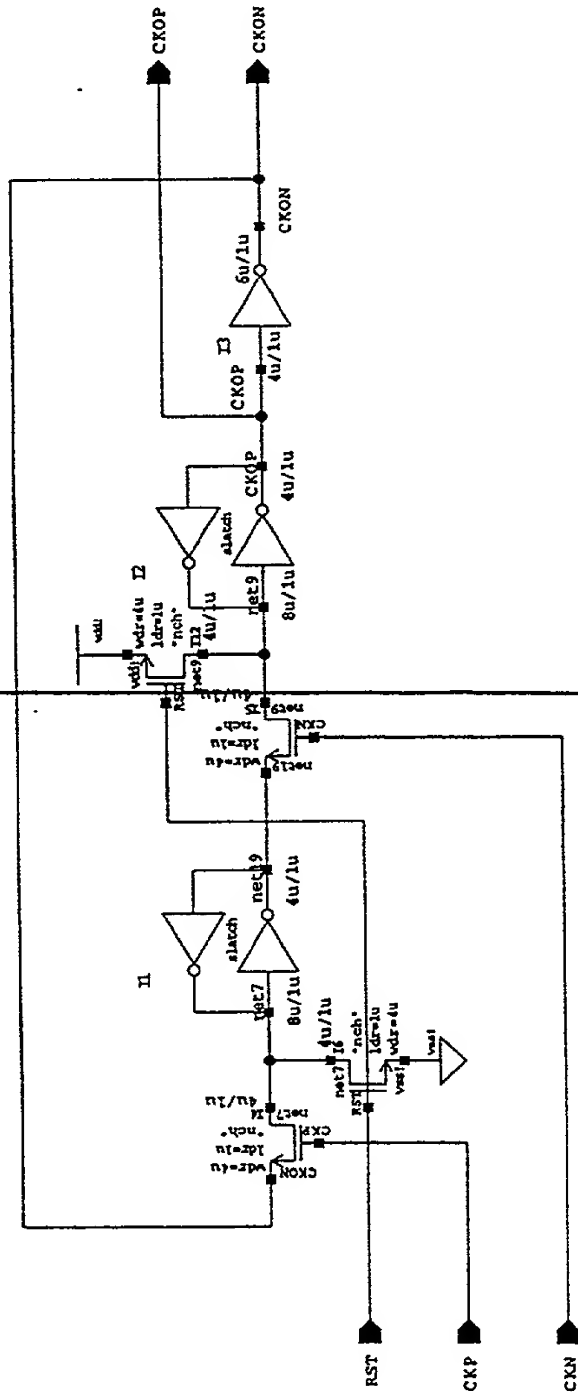
Option to correct block
 6400 - increase (det test error) to 1
 6144 - disable select test and 1 error
 6144 - add 00000000
 6144 - increase (det test error) to 1
 6144 - increase (det test error) to 1



MICRON COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
PROJECT: L03	DESIGNER: JOTOOLE		
TITLE: Wakeup Abort Logic Counter Bit			
NAME: I03reva/wuabort_cbit	REV: B1	SIZE: A	
DATE: Sep 26 08:40:51 1994		SHEET: 1	

Fig. 8.040101

12/29/92



12/29/92

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Timed Lockout Divider Cell			
NAME: 103reva/tldcel		REV: 1	SIZE: A
DATE: Sep 22 15:26:56 1994		SHEET: 1	

MICRON
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

FIG. 8.0402

8.05AA	8.05AB	8.05AC	8.05AD	8.05AE
8.05BA	8.05BB	8.05BC	8.05BD	8.05BE
8.05CA	8.05CB	8.05CC	8.05CD	8.05CE
8.05DA	8.05DB	8.05DC	8.05DD	8.05DE

50.8.8.05

[illegible]

8.0501AA	8.0501AB	8.0501AC	8.0501AD	8.0501AE
8.0501BA	8.0501BB	8.0501BC	8.0501BD	8.0501BE

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DOCUMENT.

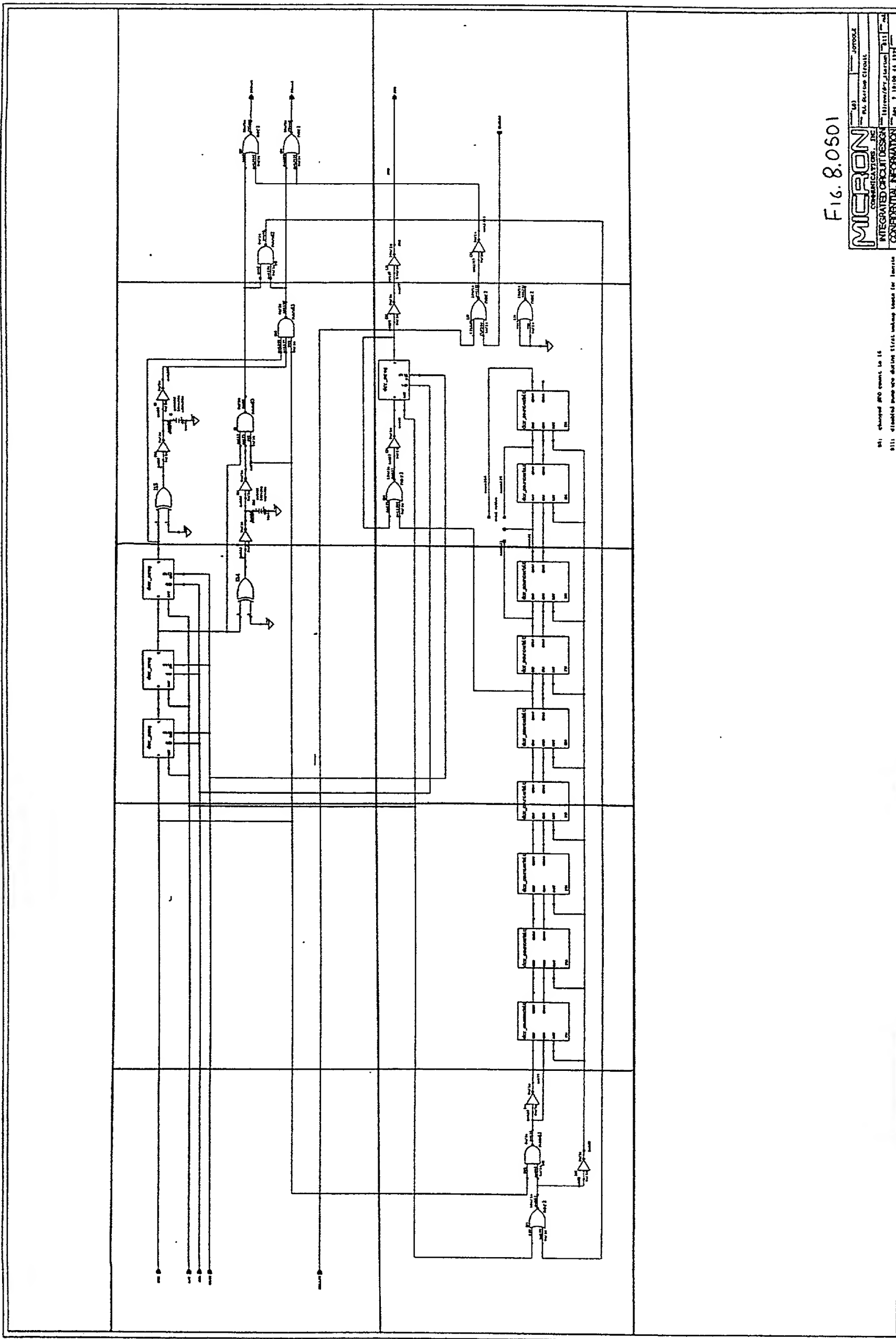


Fig. 8.0501

8.050101AB

8.050101AA

EX-115-111

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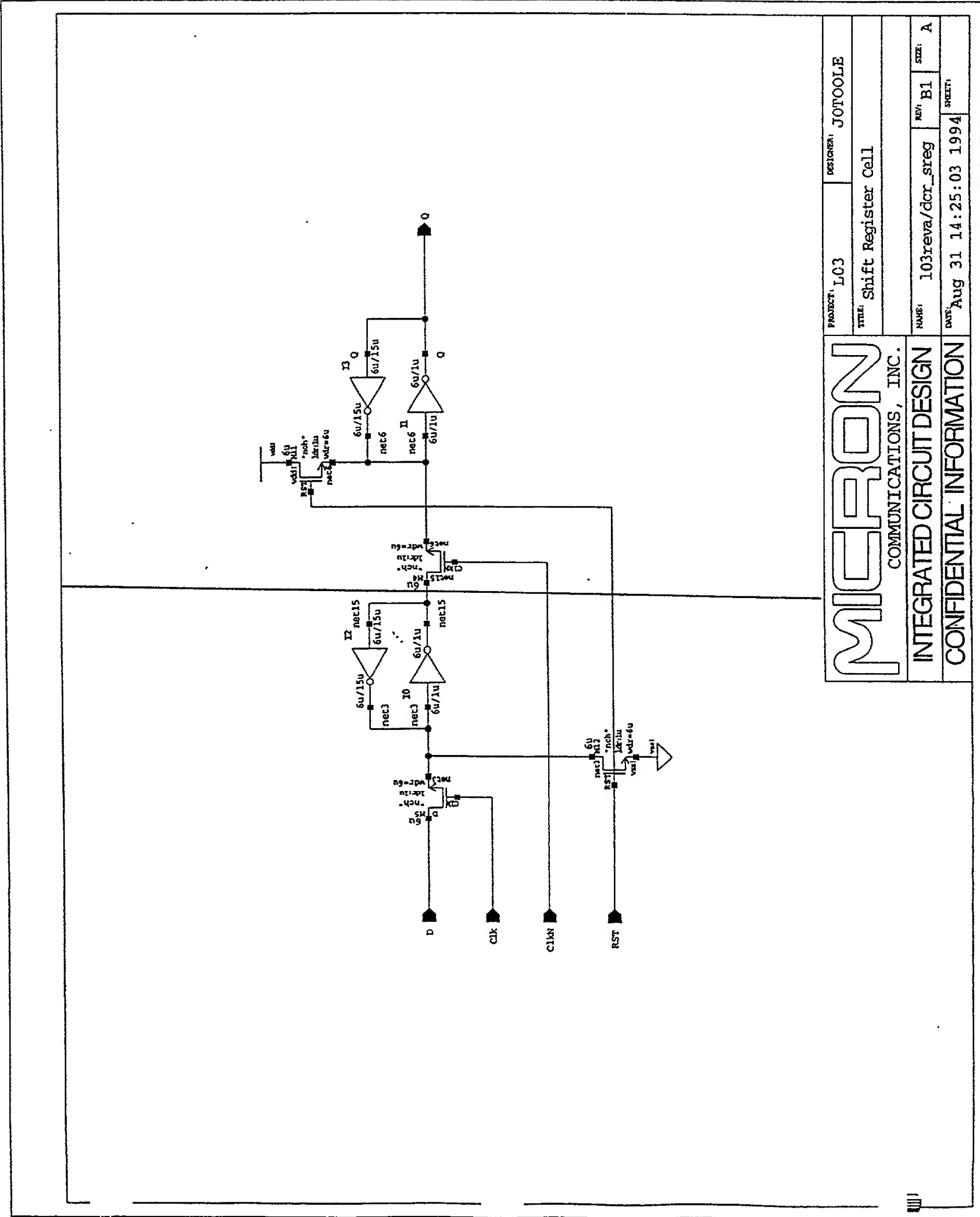


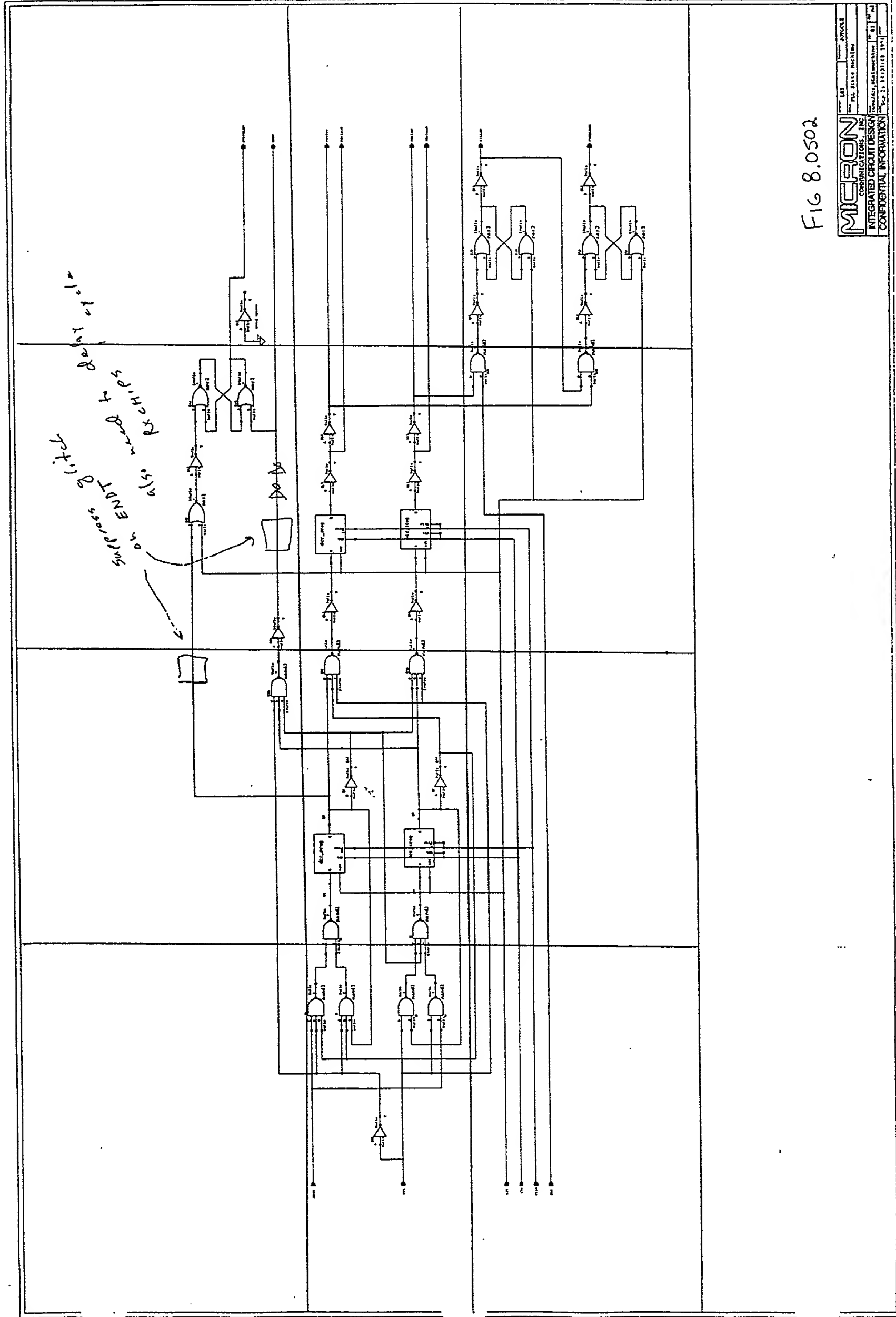
FIG. 8.050101

8.050102AB

8.050102AA

8.050102

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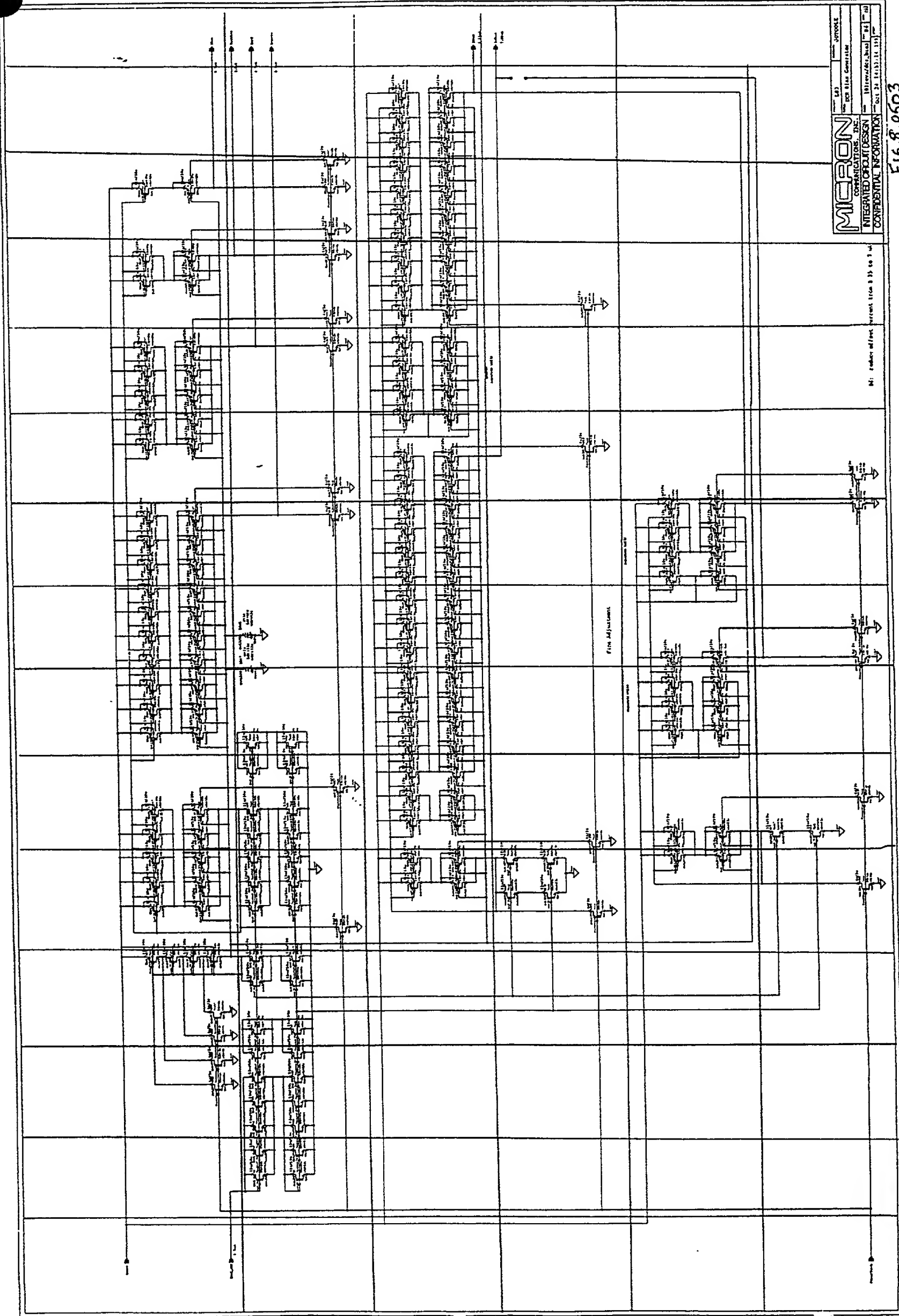
8.05034A 8.05034B 8.05034C 8.05034D 8.05034E 8.05034F 8.05034G 8.05034H 8.05034I 8.05034J 8.05034K 8.05034L 8.05034M 8.05034N 8.05034O

MI40-030

8.05034A	8.05034B	8.05034C	8.05034D	8.05034E	8.05034F	8.05034G	8.05034H	8.05034I	8.05034J	8.05034K	8.05034L	8.05034M	8.05034N	8.05034O
8.0503BA	8.0503BB	8.0503BC	8.0503BD	8.0503BE	8.0503BF	8.0503BG	8.0503BH	8.0503BI	8.0503BJ	8.0503BK	8.0503BL	8.0503BM	8.0503BN	8.0503BO
8.0503CA	8.0503CB	8.0503CC	8.0503CD	8.0503CE	8.0503CF	8.0503CG	8.0503CH	8.0503CI	8.0503CJ	8.0503CK	8.0503CL	8.0503CM	8.0503CN	8.0503CO
8.0503DA	8.0503DB	8.0503DC	8.0503DD	8.0503DE	8.0503DF	8.0503DG	8.0503DH	8.0503DI	8.0503DJ	8.0503DK	8.0503DL	8.0503DM	8.0503DN	8.0503DO
8.0503EA	8.0503EB	8.0503EC	8.0503ED	8.0503EE	8.0503EF	8.0503EG	8.0503EH	8.0503EI	8.0503EJ	8.0503EK	8.0503EL	8.0503EM	8.0503EN	
8.0503FA	8.0503FB	8.0503FC	8.0503FD	8.0503FE	8.0503FF	8.0503FG	8.0503FH	8.0503FI	8.0503FJ	8.0503FK	8.0503FL	8.0503FM	8.0503FN	

8.0503GA 8.0503GB 8.0503GC 8.0503GD 8.0503GE 8.0503GF 8.0503GG 8.0503GH 8.0503GI 8.0503GJ 8.0503GK 8.0503GL 8.0503GM 8.0503GN 8.0503GO

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MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
Rev. 1.0
Dec 11/83
11/83

Rev. 1.0
Dec 11/83
11/83

F16.8.0503

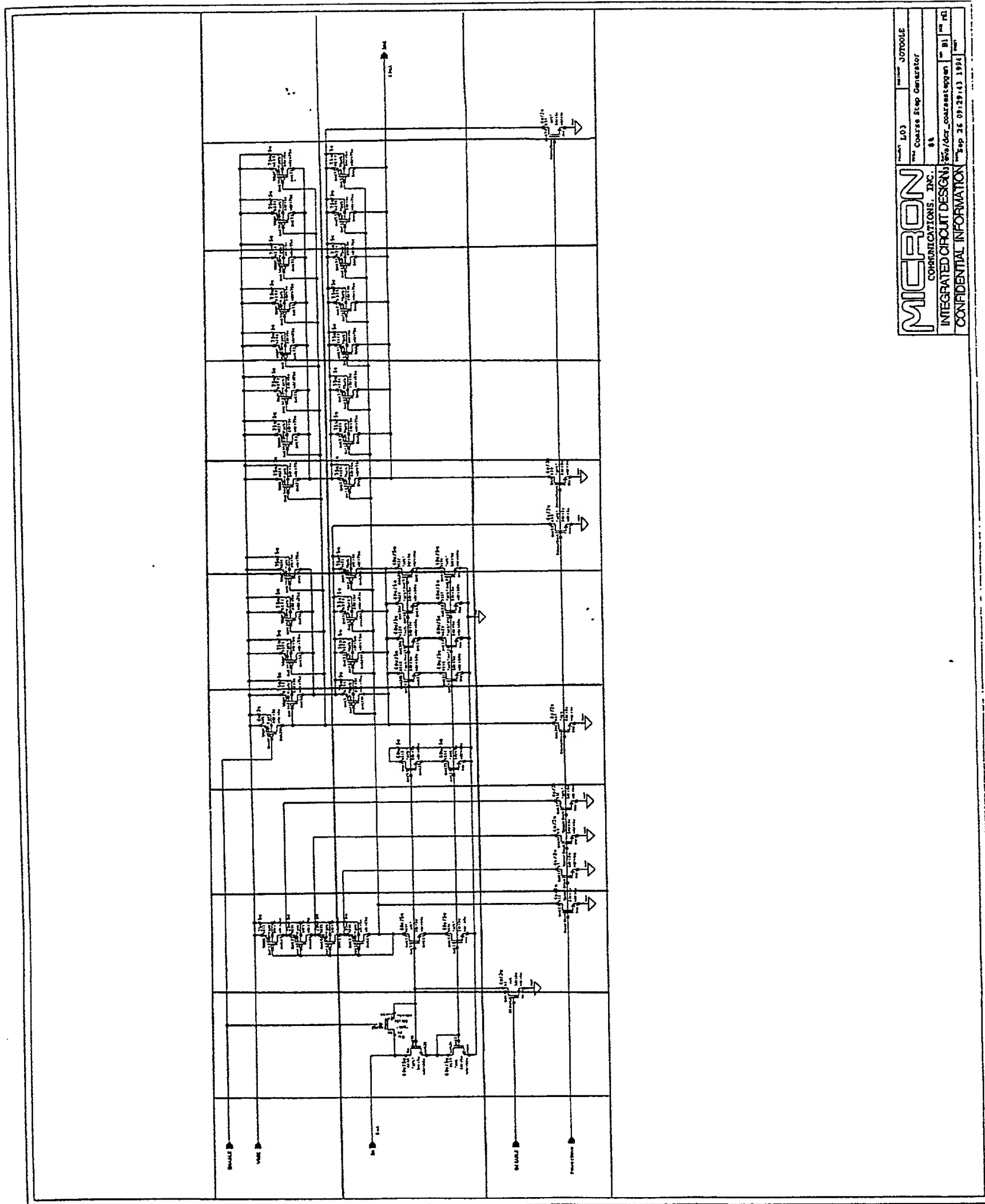
[illegible]

8.050401AA 8.050401AB 8.050401AC 8.050401AD 8.050401AE 8.050401AF 8.050401AG 8.050401AH 8.050401AJ 8.050401AK

8.050401AA	8.050401AB	8.050401AC	8.050401AD	8.050401AE	8.050401AF	8.050401AG	8.050401AH	8.050401AJ	
8.050401BA	8.050401BB	8.050401BC	8.050401BD	8.050401BE	8.050401BF	8.050401BG	8.050401BH	8.050401BJ	8.050401BK
8.050401CA	8.050401CB	8.050401CC	8.050401CD	8.050401CE	8.050401CF	8.050401CG	8.050401CH	8.050401CJ	8.050401CK

8.050401DL 8.050401DM 8.050401DN 8.050401DO 8.050401DP 8.050401DQ 8.050401DR 8.050401DS 8.050401DT 8.050401DU 8.050401DV 8.050401DW 8.050401DX 8.050401DY 8.050401DZ

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MICRON		LO3	JUTTOLE
COMMUNICATIONS, INC.		Coarse Step Generator	
INTEGRATED CIRCUIT DESIGN		\$1	
CONFIDENTIAL INFORMATION		Rev 26 09:29:43 1994	Rev 26

Fig 8.050401

2005.08.11

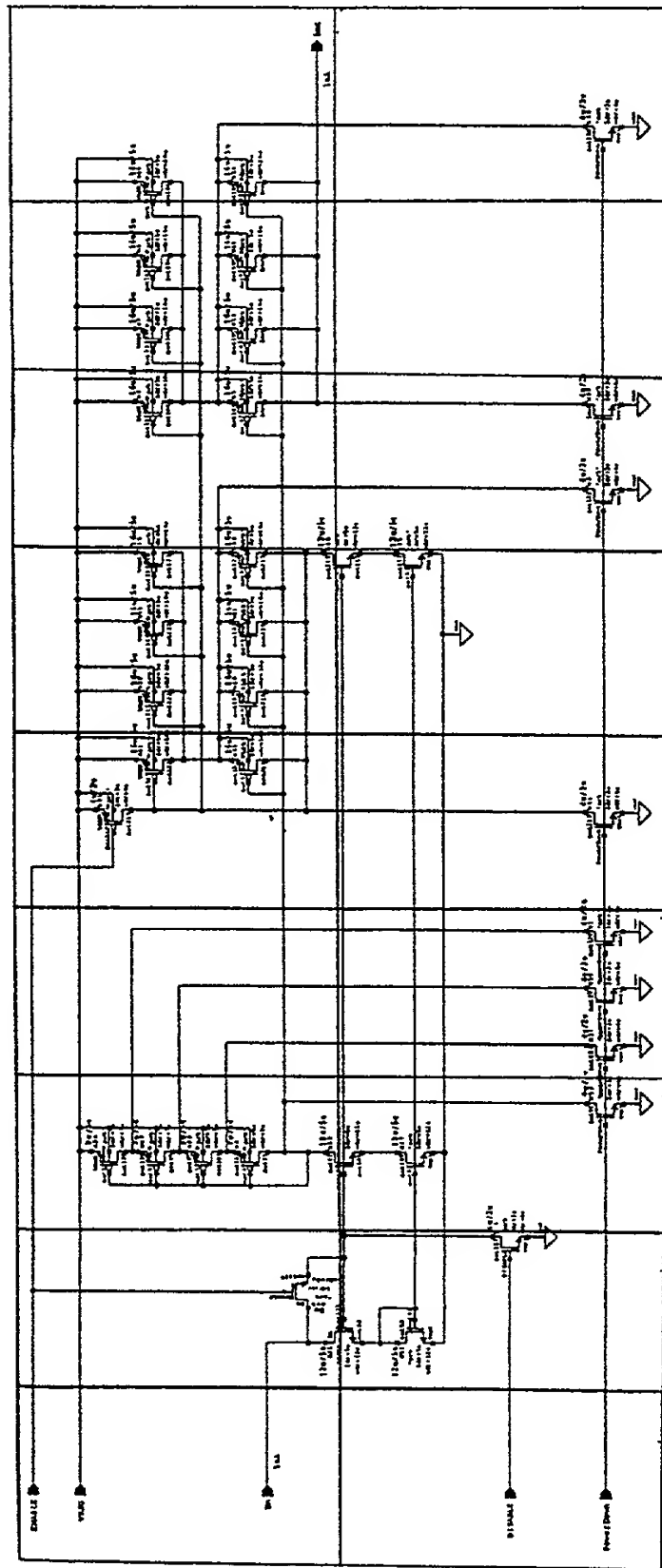
Fig. 8.050402



8.050403AA	8.050403AB	8.050403AC	8.050403AD	8.050403AE	8.050403AF	8.050403AG	8.050403AH	8.050403AI
8.050403BA	8.050403BB	8.050403BC	8.050403BD	8.050403BE	8.050403BF	8.050403BG	8.050403BH	8.050403BI

Итого: 8.050403

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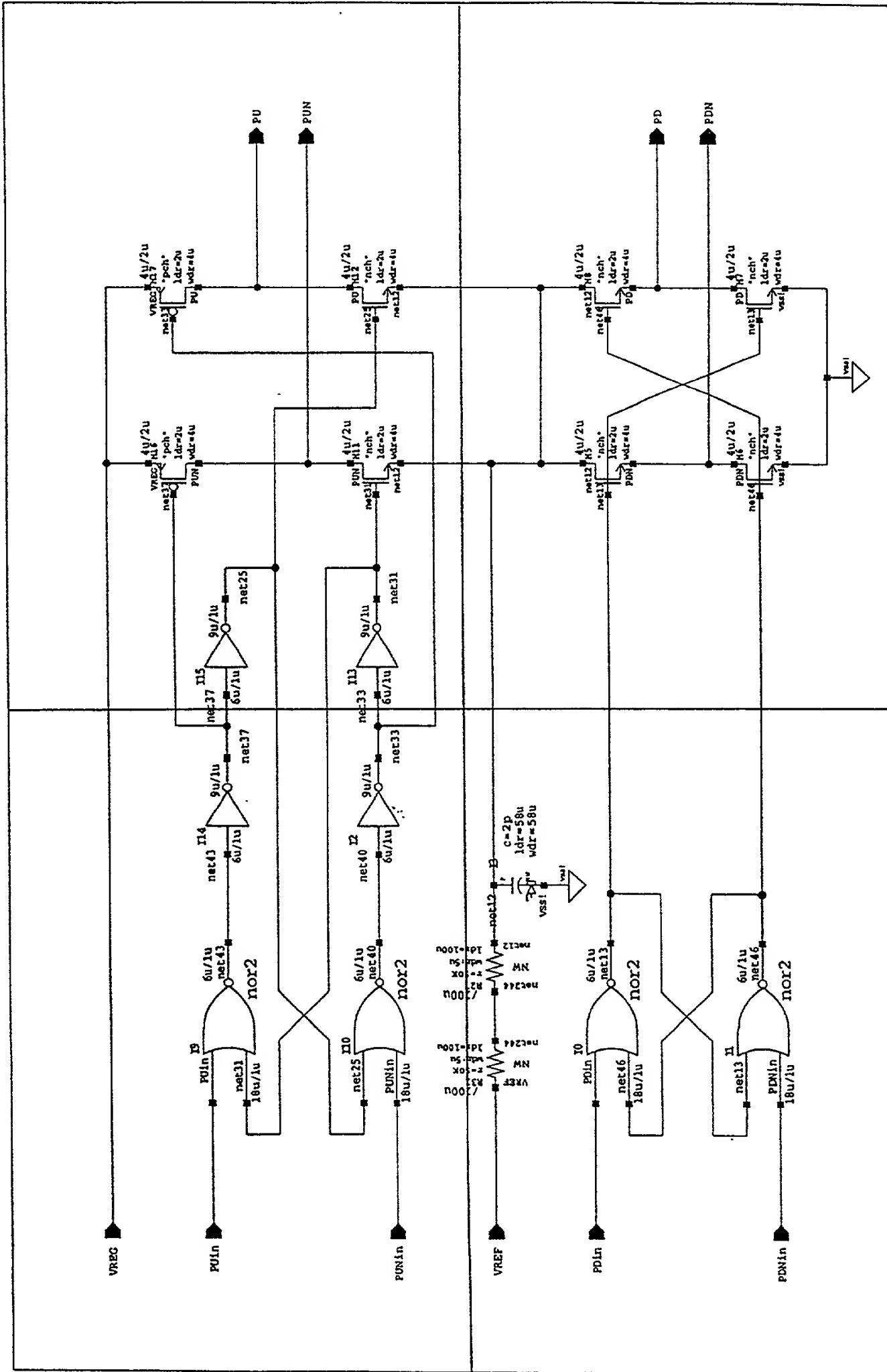
MICRON		Lot 101	Medium Fine Step Generator
COMMUNICATIONS, INC.		0.21	
INTEGRATED CIRCUIT DESIGN		02/dec modification	01
CONFIDENTIAL INFORMATION		Exp 26 09/31/88 1994	01

Fig. 8.050403

8.050404AA	8.050404AB
8.050404BA	8.050404BB

IL 11 03 BB.0504040044

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MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: DCR Fine Step Controller	
INTEGRATED CIRCUIT DESIGN		NAME: j03revb/dcr_finestepctrl	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:32:11 1994	SHEET: A

FIG. 8.050409

8.050405AA 8.050405AB 8.050405AC 8.050405AD 8.050405AE 8.050405AF 8.050405AG 8.050405AH 8.050405AI 8.050405AJ 8.050405AK 8.050405AL 8.050405AM

MI40-030

8.050405BA	8.050405BB	8.050405BC	8.050405BD	8.050405BE	8.050405BF	8.050405BG	8.050405BH	8.050405BI	8.050405BJ	8.050405BK	8.050405BL	8.050405BM
8.050405CA	8.050405CB	8.050405CC	8.050405CD	8.050405CE	8.050405CF	8.050405CG	8.050405CH	8.050405CI	8.050405CJ	8.050405CK	8.050405CL	8.050405CM
8.050405DA	8.050405DB	8.050405DC	8.050405DD	8.050405DE	8.050405DF	8.050405DG	8.050405DH	8.050405DI	8.050405DJ			
8.050405EA	8.050405EB	8.050405EC	8.050405ED	8.050405EE	8.050405EF	8.050405EG	8.050405EH	8.050405EI	8.050405EJ			

И.И.С. 88.05040505

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

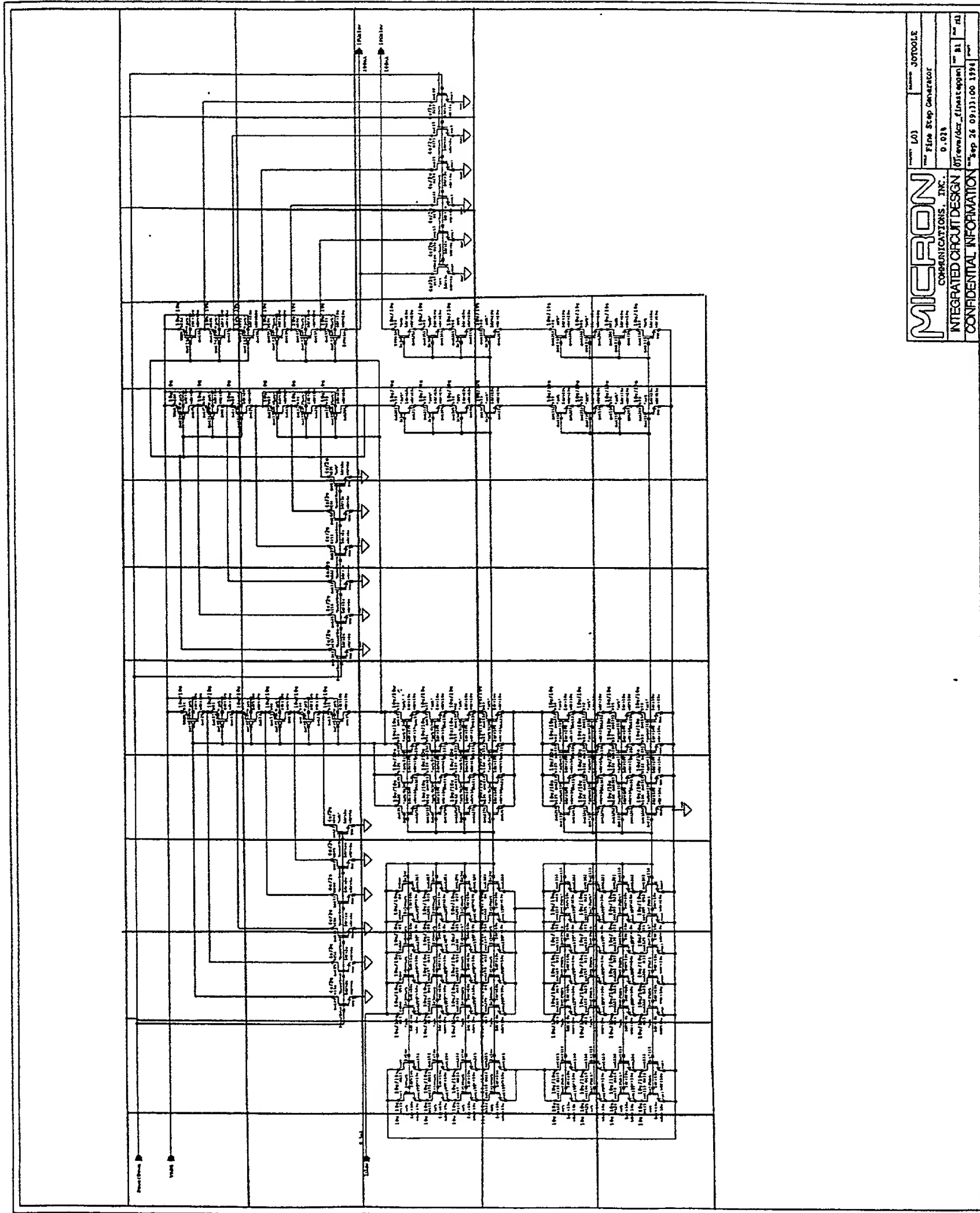


Fig 8.050405

BB. 00505 II II II

8.0506AA	8.0506AB
8.0506BA	8.0506BB

EX 88.0506

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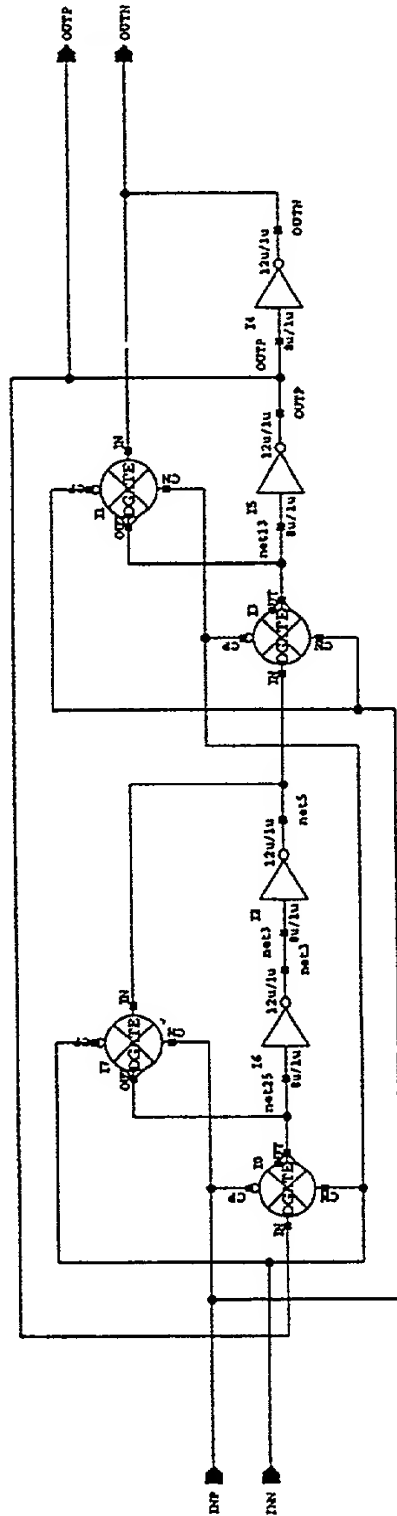


FIG. 8.050601

MICRON		PROJECT: L03	REVISION: J0000LE
COMMUNICATIONS, INC.		TITLE: Rx Clock Generator	
INTEGRATED CIRCUIT DESIGN		Flip-Flop	
CONFIDENTIAL INFORMATION		T03reva/dcr rxclkgeniff	REV: B1
		DATE: Sep 26 09:36:05 1994	FILE: nil

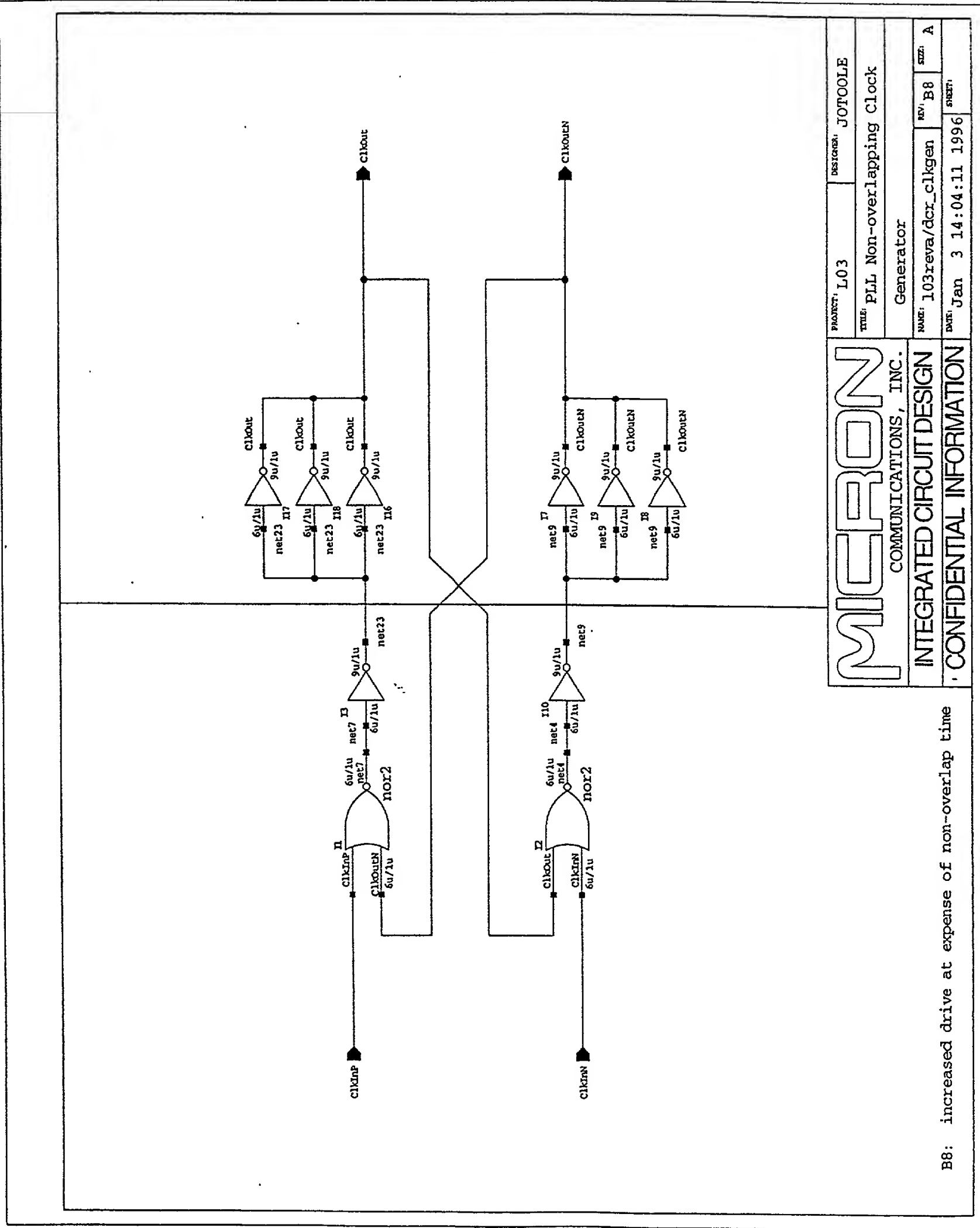
[illegible]

8.0507AB

8.0507AA

8.0507

FIG. 8.0507



B8: increased drive at expense of non-overlap time

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: PLL Non-overlapping Clock	
Generator	
NAME: 103reva/dcr_clkgen	REV: B8
DATE: Jan 3 14:04:11 1996	SIZE: A

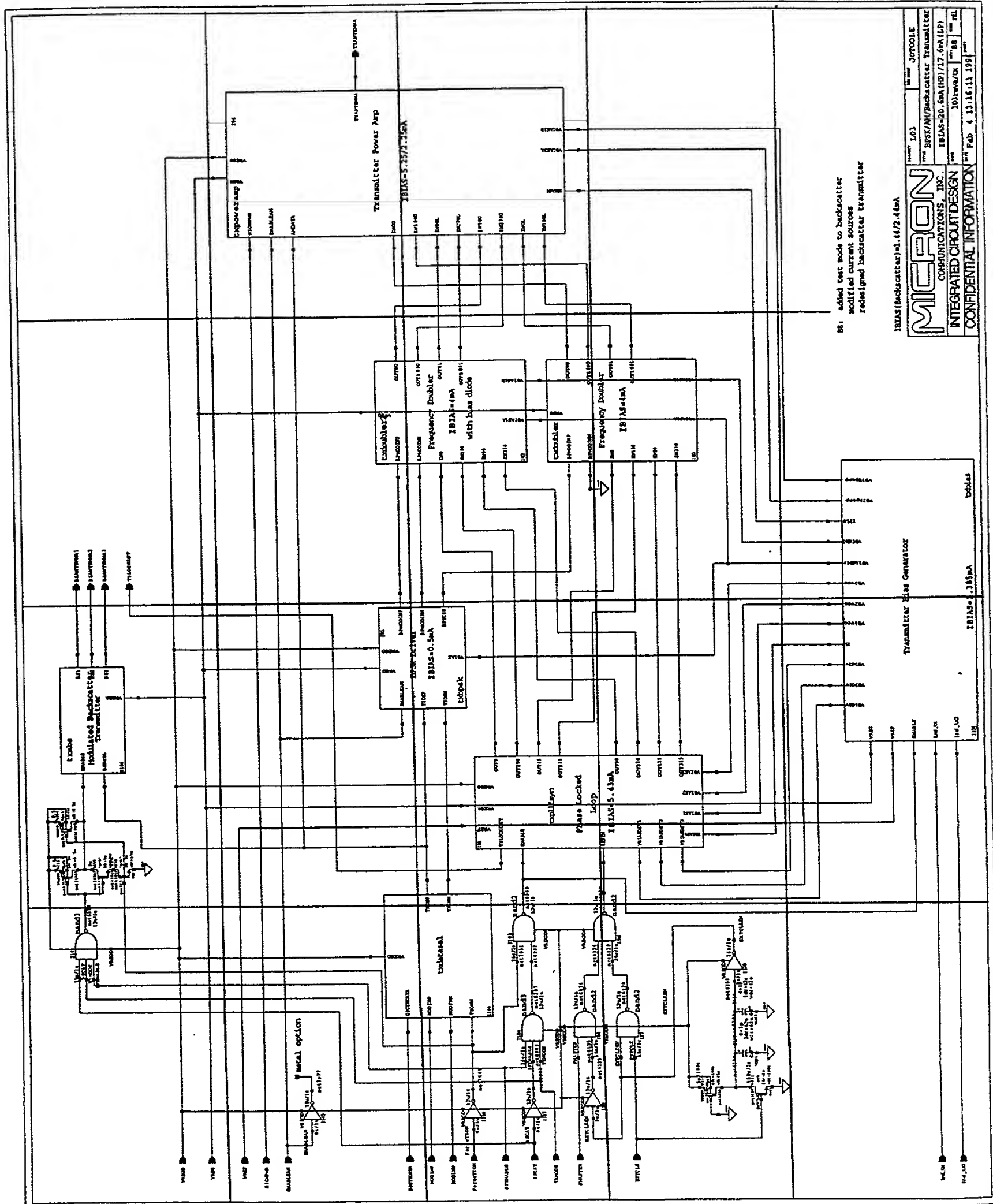
FIG. 8.0507

THE STATE OF MICHIGAN
DEPARTMENT OF TREASURY
DIVISION OF REVENUE

8.06AA	8.06AB	8.06AC	8.06AD
8.06BA	8.06BB	8.06BC	8.06BD
8.06CA	8.06CB	8.06CC	8.06CD
8.06DA	8.06DB	8.06DC	8.06DD
8.06EA	8.06EB	8.06EC	8.06ED

JE II 07 BB 0016

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88: added test mode to backscatter
 modified current sources
 redesigned backscatter transmitter

IBIAS(backscatter)=1.6/2.4mA

MICROPRON		PART 101	NAME J07000LE
COMMUNICATIONS, INC.		TYPE BPSK/AM/Backscatter Transmitter	
INTEGRATED CIRCUIT DESIGN		IBIAS=20.6mA (HP)/17.6mA (LP)	REV 88
CONFIDENTIAL INFORMATION		101rev/75	REV 88
		DATE Feb 4 13:16:11 1991	

FIG. 8.06

MI40-030

MI40-030

8.0601AA	8.0601AB
8.0601BA	8.0601BB

MI40-030

FIG. 8.0601
B6: make blockdet driver smaller

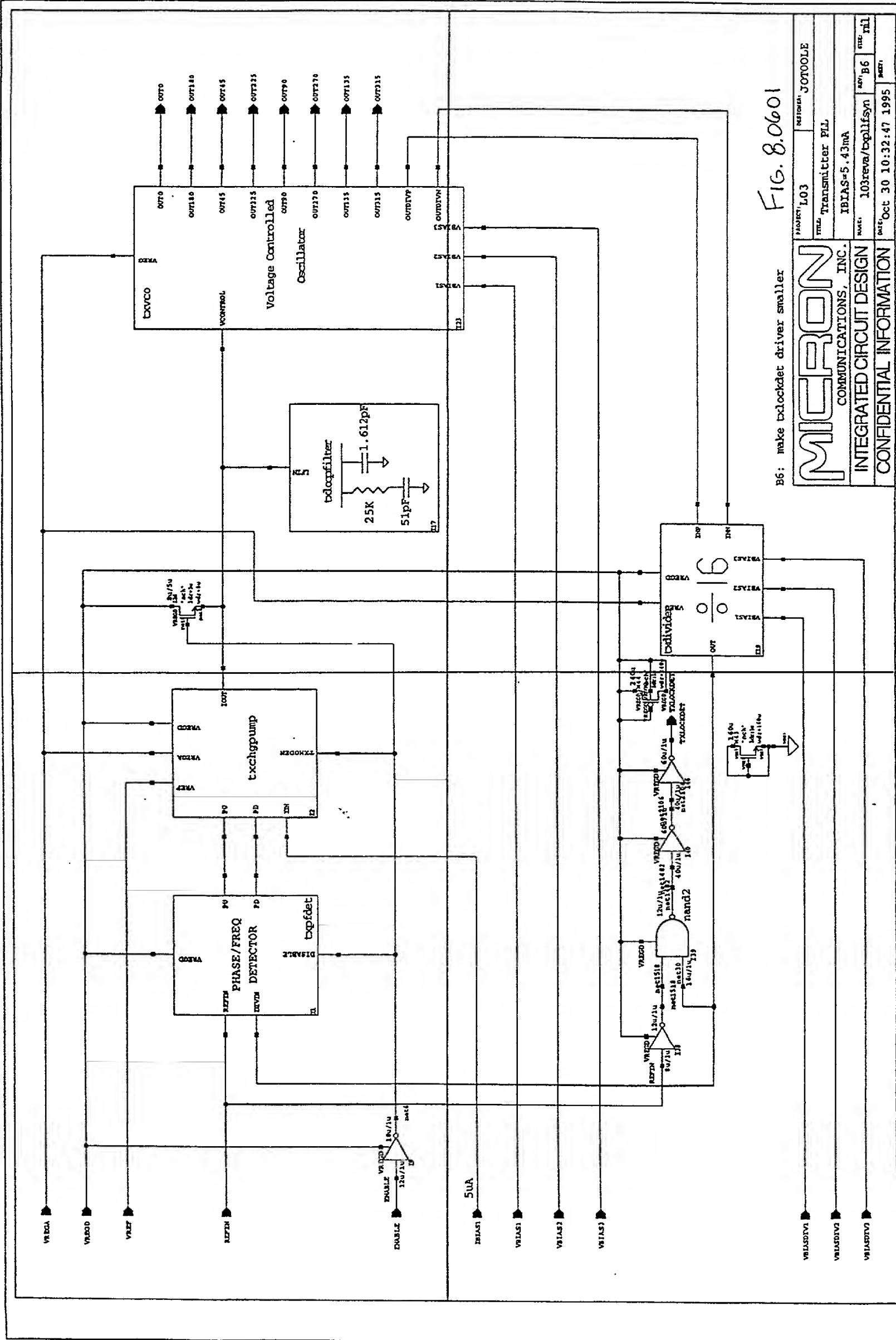


FIG. 8.0601

B6: make blockdet driver smaller

MICRON		PROJECT: L03	REVISION: J0000LE
COMMUNICATIONS, INC.		TYPE: Transmitter PLL	
INTEGRATED CIRCUIT DESIGN		IBIAS=5.43mA	
CONFIDENTIAL INFORMATION		DATE: Oct 30 10:32:47 1995	REV: B6

8.060101AA	8.060101AB	8.060101AC
8.060101BA	8.060101BB	8.060101BC
8.060101CA	8.060101CB	8.060101CC

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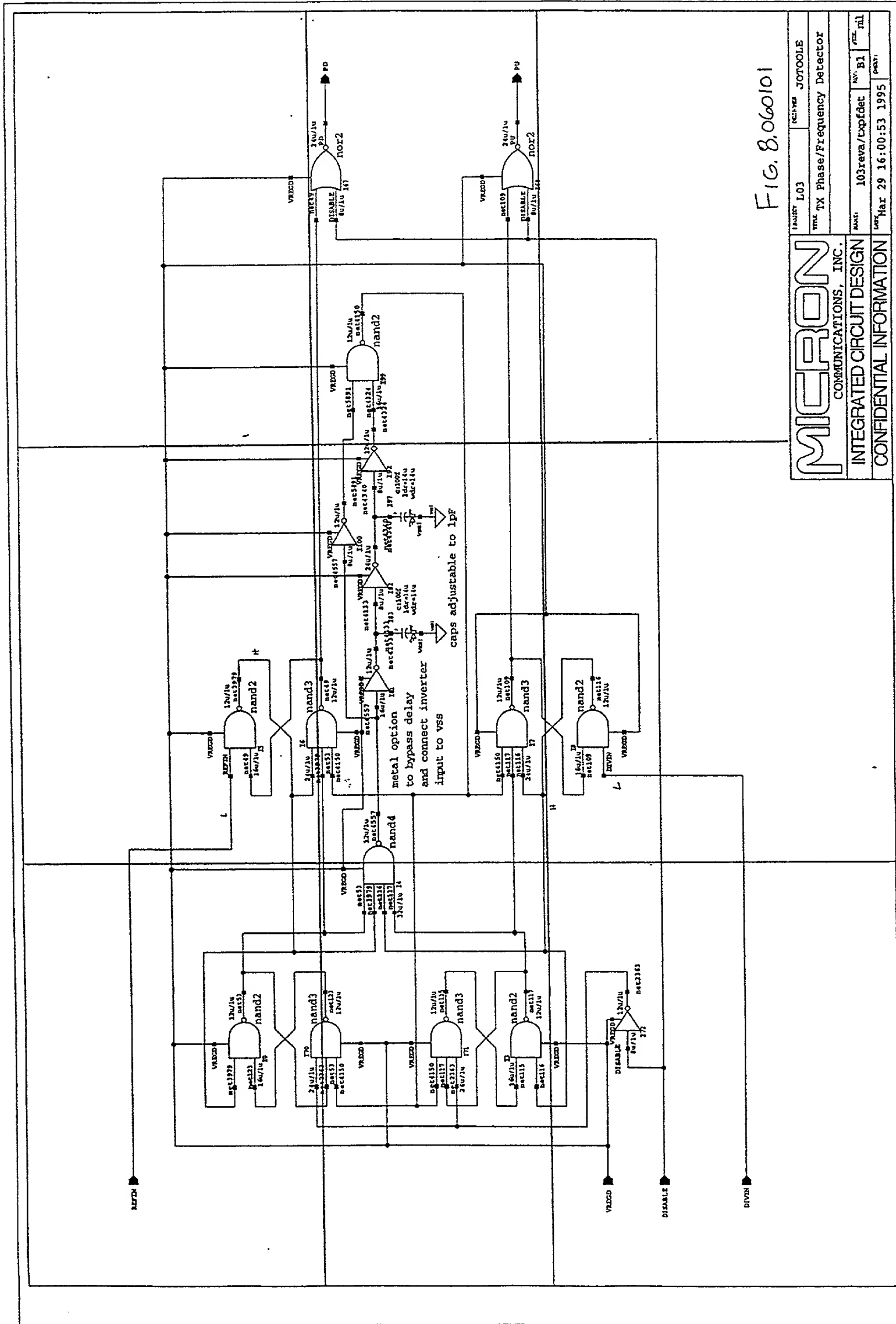


FIG. 8.060101

MICRON		TAUDET L03	REV. 100	JOTOOLE
COMMUNICATIONS, INC.		TX Phase/Frequency Detector		
INTEGRATED CIRCUIT DESIGN		NAME	103revA/txpfdet	REV. B1
CONFIDENTIAL INFORMATION		DATE	Mar 29 16:00:53 1995	FILE

8.060102AA	8.060102AB
8.060102BA	8.060102BB

Station	Time	Lat	Long	Alt	Wind	Temp	Humid	Cloud	Vis	Bar	Notes
1	0100	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
2	0200	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
3	0300	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
4	0400	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
5	0500	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
6	0600	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
7	0700	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
8	0800	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
9	0900	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
10	1000	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
11	1100	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
12	1200	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
13	1300	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
14	1400	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
15	1500	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
16	1600	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
17	1700	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
18	1800	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
19	1900	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
20	2000	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
21	2100	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
22	2200	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
23	2300	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear
24	0000	34° 15' N	118° 15' W	10	010	55.0	85	010	10	30.0	Clear

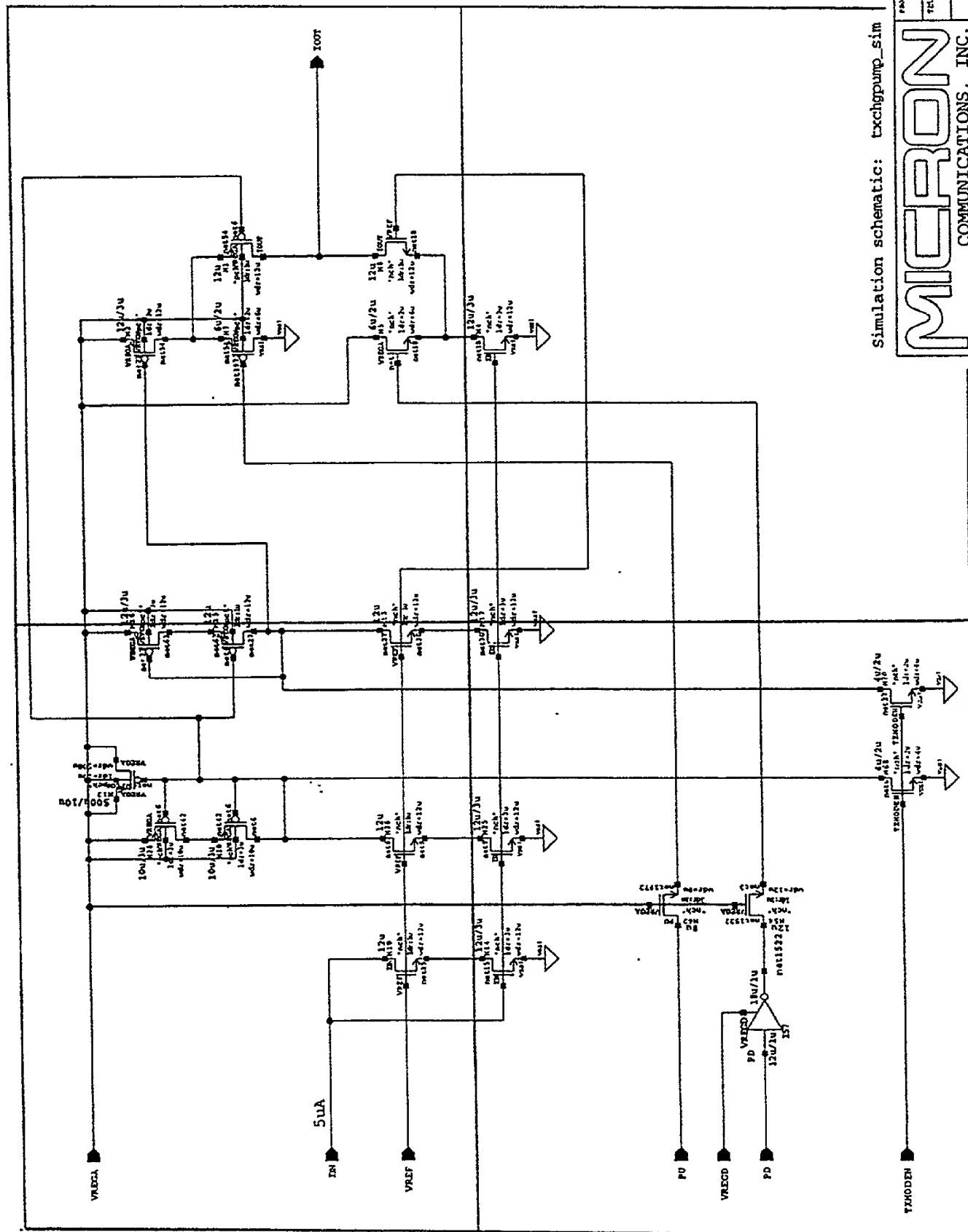


FIG. 8.060102

Simulation schematic: txchgump_sim

21C PROZ
COMMUNICATIONS, INC.

DESIGNER	JOTOOLE
PROJECT	L03

TX PLL Charge Pump

103reva/exchg pump	rev: B1	sta: mil
--------------------	---------	----------

DATE	TIME
FEB 28 09:55:50 1995	

8.060103AA	8.060103AB
8.060103BA	8.060103BB
8.060103CA	8.060103CB

BB.000000.0000

[illegible]

MICROPRON COMMUNICATIONS, INC.		PROJECT: L03		Indicates: JOTOOLUE	
INTEGRATED CIRCUIT DESIGN		TITLE: TX PLL Loop Filter			
		BW=700KHZ		PM=60deg	
NAME: 103reva/bdloopfilter		REV: B8		SIZE: mil	
CONFIDENTIAL INFORMATION		DATE: Feb 5 14:40:11 1996		SHEET:	

B2: moved extra caps to blasok

B8: moved 2 2K resistors to tmbms

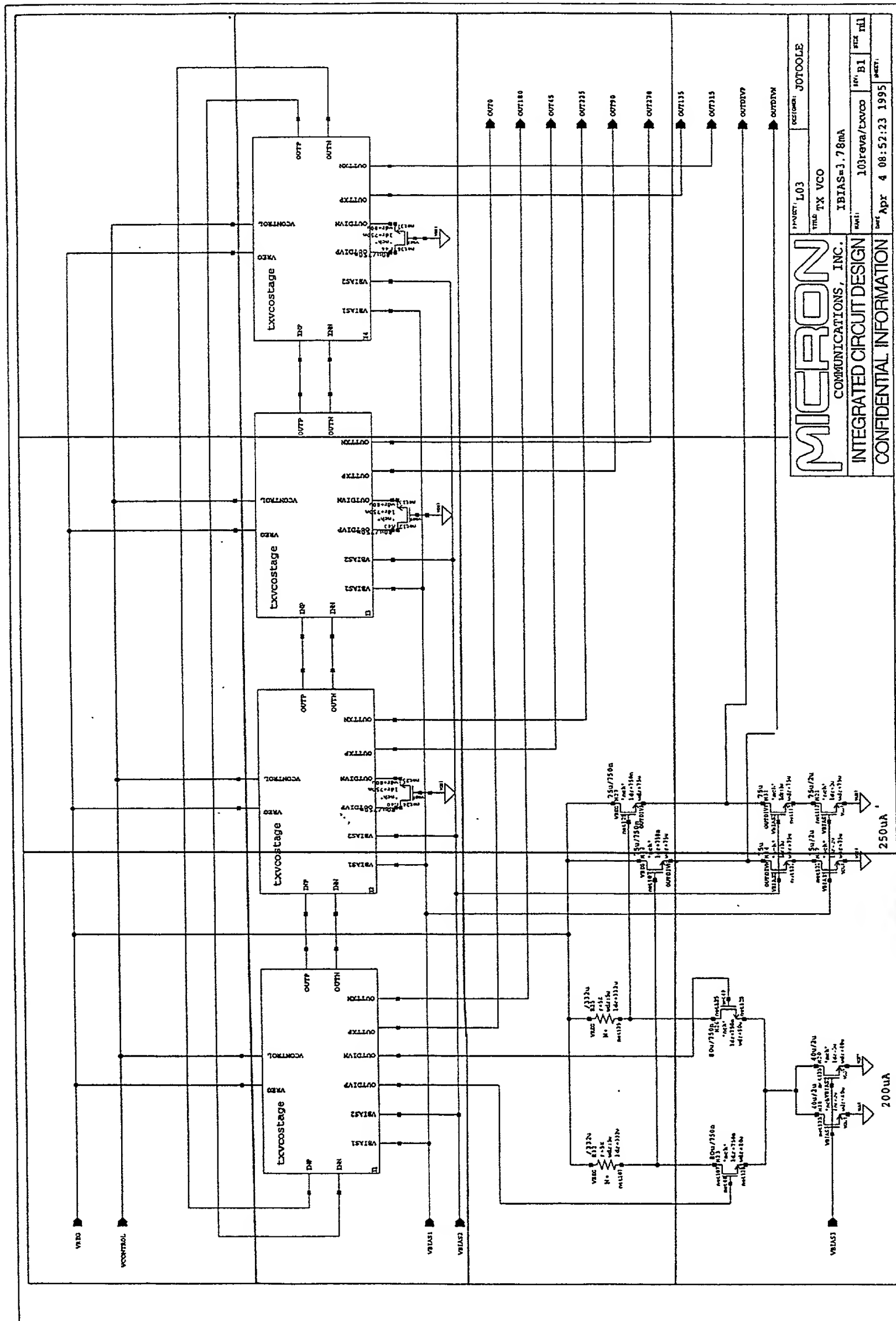
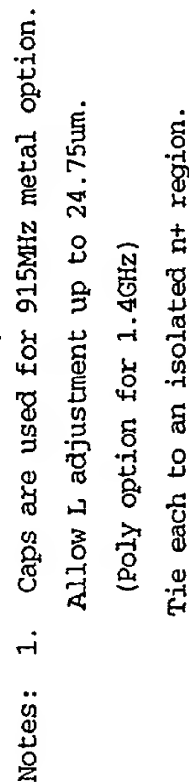
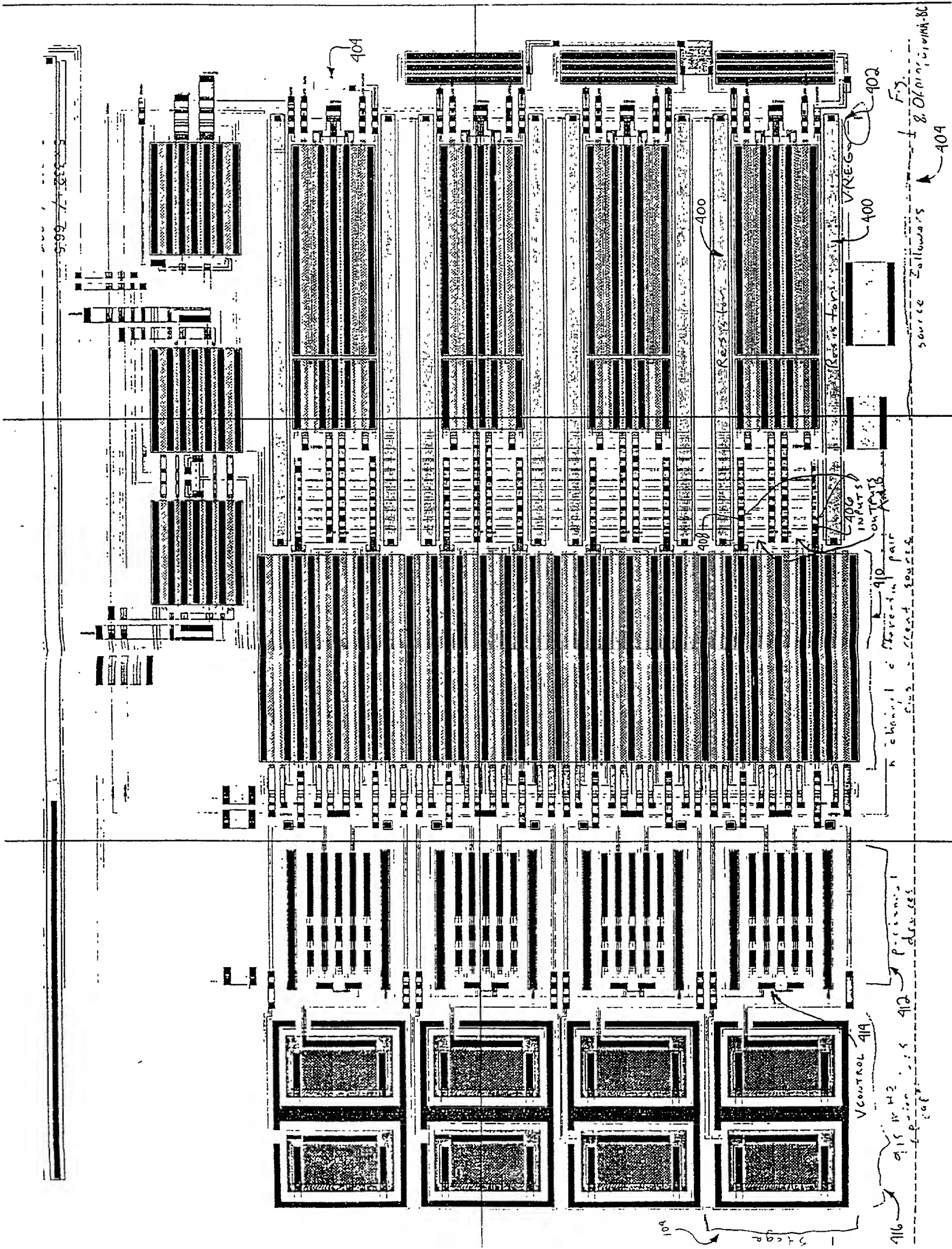


Fig. 8.060104



Notes: 1. Caps are used for 915MHz metal option.
 Allow L adjustment up to 24.75um.
 (Poly option for 1.4GHz)
 Tie each to an isolated n+ region.



8.060105AA	8.060105AB	8.060105AC	8.060105AD
8.060105BA	8.060105BB	8.060105BC	8.060105BD
8.060105CA	8.060105CB	8.060105CC	8.060105CD
8.060105DA	8.060105DB	8.060105DC	8.060105DD

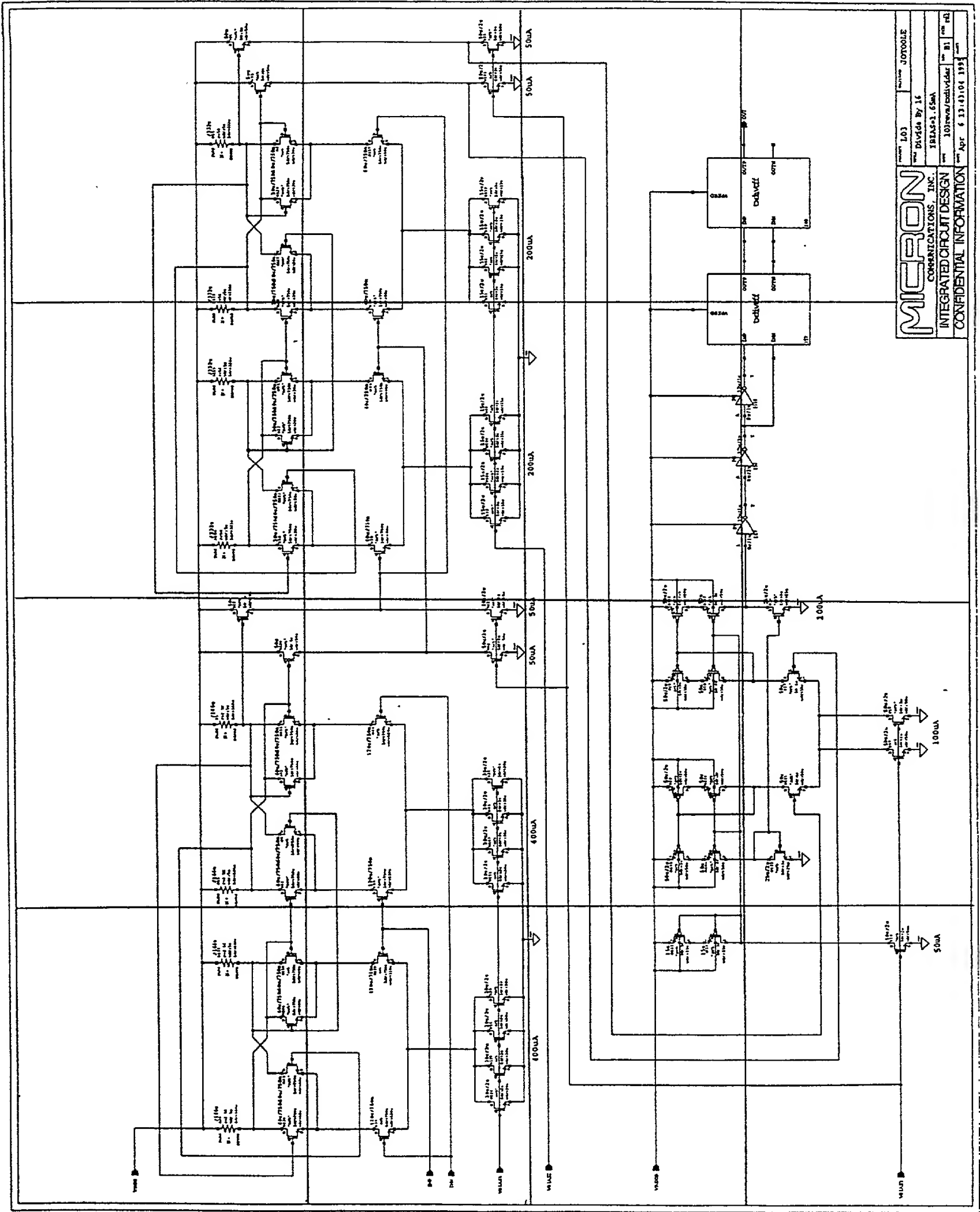
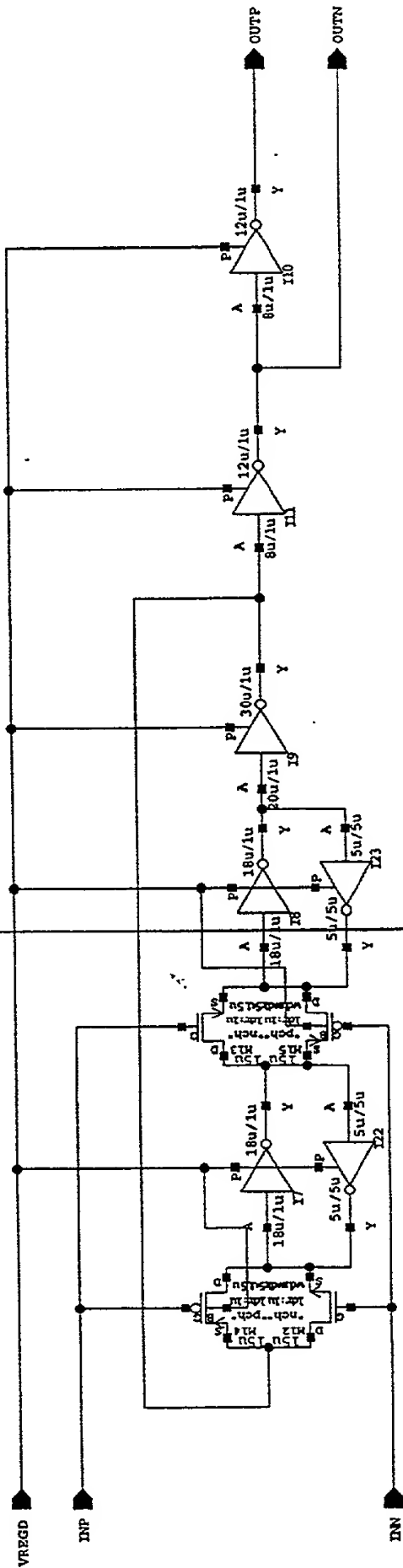


FIG. 8.060105

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PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Divider Flip-flop			
NAME: 103reva/bxdlvtff	REV: B1	SIZE: A	
DATE: Mar 30 09:47:12 1995	SHEET: 1		

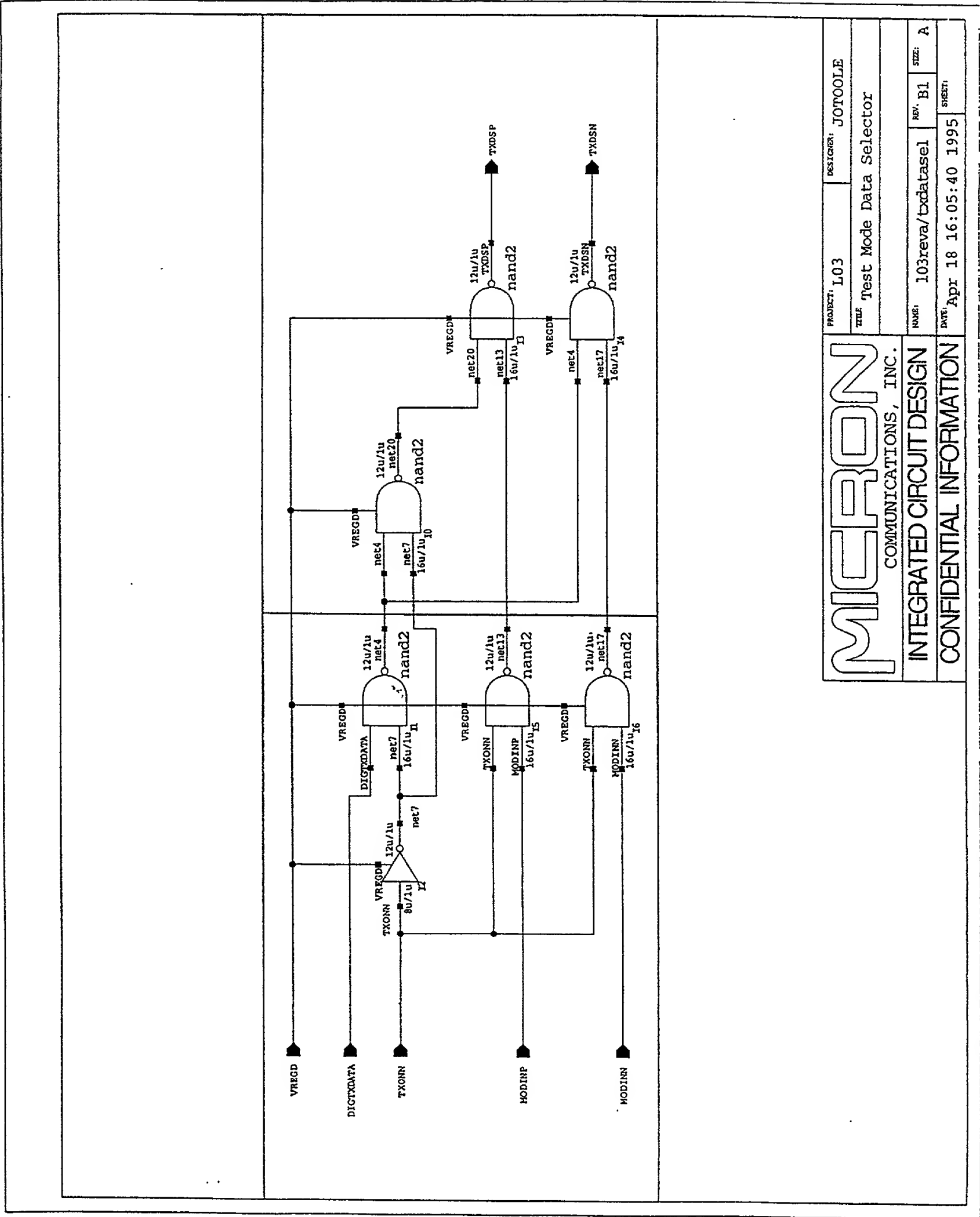
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 8.06010501

8.0602AA	8.0602AB
----------	----------

EX 88.0602

THIS DOCUMENT IS UNCLASSIFIED
DATE 08-08-2001 BY 60322 UCBAW/BJS
REASON: EXECUTIVE ORDER 11652



MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Test Mode Data Selector	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/txdatasel	REV: B1
CONFIDENTIAL INFORMATION		DATE: Apr 18 16:05:40 1995	SIZE: A
			SHEET: 1

FIG. 8.0602

8.0603AB

8.0603AA

8.0603AB

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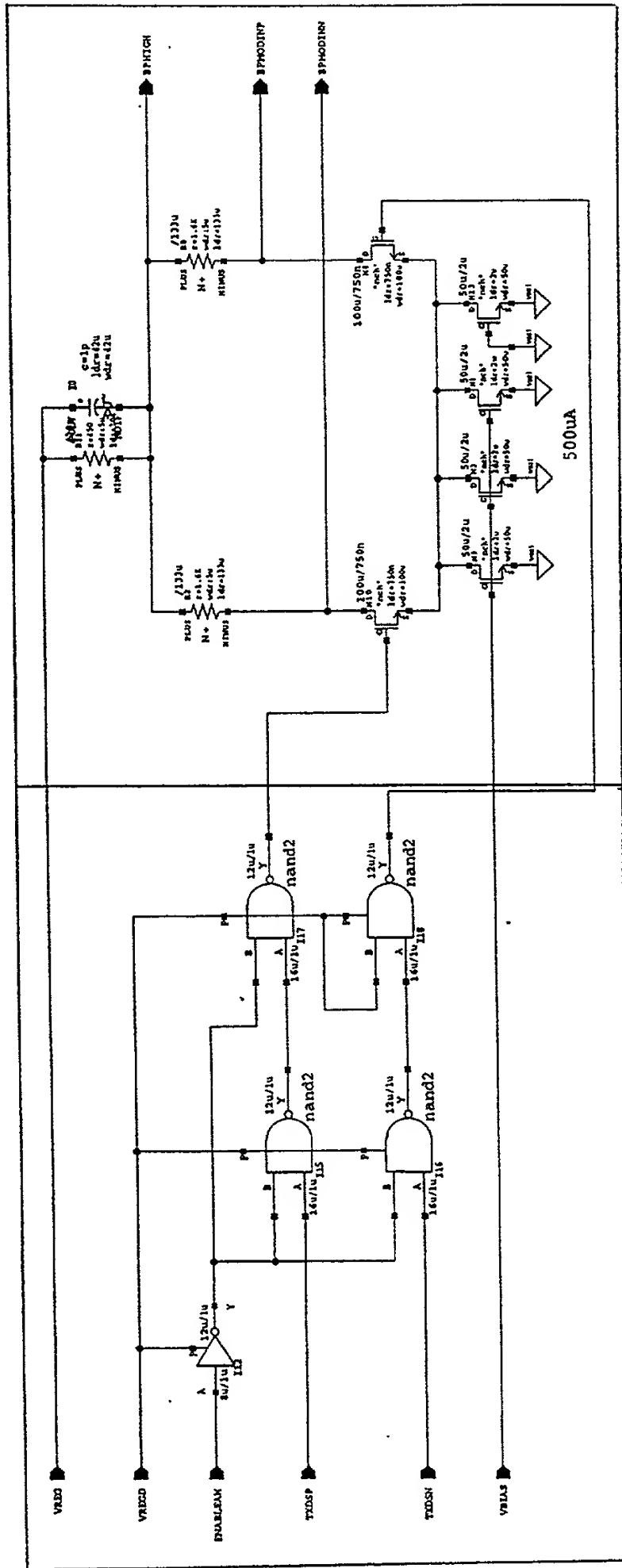


FIG. 8.0603

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TYPE: BPSK Modulation Driver	
INTEGRATED CIRCUIT DESIGN		IBIAS=500uA	
CONFIDENTIAL INFORMATION		NAME: 103reva/bobpsk	REV: B8
		DATE: Jan 18 10:28:46 1996	FILE: ril

B8: modified current source

8.0604AB

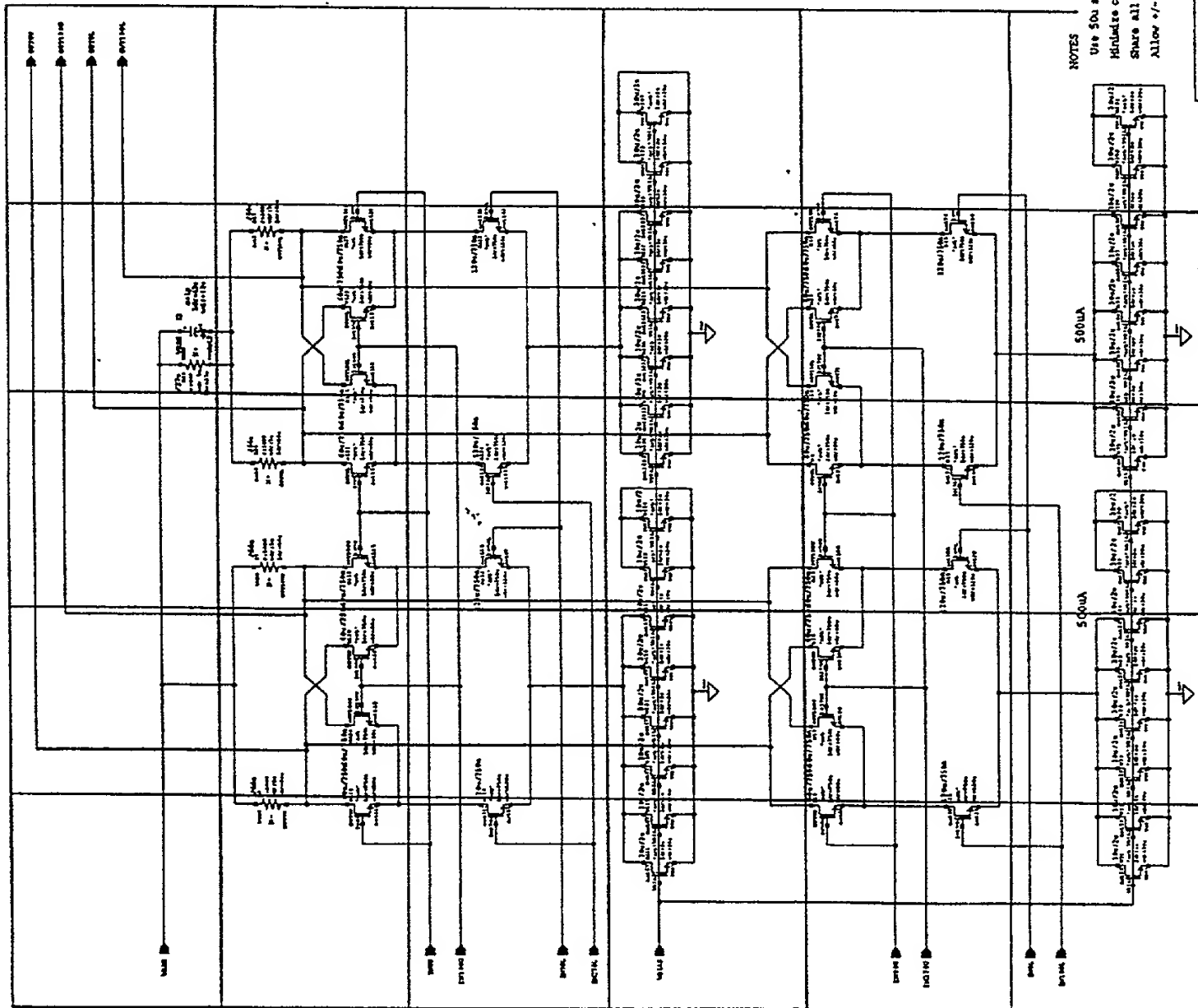
8.0604AA

IF 11 03 88 00 00 00 00 00

8.060401AA	8.060401AB	8.060401AC	8.060401AD	8.060401AE
8.060401BA	8.060401BB	8.060401BC	8.060401BD	8.060401BE
8.060401CA	8.060401CB	8.060401CC	8.060401CD	8.060401CE
8.060401DA	8.060401DB	8.060401DC	8.060401DD	8.060401DE
8.060401EA	8.060401EB	8.060401EC	8.060401ED	8.060401EE
8.060401FA	8.060401FB	8.060401FC	8.060401FD	8.060401FE

II II II 8.060401 II II

FIG. 8.060901



NOTES

Use 50u segments for all devices.
Minimize capacitance on all nodes (drains have priority).
Share all source and drain nodes.
Allow +/- 20% adjustment on resistors at power supply end.

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
Part L01	IBTAS=2mA
Frequency Doubler Core	J07001E
file=610.000	for=2200000
101rev/bcd	11 11 11
Jan 12 15:51:26 1994	

BS: modified current sources

8.0605AB

8.0605AA

II 07 8.0605

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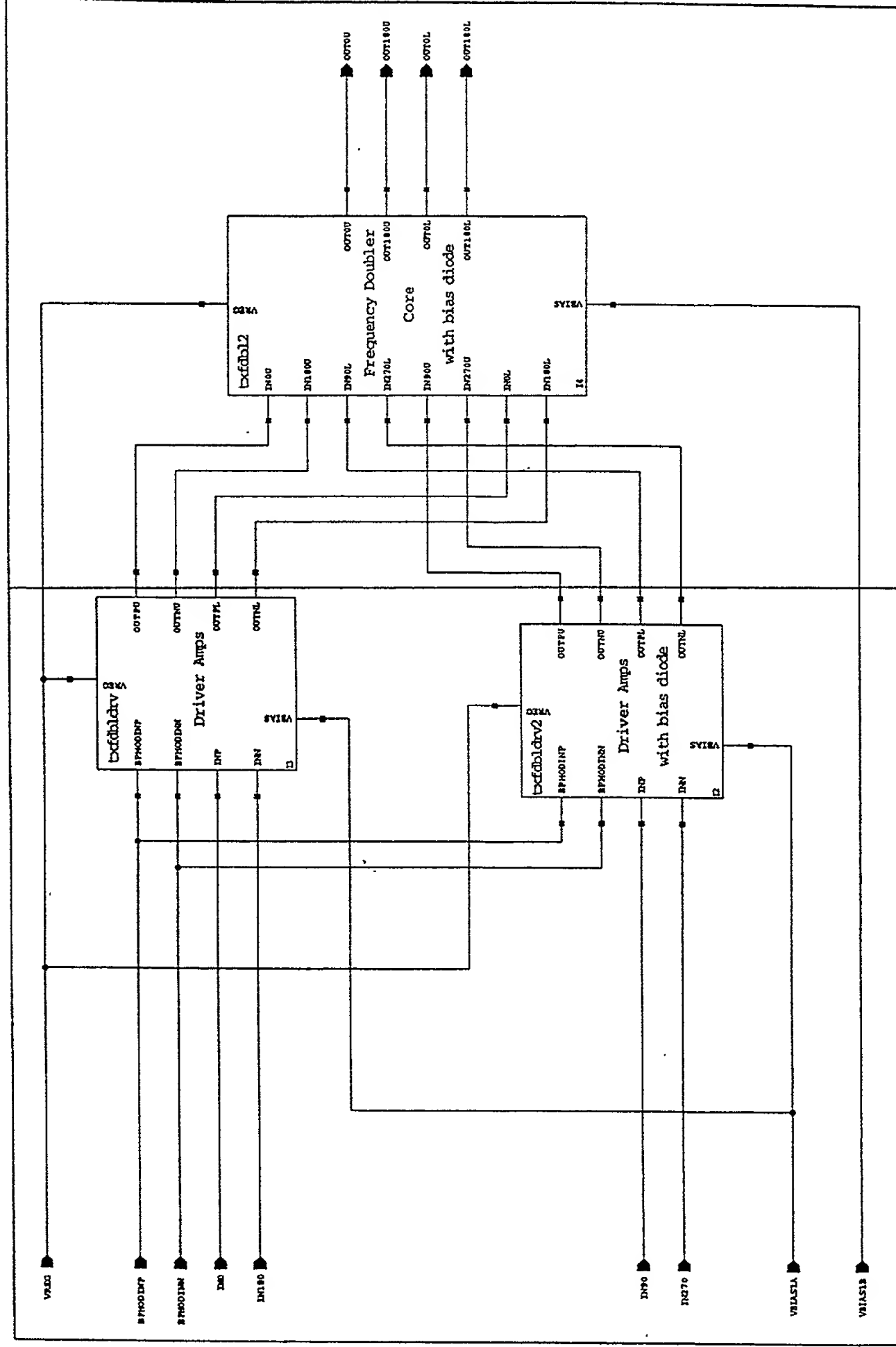


Fig. 8.0605

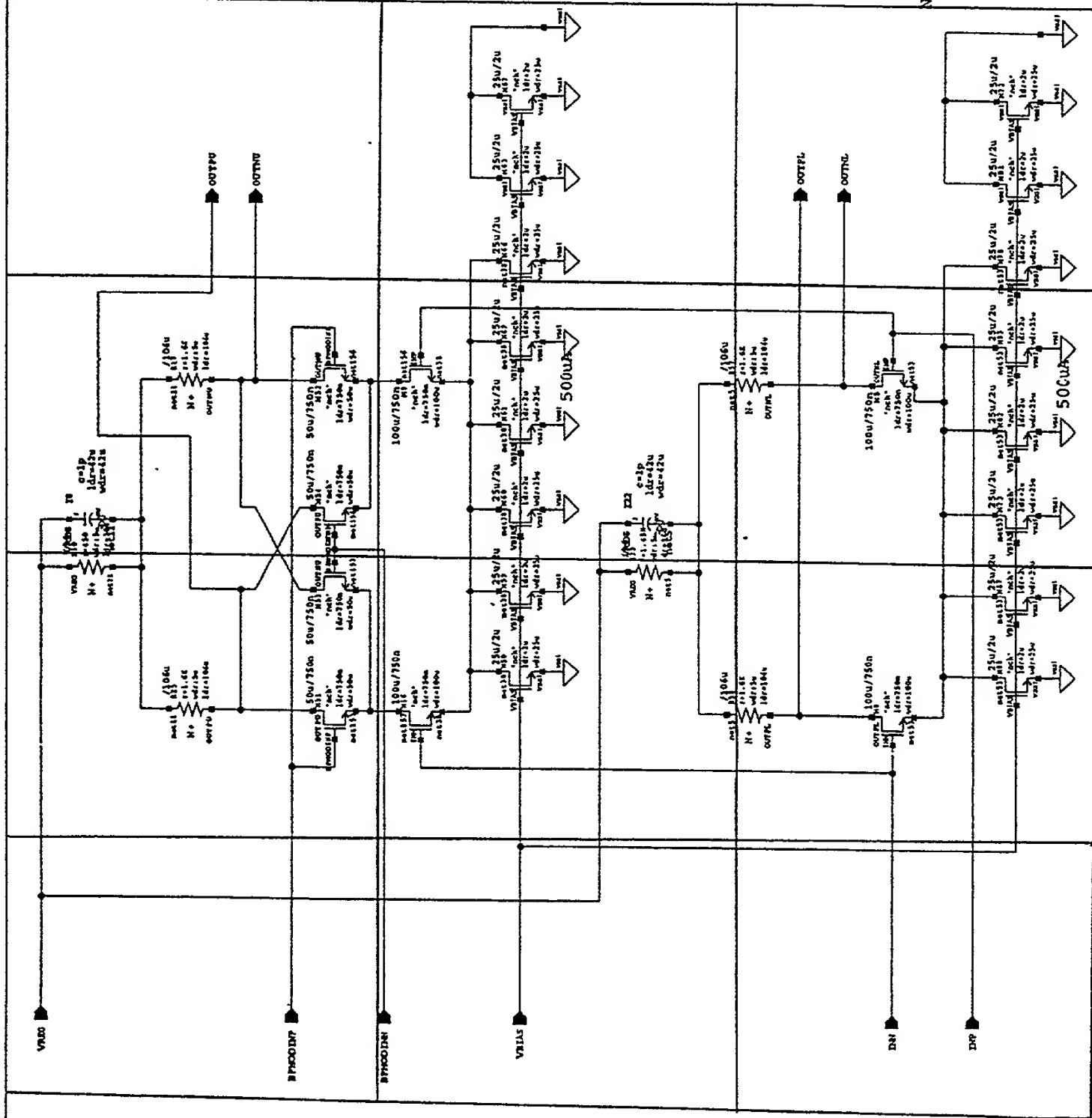
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Frequency Doubler	
INTEGRATED CIRCUIT DESIGN		IBIAS=4mA	
CONFIDENTIAL INFORMATION		NAME: 103reva/bcdoubler2	REV: B8
		DATE: Jan 12 17:22:51 1996	FILE: ml

B8: current sources modified

8.060501AA	8.060501AB	8.060501AC	8.060501AD
8.060501BA	8.060501BB	8.060501BC	8.060501BD
8.060501CA	8.060501CB	8.060501CC	8.060501CD

II II II 8.060501 II

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NOTES

- Minimize capacitance on output nodes.
- Share all source/drain nodes.
- Allow +/- 20% adjustment on resistors at supply end.

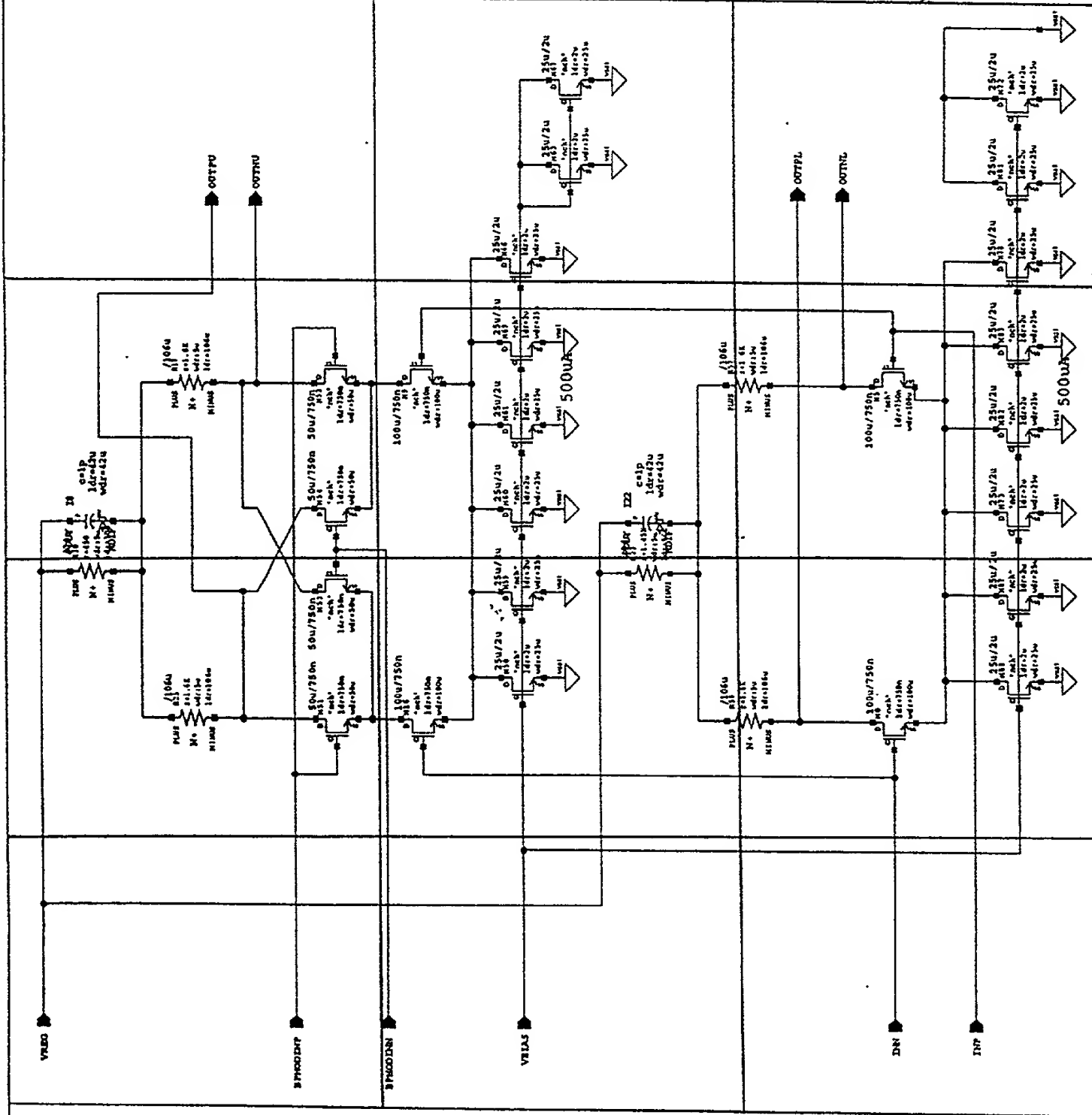
FIG. 8.060501

MICRON		DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TIME: Doubler Driver Amps
INTEGRATED CIRCUIT DESIGN		IBIAS=1mA
CONFIDENTIAL INFORMATION		NAME: 103reva/bxtdbdrv
		REV: B8
		DATE: Jan 12 15:37:26 1996

B8: modified current sources

8.060502AA	8.060502AB	8.060502AC	8.060502AD
8.060502BA	8.060502BB	8.060502BC	8.060502BD
8.060502CA	8.060502CB	8.060502CC	8.060502CD

Итого 8.060502



NOTES

- Minimize capacitance on output nodes.
- Share all source/drain nodes.
- Allow +/- 20% adjustment on resistors at supply end.

FIG. 8.060502

B8: modified current sources

NOODIN COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROD DATE: L03	DESIGNER: JOTOOLE
----------------	-------------------

TEL.	Doubler Driver Amps
100	100
200	200
300	300
400	400
500	500
600	600
700	700
800	800
900	900
1000	1000
1100	1100
1200	1200
1300	1300
1400	1400
1500	1500
1600	1600
1700	1700
1800	1800
1900	1900
2000	2000
2100	2100
2200	2200
2300	2300
2400	2400
2500	2500
2600	2600
2700	2700
2800	2800
2900	2900
3000	3000
3100	3100
3200	3200
3300	3300
3400	3400
3500	3500
3600	3600
3700	3700
3800	3800
3900	3900
4000	4000
4100	4100
4200	4200
4300	4300
4400	4400
4500	4500
4600	4600
4700	4700
4800	4800
4900	4900
5000	5000
5100	5100
5200	5200
5300	5300
5400	5400
5500	5500
5600	5600
5700	5700
5800	5800
5900	5900
6000	6000
6100	6100
6200	6200
6300	6300
6400	6400
6500	6500
6600	6600
6700	6700
6800	6800
6900	6900
7000	7000
7100	7100
7200	7200
7300	7300
7400	7400
7500	7500
7600	7600
7700	7700
7800	7800
7900	7900
8000	8000
8100	8100
8200	8200
8300	8300
8400	8400
8500	8500
8600	8600
8700	8700
8800	8800
8900	8900
9000	9000
9100	9100
9200	9200
9300	9300
9400	9400
9500	9500
9600	9600
9700	9700
9800	9800
9900	9900
10000	10000

IBIAS=1mA

13444 103reva/1x fdb]drv2

DATE: JAN 18 08:22:12 1996

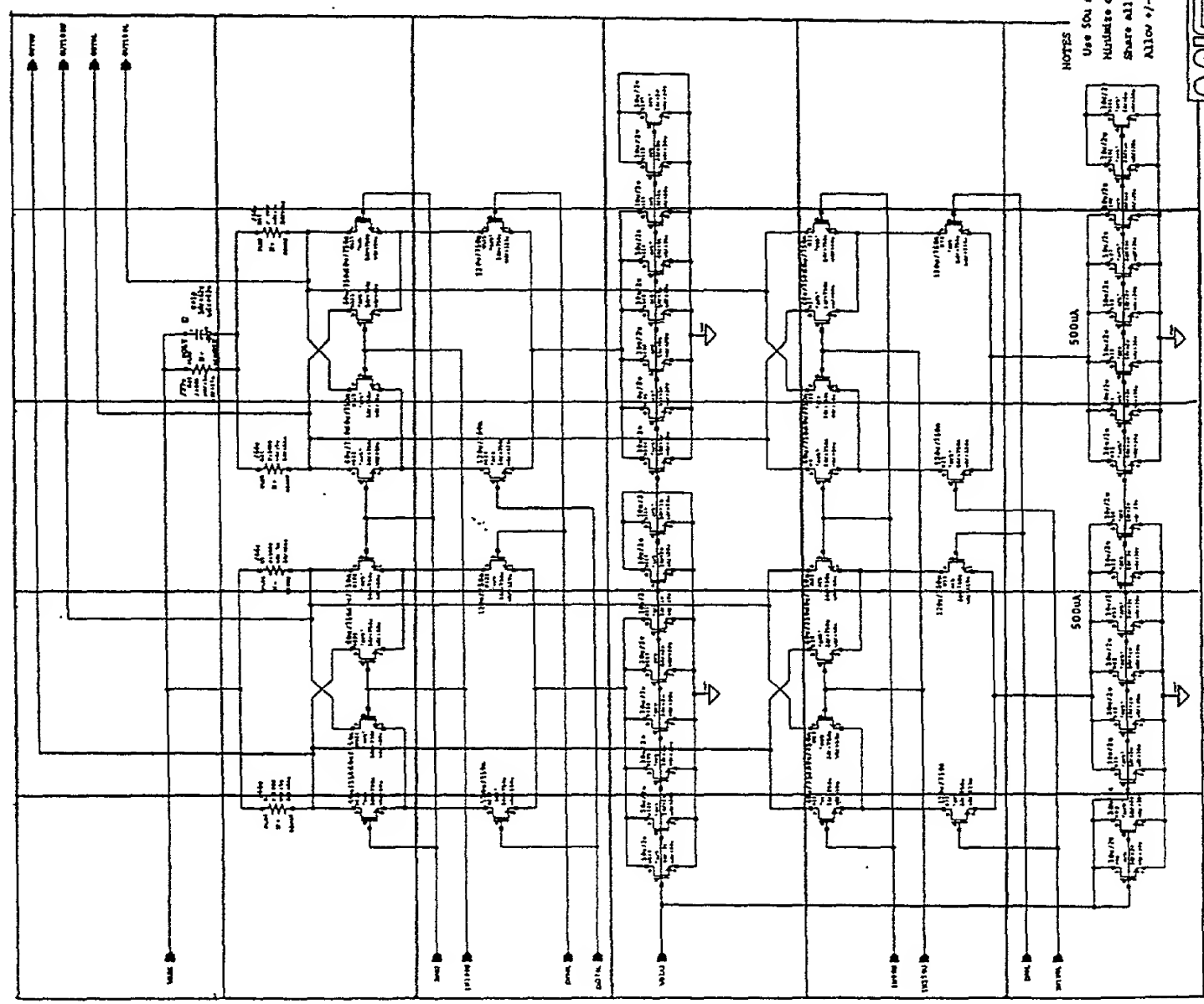
14303

14303

8.060503AA	8.060503AB	8.060503AC	8.060503AD	8.060503AE
8.060503BA	8.060503BB	8.060503BC	8.060503BD	8.060503BE
8.060503CA	8.060503CB	8.060503CC	8.060503CD	8.060503CE
8.060503DA	8.060503DB	8.060503DC	8.060503DD	8.060503DE
8.060503EA	8.060503EB	8.060503EC	8.060503ED	8.060503EE
8.060503FA	8.060503FB	8.060503FC	8.060503FD	8.060503FE

正 正 正 8.060503

1. This circuit is a modified current source.
 2. The circuit is designed to operate at 1.22GHz.
 3. The circuit is designed to operate at 1.22GHz.
 4. The circuit is designed to operate at 1.22GHz.



NOTES
 Use 50u segments for all devices.
 Minimize capacitance on all nodes (drains have priority).
 Share all source and drain nodes.
 Allow +/- 20% adjustment on resistors at power supply end.

MICRON		IBIAS=2mA
COMMUNICATIONS, INC.	Frequency Doubler Core	
INTEGRATED CIRCUIT DESIGN	Fin=410.4MHz	Io=1.22GHz
CONFIDENTIAL INFORMATION	100pF/100nF/100mF	88
		Jan 18 08:23:28 1996

88: modified current source

FIG. 8.060503

8.0606AA	8.0606AB	8.0606AC	8.0606AD	8.0606AE	8.0606AF	8.0606AG	8.0606AH
8.0606BA	8.0606BB	8.0606BC	8.0606BD	8.0606BE	8.0606BF	8.0606BG	8.0606BH
8.0606CA	8.0606CB	8.0606CC	8.0606CD	8.0606CE	8.0606CF	8.0606CG	8.0606CH
8.0606DA	8.0606DB	8.0606DC	8.0606DD	8.0606DE	8.0606DF	8.0606DG	8.0606DH
8.0606EA	8.0606EB	8.0606EC	8.0606ED	8.0606EE	8.0606EF	8.0606EG	8.0606EH
8.0606FA	8.0606FB	8.0606FC	8.0606FD	8.0606FE	8.0606FF	8.0606FG	8.0606FH
				8.0606GE			
8.0606HA	8.0606HB	8.0606HC	8.0606HD	8.0606HE			
				8.0606IE			
							8.0606CI
							8.0606DI
							8.0606EI
							8.0606FI

MICRON

INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Transmitter Power Amp
IBU05-25sk (H) 2.25sk(L)
103revs/expoweramp
Jan 12 17:27:33 1996

28: current sources modified

MICROON		PROJECT	LO3	ISSUES	JOTOOOLE
COMMUNICATIONS, INC.					
NEW Transducer Power Amp					
18L2A-5, 25MA (H) 2.25MA(L)					
*** 1037964/2400000 ***					
*** 88 ***					
*** Jan 12 17:27:33 1998 ***					
CONFIDENTIAL INFORMATION					

8.0607AA 8.0607AB 8.0607AC 8.0607AD 8.0607AE 8.0607AF 8.0607AG 8.0607AH 8.0607AI 8.0607AJ

8.0607AA	8.0607AB	8.0607AC	8.0607AD	8.0607AE	8.0607AF	8.0607AG	8.0607AH	8.0607AI	8.0607AJ
8.0607BA	8.0607BB	8.0607BC	8.0607BD	8.0607BE	8.0607BF	8.0607BG	8.0607BH	8.0607BI	8.0607BJ
8.0607CA	8.0607CB	8.0607CC	8.0607CD	8.0607CE	8.0607CF	8.0607CG	8.0607CH	8.0607CI	8.0607CJ
8.0607DA	8.0607DB	8.0607DC	8.0607DD	8.0607DE	8.0607DF	8.0607DG	8.0607DH	8.0607DI	8.0607DJ
8.0607EA	8.0607EB	8.0607EC	8.0607ED	8.0607EE	8.0607EF	8.0607EG	8.0607EH	8.0607EI	8.0607EJ
8.0607FA	8.0607FB	8.0607FC	8.0607FD	8.0607FE	8.0607FF	8.0607FG	8.0607FH	8.0607FI	8.0607FJ
8.0607GA	8.0607GB	8.0607GC	8.0607GD	8.0607GE	8.0607GF	8.0607GG	8.0607GH	8.0607GI	8.0607GJ
8.0607HA	8.0607HB	8.0607HC	8.0607HD	8.0607HE	8.0607HF	8.0607HG	8.0607HH	8.0607HI	8.0607HJ
8.0607IA	8.0607IB	8.0607IC	8.0607ID	8.0607IE	8.0607IF	8.0607IG	8.0607IH	8.0607II	8.0607IJ
8.0607JA	8.0607JB	8.0607JC	8.0607JD	8.0607JE	8.0607JF	8.0607JG	8.0607JH	8.0607JI	8.0607JJ

8.0607KA 8.0607KB 8.0607KC 8.0607KD 8.0607KE 8.0607KF 8.0607KG 8.0607KH 8.0607KI 8.0607KJ

CONFIDENTIAL

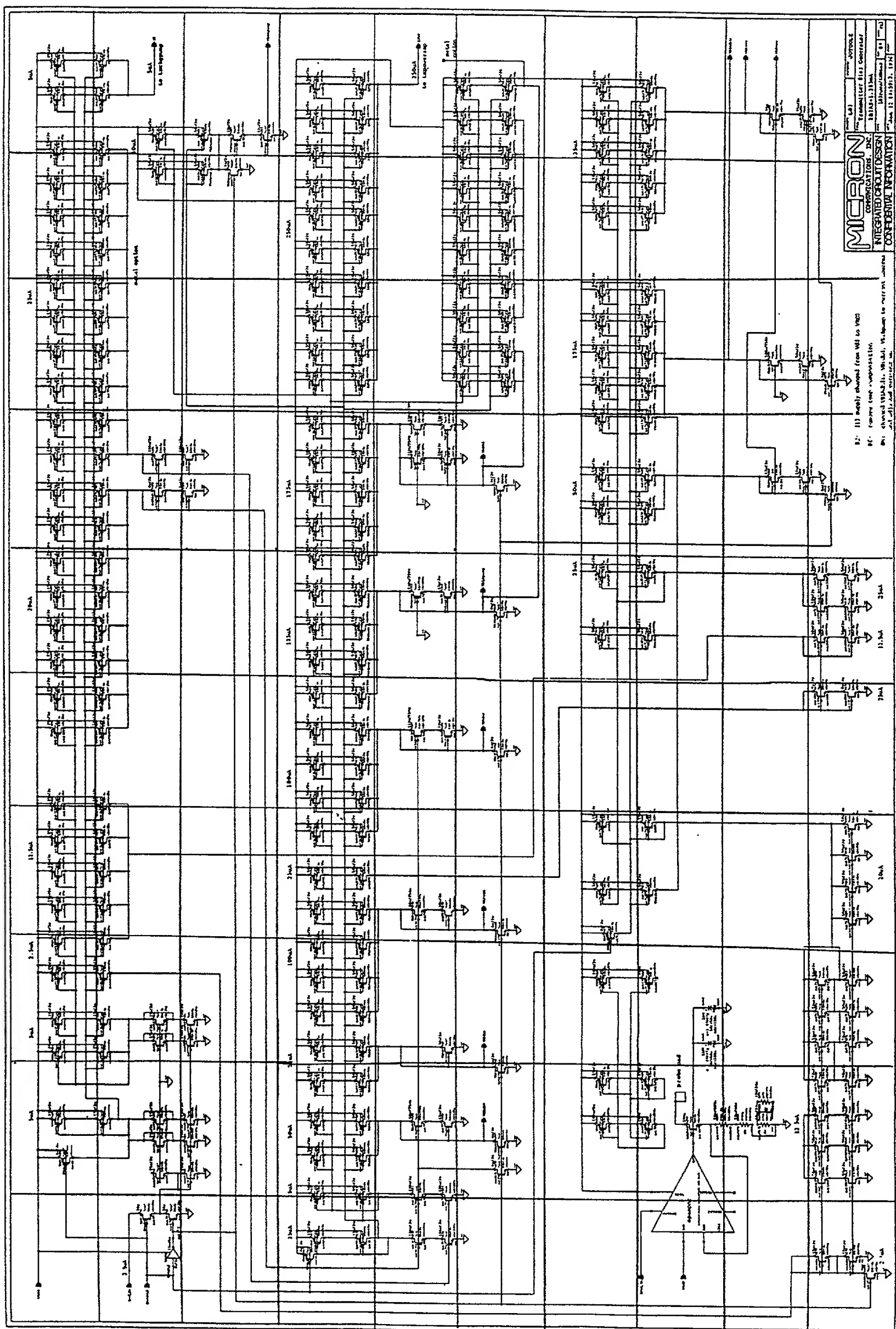
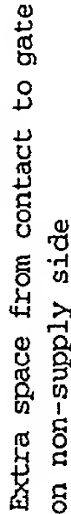


Fig. 8.0607

8.0608AA	8.0608AB
8.0608BA	8.0608BB

8.0608BB



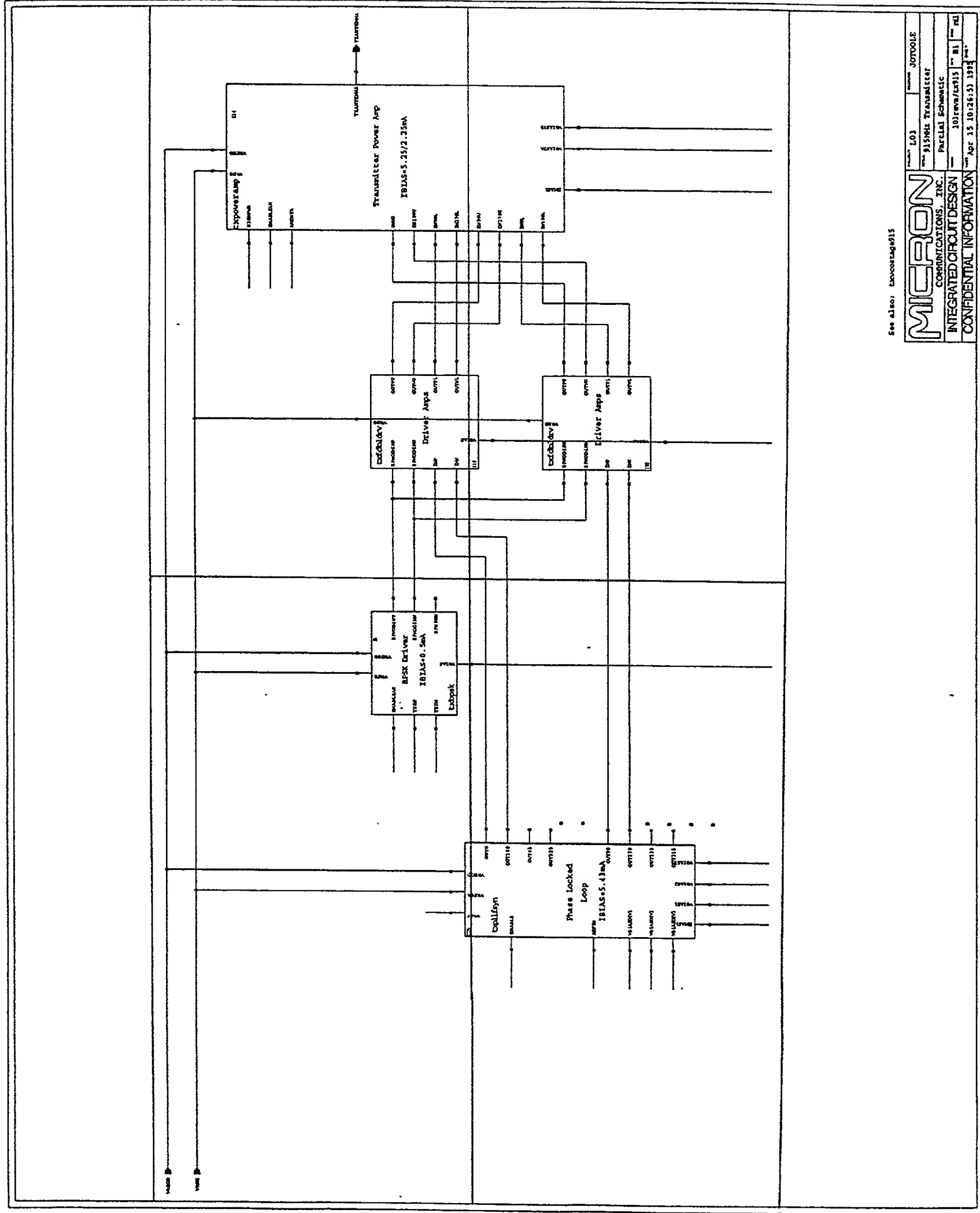
B8: initial release of this design
B10: disconnected inverter

PROJECT: L03	DESIGNER: JOTOOLE	
TITLE: Modulated Backscatter		
Transmitter		
NAME: 103reva/txmb	REV: B10	SIZE: A
DATE: Mar 26 11:07:42 1996		SHEET:

Fig. 8.0608

8.07AA	8.07AB
8.07BA	8.07BB

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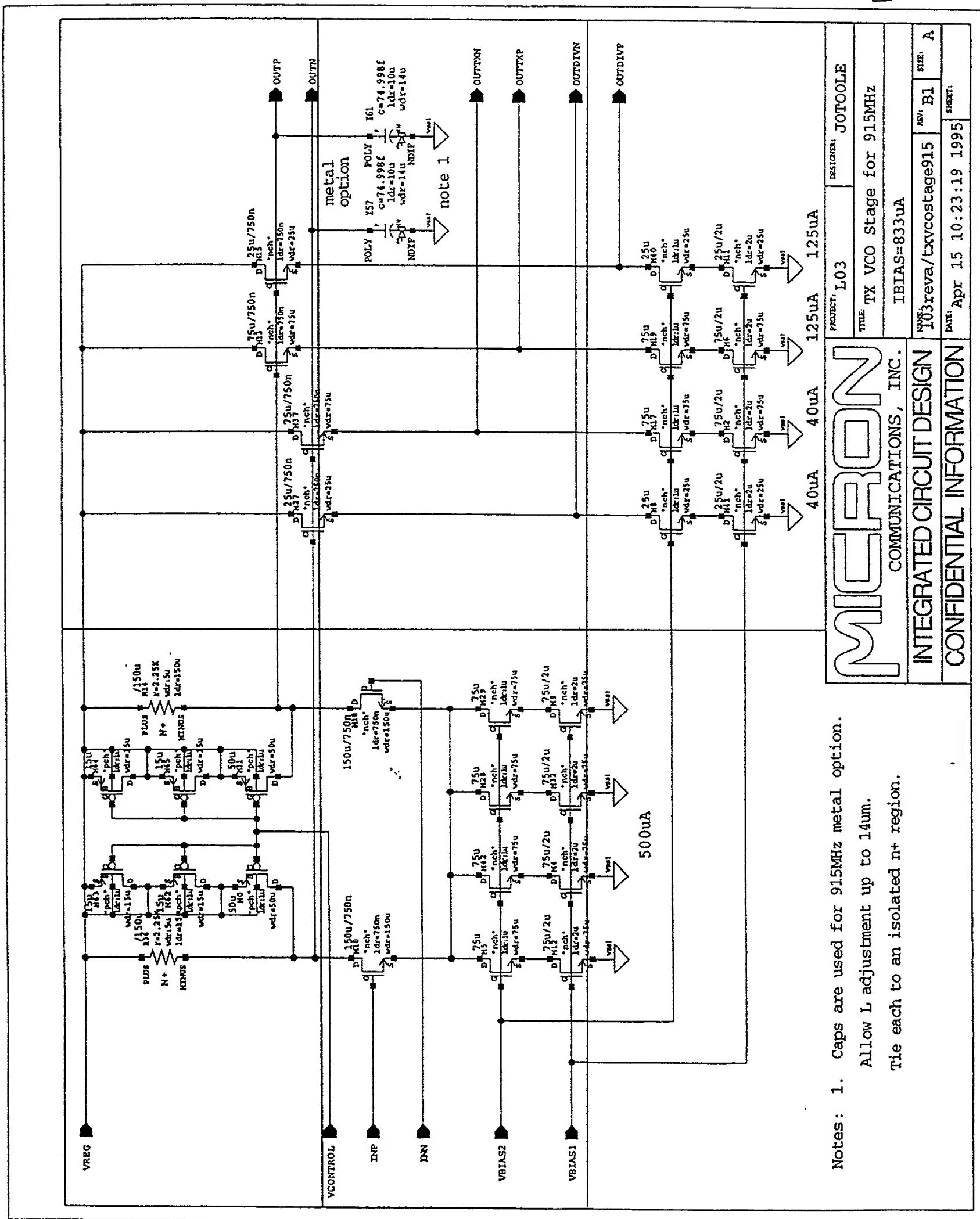
See also: L000000000000

MICRON		L03	J00000
COMMUNICATIONS, INC.		315MHz Transmitter	
INTEGRATED CIRCUIT DESIGN		Partial Schematic	
CONFIDENTIAL INFORMATION		101rev/0015	BI
		Apr 15 10:26:53 1992	

FIG. 8.07

8.0701AA	8.0701AB
8.0701BA	8.0701BB
8.0701CA	8.0701CB

II II III III III III



9AA	9AB
9BA	9BB
9CA	9CB

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 AND IS NOT INTENDED TO BE USED IN CONNECTION WITH
 ANY STANDARD, SPECIFICATION, OR OTHER TECHNICAL
 REQUIREMENT.

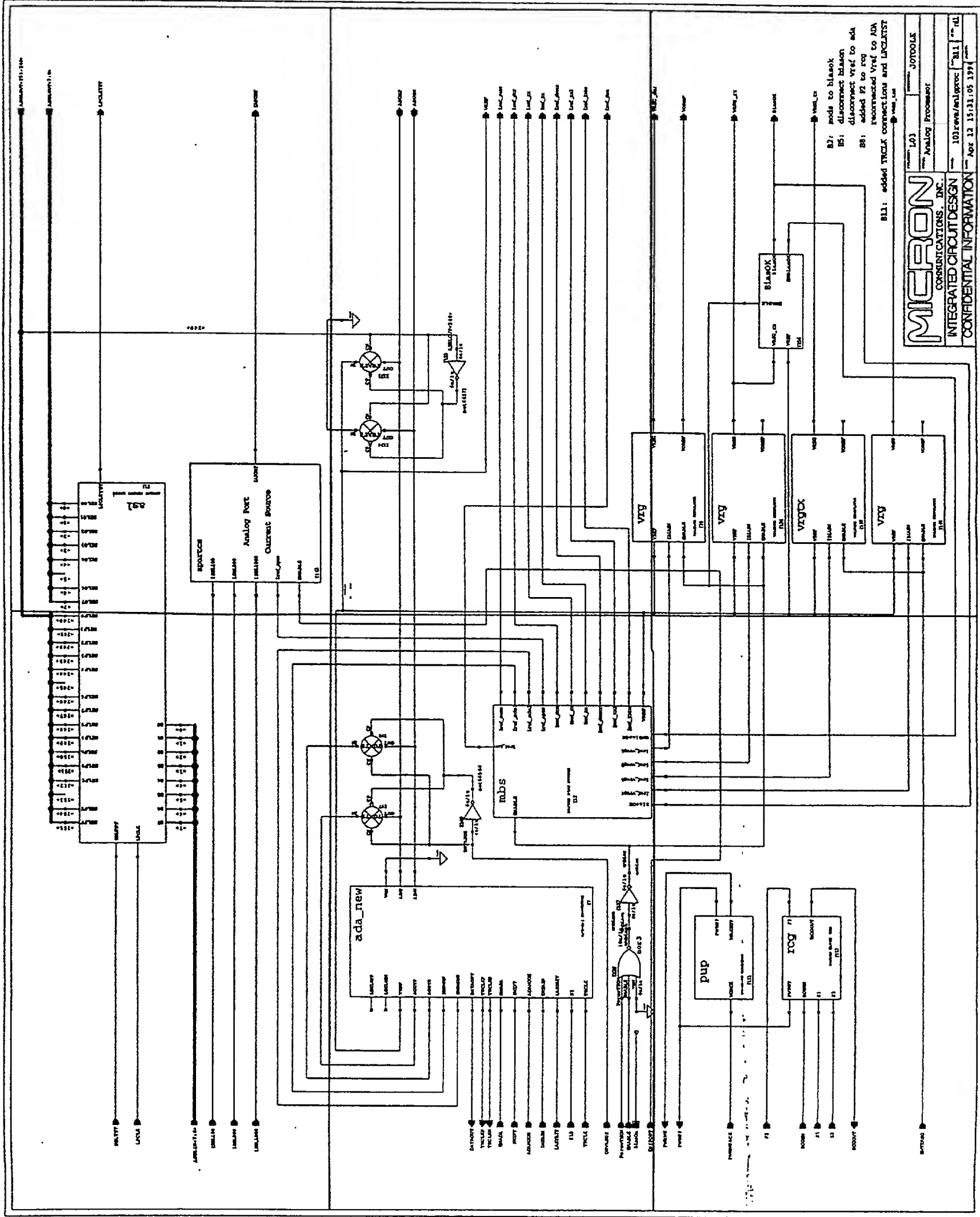
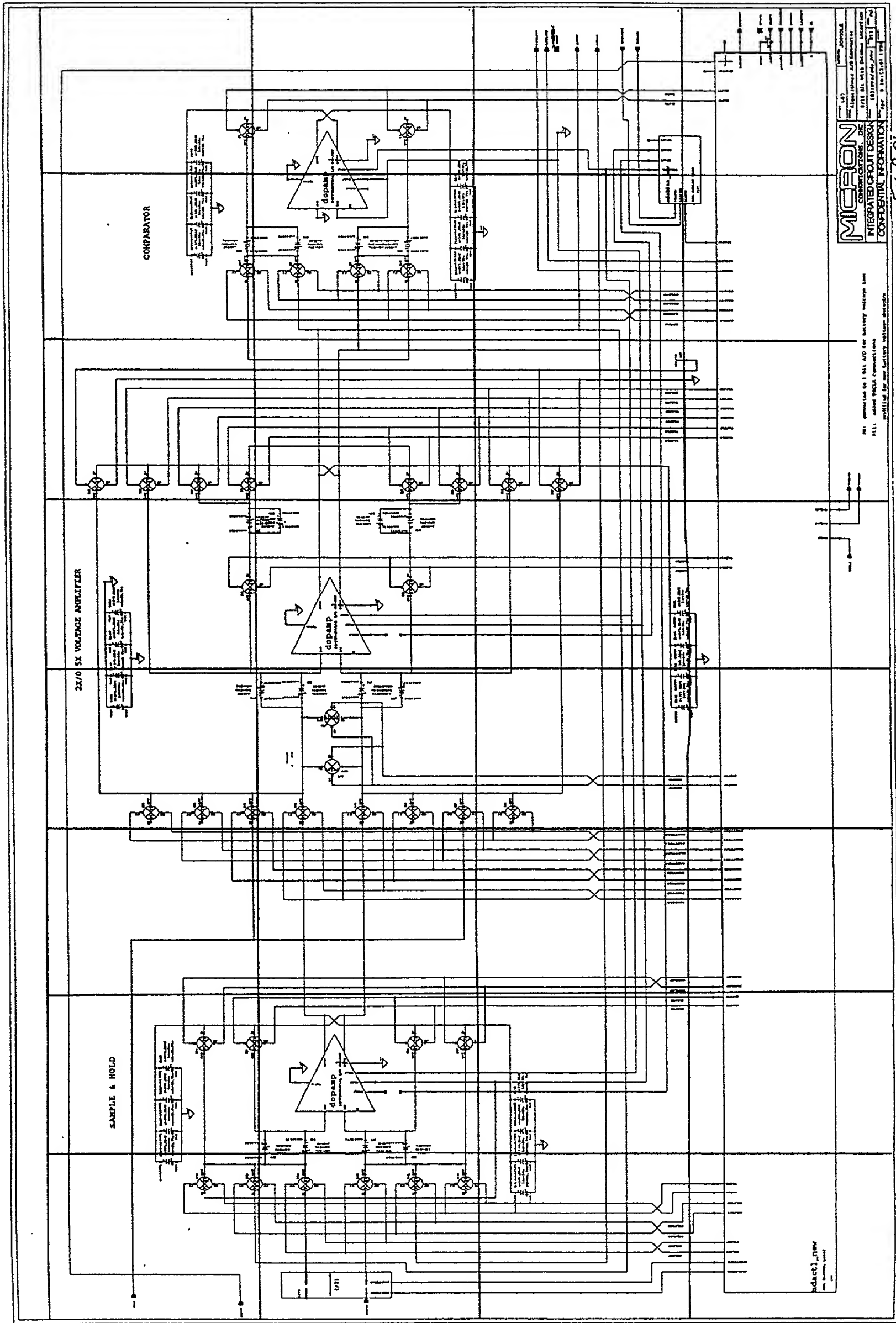


Fig. 9

9.01AA	9.01AB	9.01AC	9.01AD	9.01AE	9.01AF	9.01AG	9.01AH
9.01BA	9.01BB	9.01BC	9.01BD	9.01BE	9.01BF	9.01BG	9.01BH
9.01CA	9.01CB	9.01CC	9.01CD	9.01CE	9.01CF	9.01CG	9.01CH
9.01DA	9.01DB	9.01DC	9.01DD	9.01DE	9.01DF	9.01DG	9.01DH

1. This drawing is a schematic diagram of the internal circuitry of the MICRON 22/0 SX Voltage Amplifier. It shows the internal structure of the device, including the input stage, the 22/0 SX Voltage Amplifier, and the output stage. The diagram is intended for use by the user to understand the internal operation of the device and to troubleshoot any problems that may arise.



MICRON
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
Rev. 1.0
Date: 10/11/83
By: [Signature]

FIG. 9.01

9.0101AA	9.0101AB	9.0101AC	9.0101AD	9.0101AE	9.0101AF	9.0101AG	9.0101AH	9.0101AI	9.0101AJ	9.0101AK
9.0101BA	9.0101BB	9.0101BC	9.0101BD	9.0101BE	9.0101BF	9.0101BG	9.0101BH	9.0101BI	9.0101BJ	9.0101BK
9.0101CA	9.0101CB	9.0101CC	9.0101CD	9.0101CE	9.0101CF	9.0101CG	9.0101CH	9.0101CI	9.0101CJ	9.0101CK

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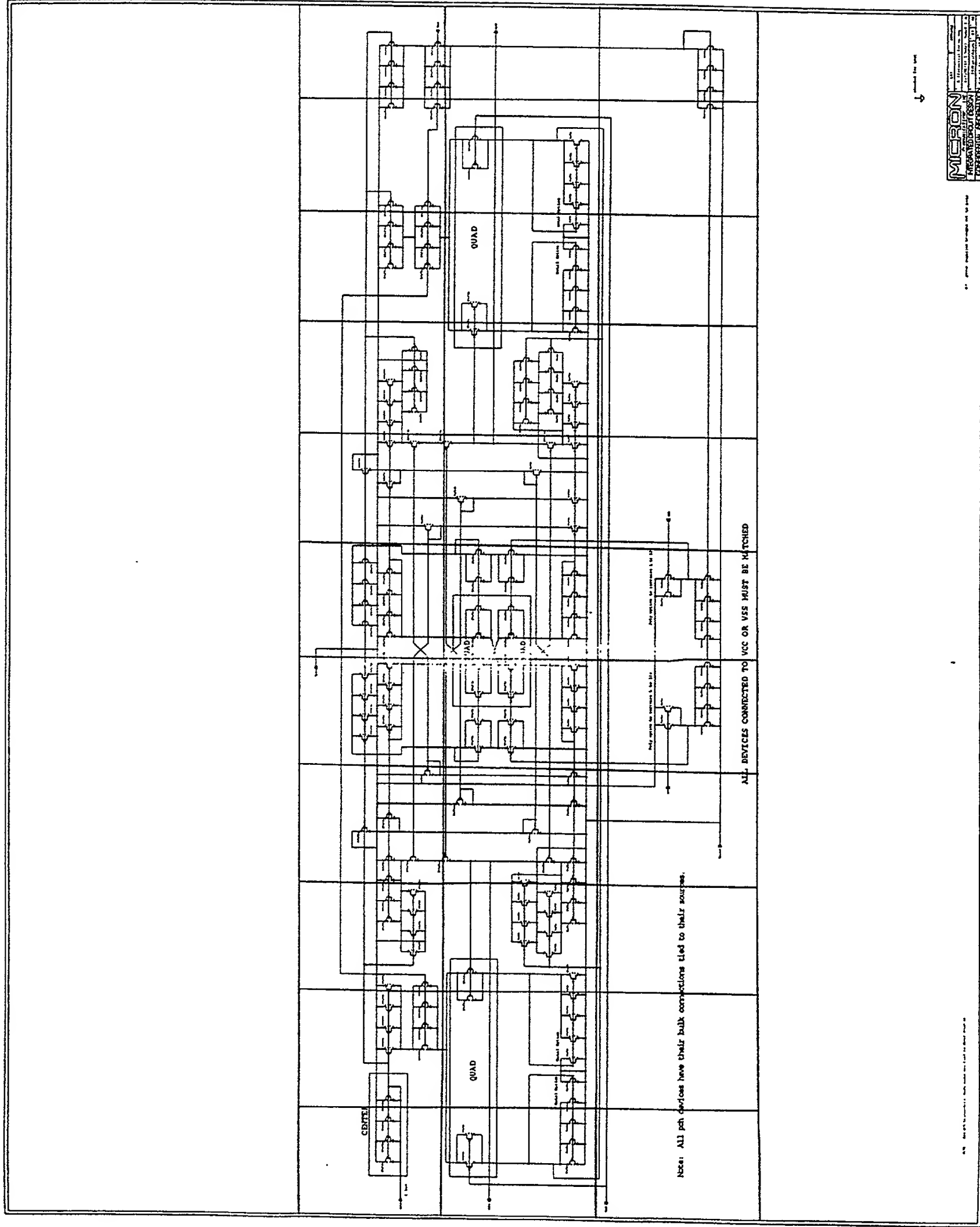
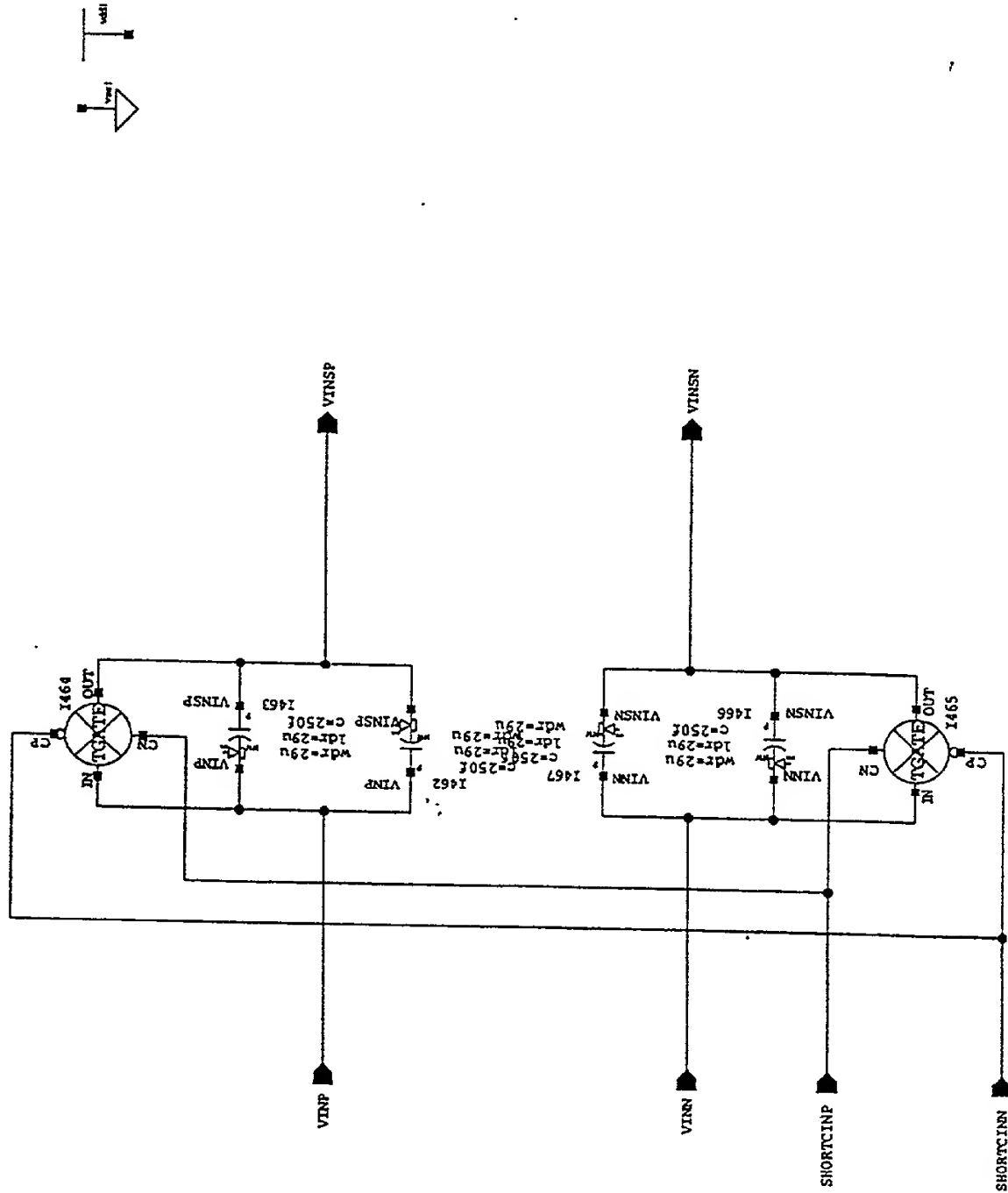


FIG. 9.0101

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PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Analog Divide by 2		REV: B1	
NAME: 103reva/adaprescale		SIZE: A	
DATE: May 19 16:34:53 1995		SHEET: 1	

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

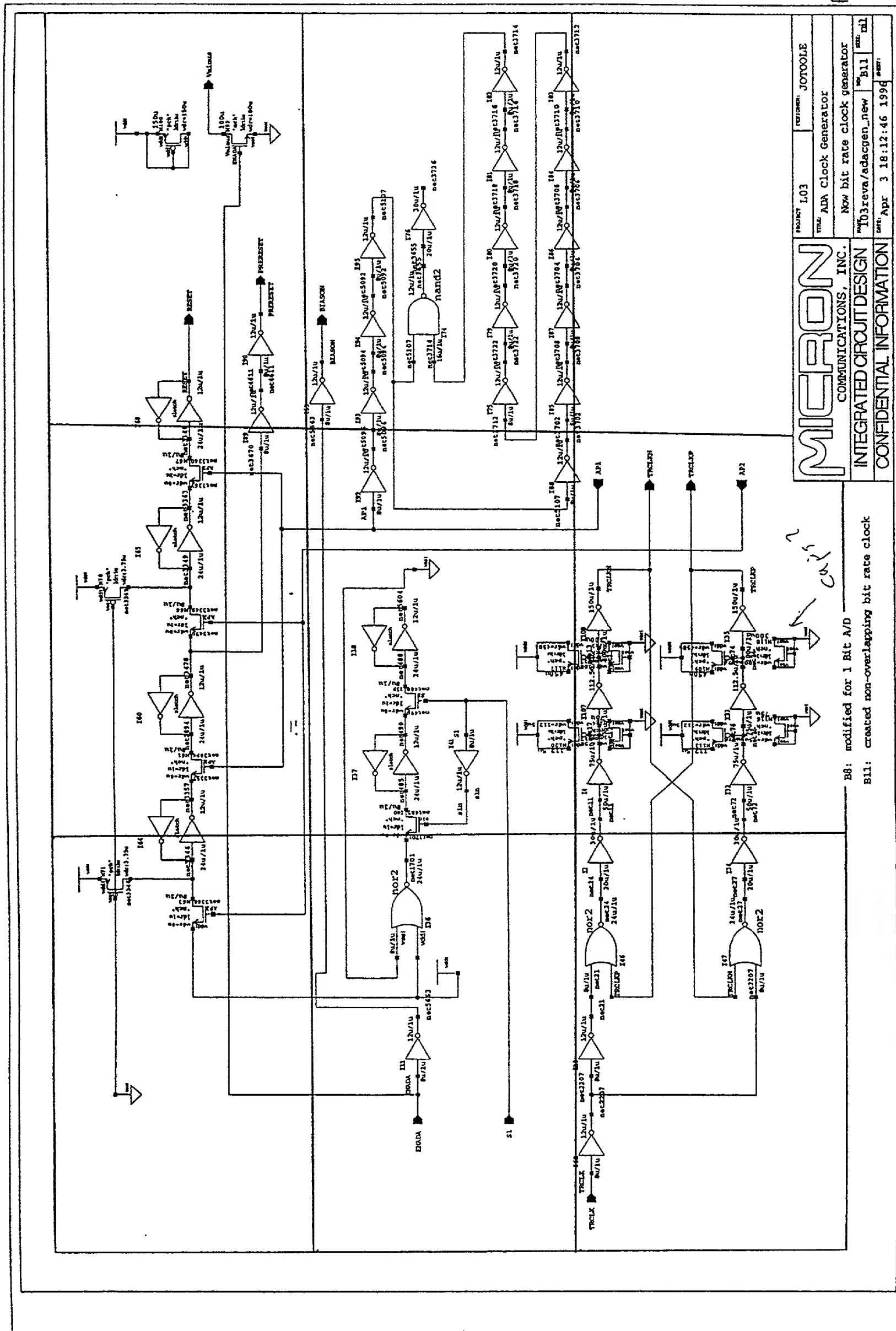
FIG. 9.0102

9.0103BA	9.0103BB	9.0103BC	9.0103BD	9.0103BE	9.0103BF	9.0103BG	9.0103BH		9.0103AJ	9.0103AK	9.0103AL	9.0103AM	9.0103AN	9.0103AO	9.0103AP
9.0103CA	9.0103CB	9.0103CC	9.0103CD	9.0103CE	9.0103CF	9.0103CG	9.0103CH	9.0103CI	9.0103BJ	9.0103BK	9.0103BL	9.0103BM	9.0103BN	9.0103BO	9.0103BP
9.0103DA	9.0103DB	9.0103DC	9.0103DD	9.0103DE	9.0103DF	9.0103DG	9.0103DH	9.0103DI	9.0103CJ	9.0103CK	9.0103CL	9.0103CM	9.0103CN	9.0103CO	9.0103CP
9.0103EA	9.0103EB	9.0103EC	9.0103ED	9.0103EE	9.0103EF	9.0103EG	9.0103EH	9.0103EI	9.0103DJ	9.0103DK	9.0103DL	9.0103DM	9.0103DN	9.0103DO	9.0103DP
9.0103FA	9.0103FB	9.0103FC	9.0103FD	9.0103FE	9.0103FF	9.0103FG	9.0103FH	9.0103FI	9.0103EJ	9.0103EK	9.0103EL	9.0103EM	9.0103EN	9.0103EO	9.0103EP
									9.0103FJ	9.0103FK	9.0103FL	9.0103FM	9.0103FN	9.0103FO	9.0103FP

SECRET

9.010301AA	9.010301AB	9.010301AC
9.010301BA	9.010301BB	9.010301BC
9.010301CA	9.010301CB	9.010301CC

SECRET



9.010302AB

9.010302AA

9.010302

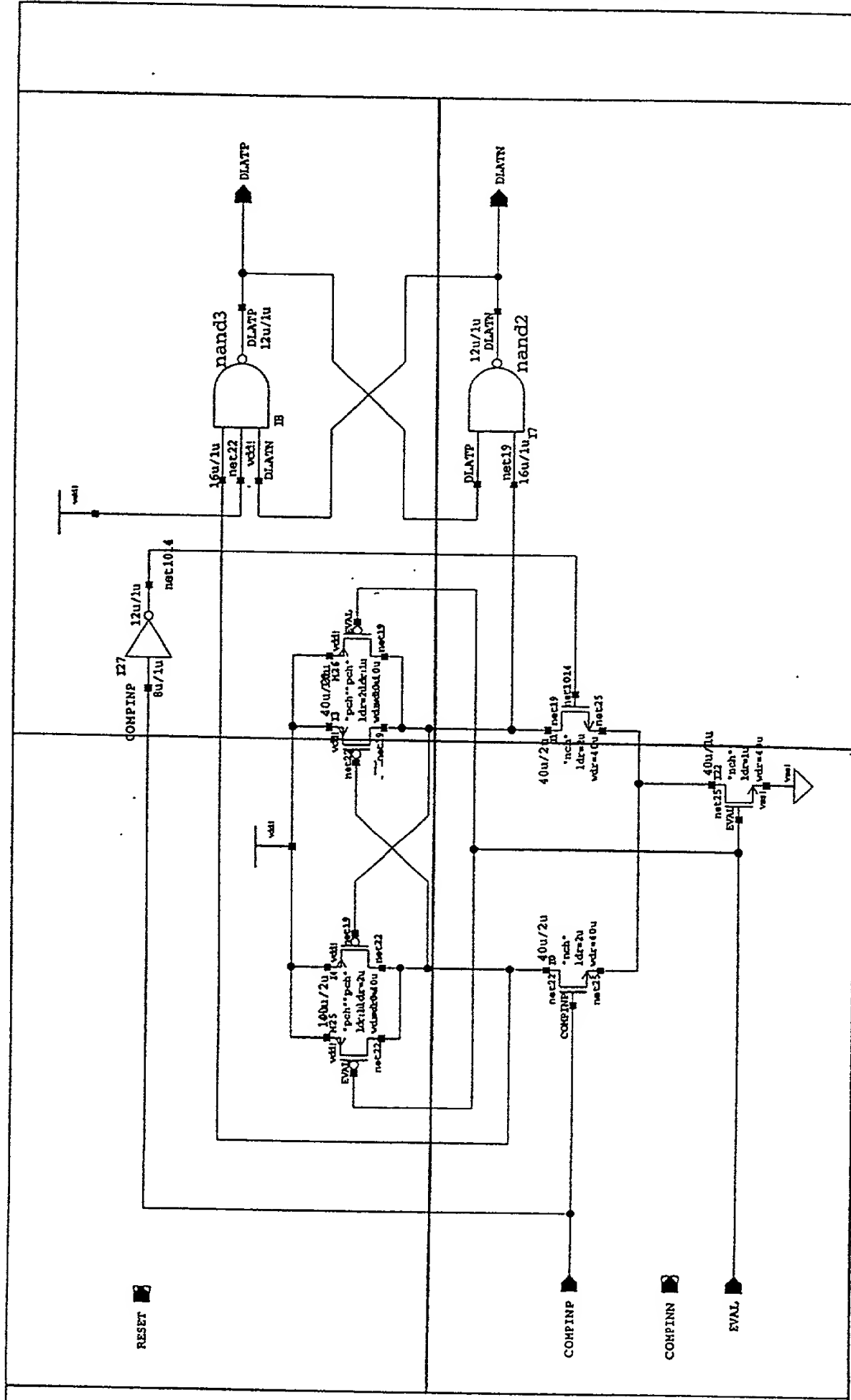
9.010303AA	9.010303AB
------------	------------

EX. 99.11111111

9.010304AA	9.010304AB
9.010304BA	9.010304BB

MI 40-030

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DATE 03-08-2001 BY 60322 UCBAW/DK/STW

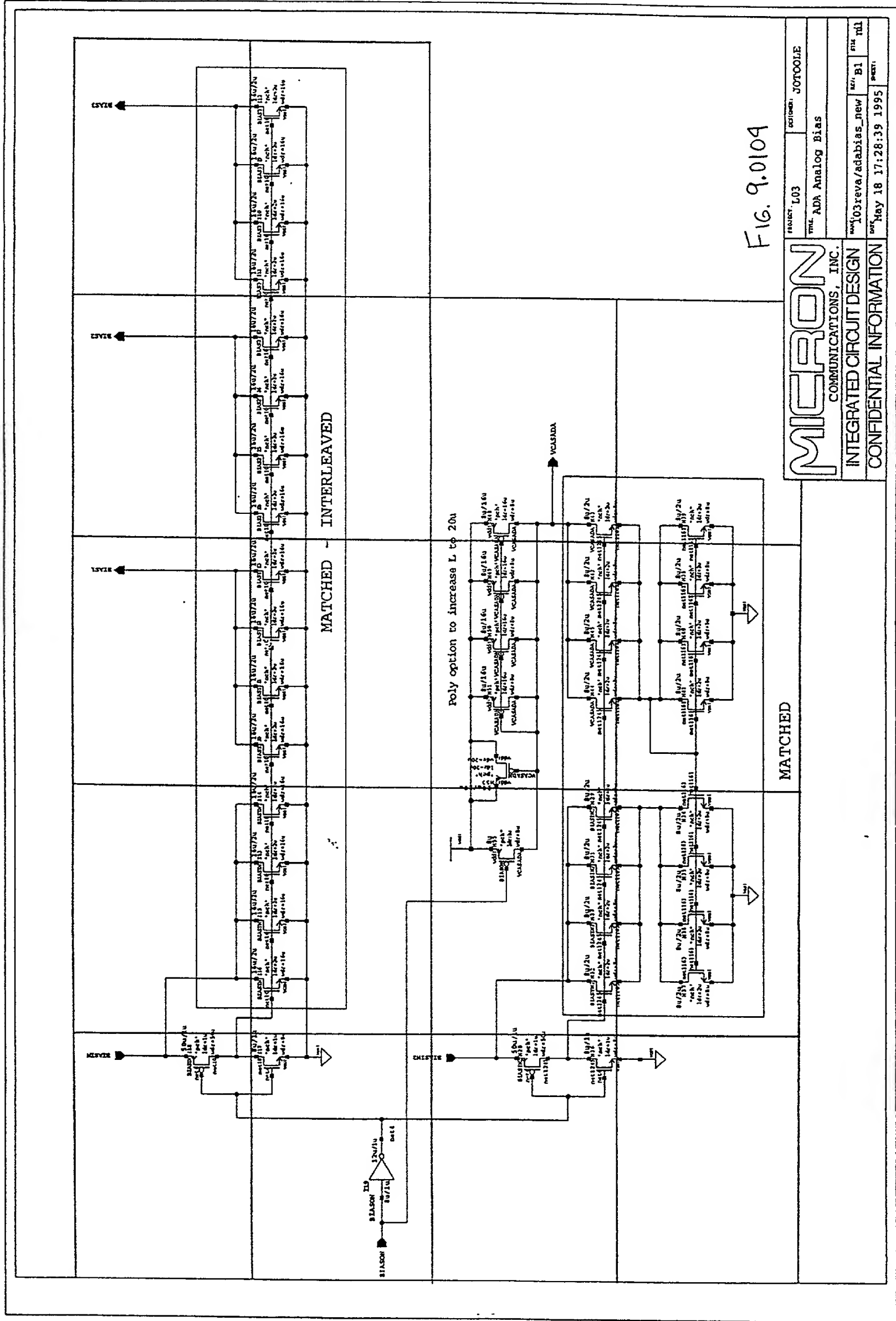


B5: disconnect eval input; connect to vss
B8: reconnect eval and change reset polarity
B11: modified for use in battery voltage sensor

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ADA Data Latch	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/adadlat_new	REV: B11
CONFIDENTIAL INFORMATION		DATE: Apr 8 10:39:12 1996	SIZE: A

Fig. 9.010304

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MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ADA Analog Bias	
INTEGRATED CIRCUIT DESIGN		REV: 103 reva/ada bias_new	REV: B1
CONFIDENTIAL INFORMATION		DATE: May 18 17:28:39 1995	DATE: 01/01/95

9.02AA 9.02AB 9.02AC 9.02AD 9.02AE 9.02AF 9.02AG 9.02AH 9.02AI 9.02AJ 9.02AK

9.02AA	9.02AB	9.02AC	9.02AD	9.02AE	9.02AF	9.02AG	9.02AH	9.02AI	9.02AJ	9.02AK
9.02BA	9.02BB	9.02BC	9.02BD	9.02BE	9.02BF	9.02BG	9.02BH	9.02BI	9.02BJ	9.02BK
9.02CA		9.02CC	9.02CD	9.02CE	9.02CF	9.02CG	9.02CH	9.02CI	9.02CJ	9.02CK
9.02DA	9.02DB	9.02DC	9.02DD		9.02DF	9.02DG	9.02DH	9.02DI	9.02DJ	9.02DK

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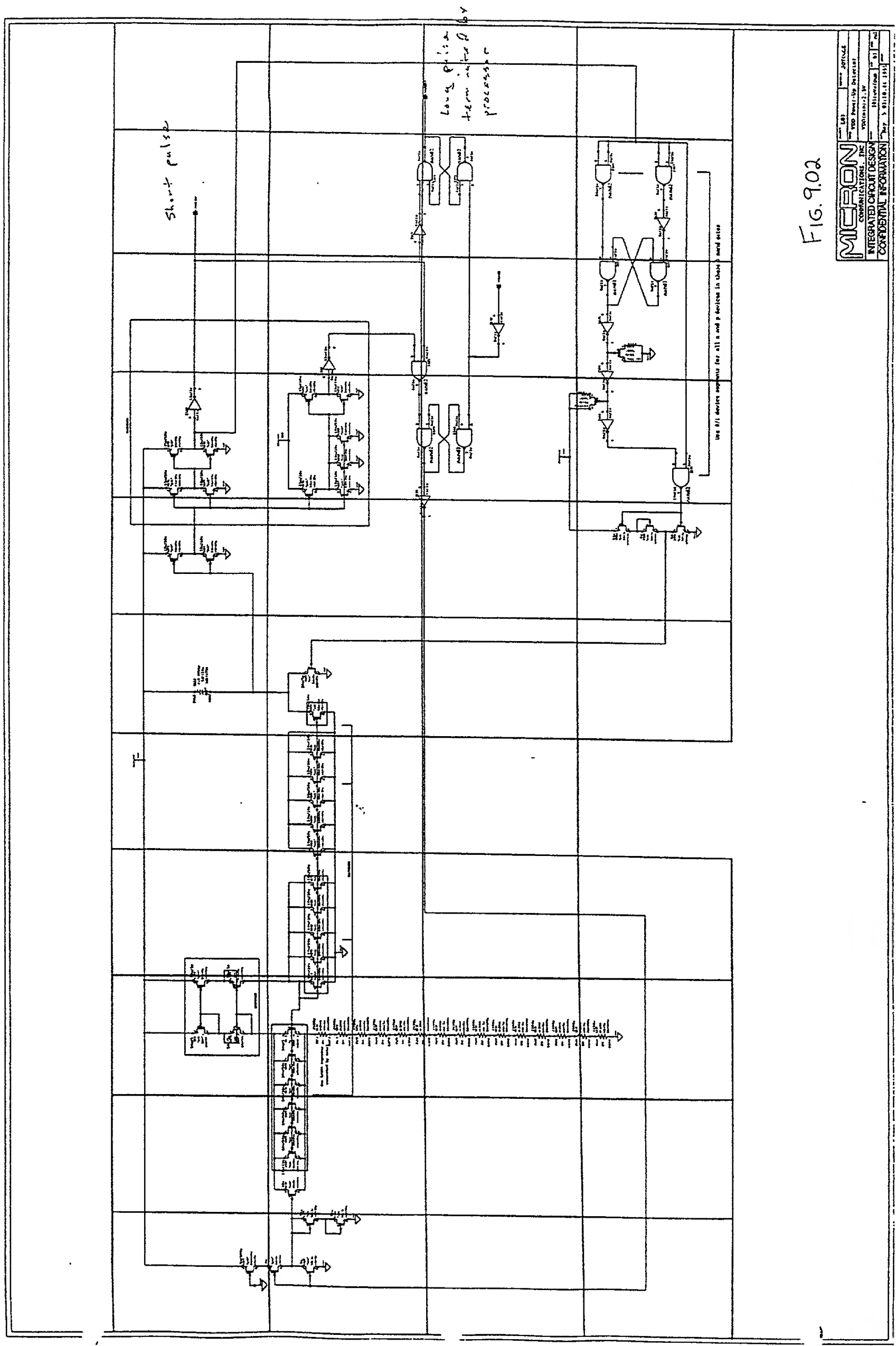
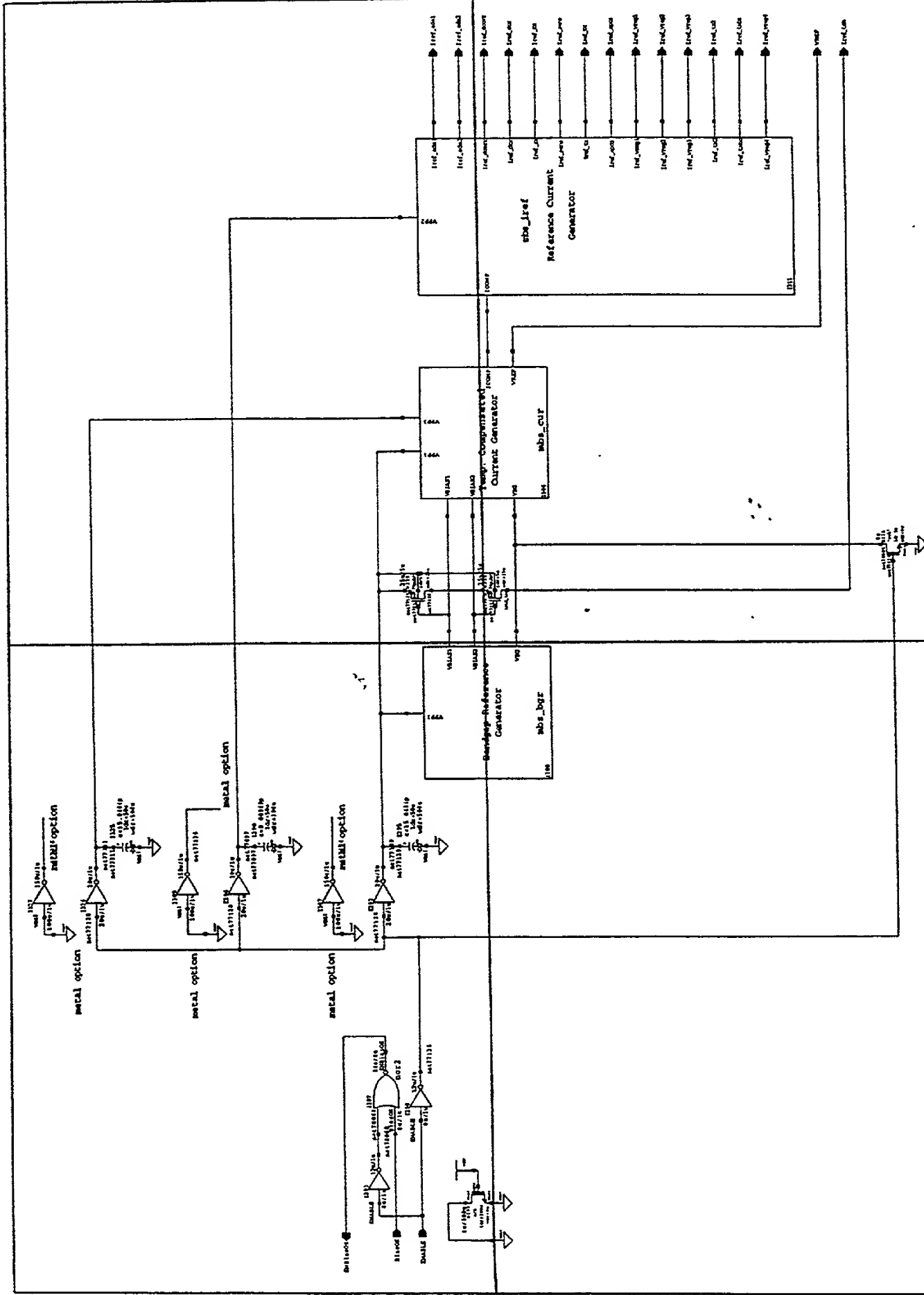


FIG. 9.02

9.03AA	9.03AB
9.03BA	9.03BB

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MICRON		LO3	BIOSING
COMMUNICATIONS, INC.		Master Bias Source	
INTEGRATED CIRCUIT DESIGN		1032000/000	B2
CONFIDENTIAL INFORMATION		Jul 28 11:04:12 1995	01

Ed: Deleted TESTING function
added BIASING logic
created buffered VREF

FIG. 9.03

9.0301AA	9.0301AB	9.0301AC	9.0301AD	9.0301AE	9.0301AF	9.0301AG	9.0301AH	9.0301AI	9.0301AJ
9.0301BA	9.0301BB	9.0301BC	9.0301BD	9.0301BE	9.0301BF	9.0301BG	9.0301BH	9.0301BI	9.0301BJ
	9.0301CB	9.0301CC	9.0301CD	9.0301CE	9.0301CF	9.0301CG	9.0301CH	9.0301CI	9.0301CJ
	9.0301DB	9.0301DC	9.0301DD	9.0301DE	9.0301DF	9.0301DG	9.0301DH	9.0301DI	9.0301DJ

THIS DOCUMENT CONTAINS UNCLASSIFIED INFORMATION
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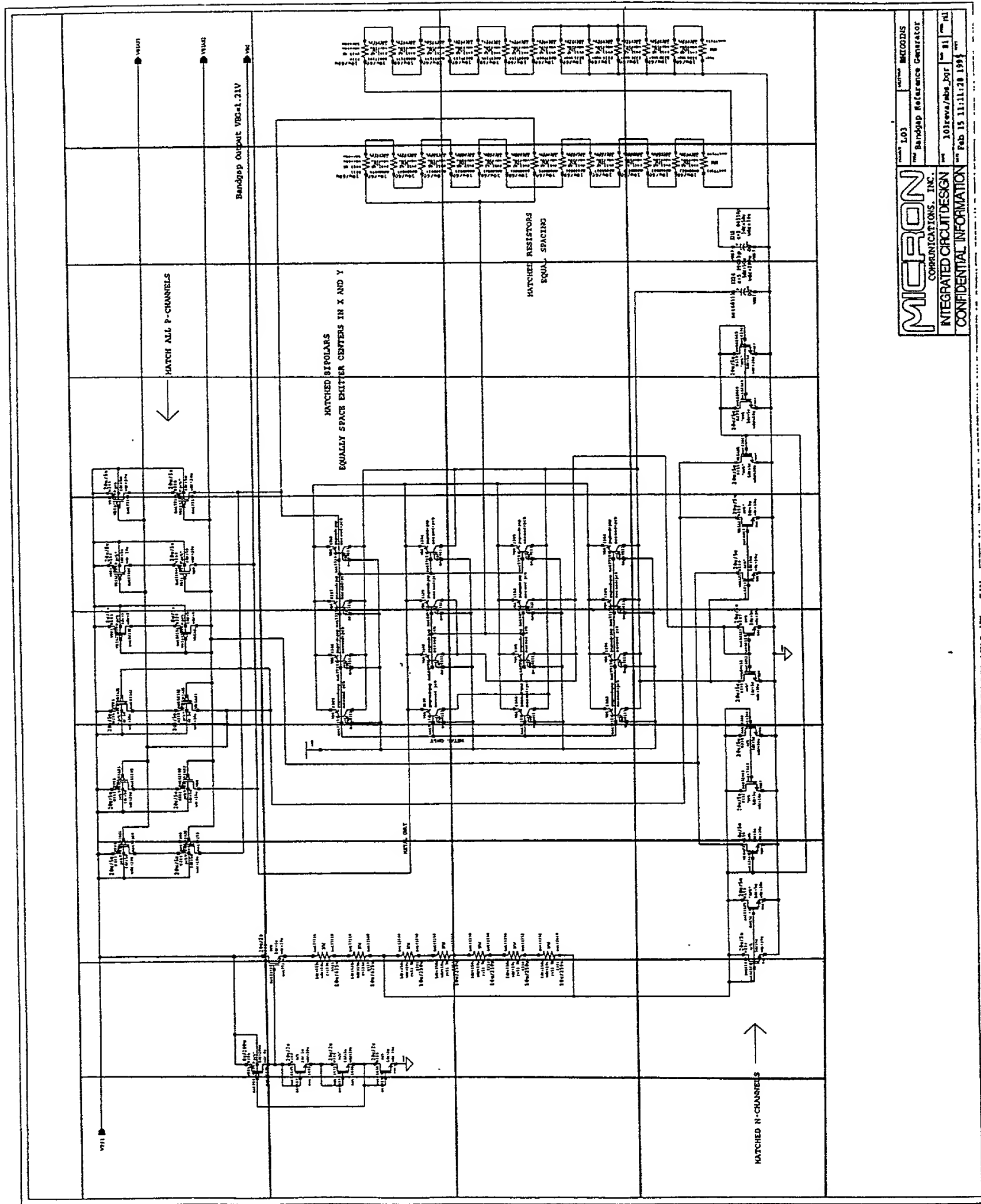


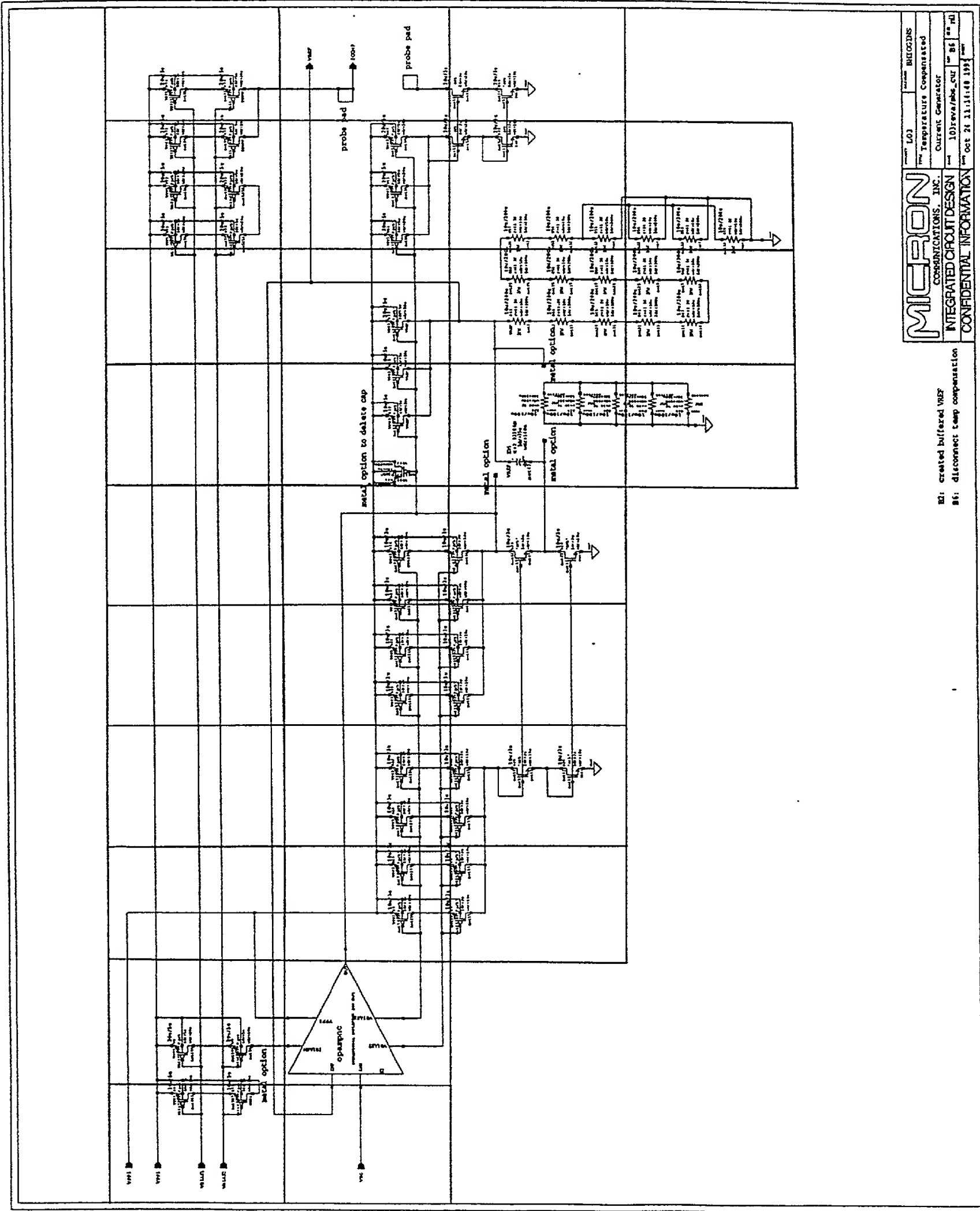
FIG. 9.0301

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
DESIGN NO.	103
DESIGN NAME	BANDGAP REFERENCE CIRCUIT
DESIGNER	103revA/mba_bpf
DATE	FEB 15 11:11:28 1991

9.0302AA	9.0302AB	9.0302AC	9.0302AD	9.0302AE	9.0302AF	9.0302AG	9.0302AH	9.0302AI	9.0302AJ
9.0302BA	9.0302BB	9.0302BC	9.0302BD	9.0302BE	9.0302BF	9.0302BG	9.0302BH	9.0302BI	9.0302BJ
		9.0302CC	9.0302CD	9.0302CE	9.0302CF	9.0302CG	9.0302CH	9.0302CI	9.0302CJ
						9.0302DG	9.0302DH	9.0302DI	

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MICRON		LOJ	BHODS
COMMUNICATIONS, INC.		Temperature Compensated	
INTEGRATED CIRCUIT DESIGN		Current Generator	
CONFIDENTIAL INFORMATION		10/rev/bs_cir	86
		Oct 26 11:11:48 1991	

82: created buffered VREF
 86: disconnect temp compensation

FIG. 9.0302

9.0303AA 9.0303AB 9.0303AC 9.0303AD 9.0303AE 9.0303AF

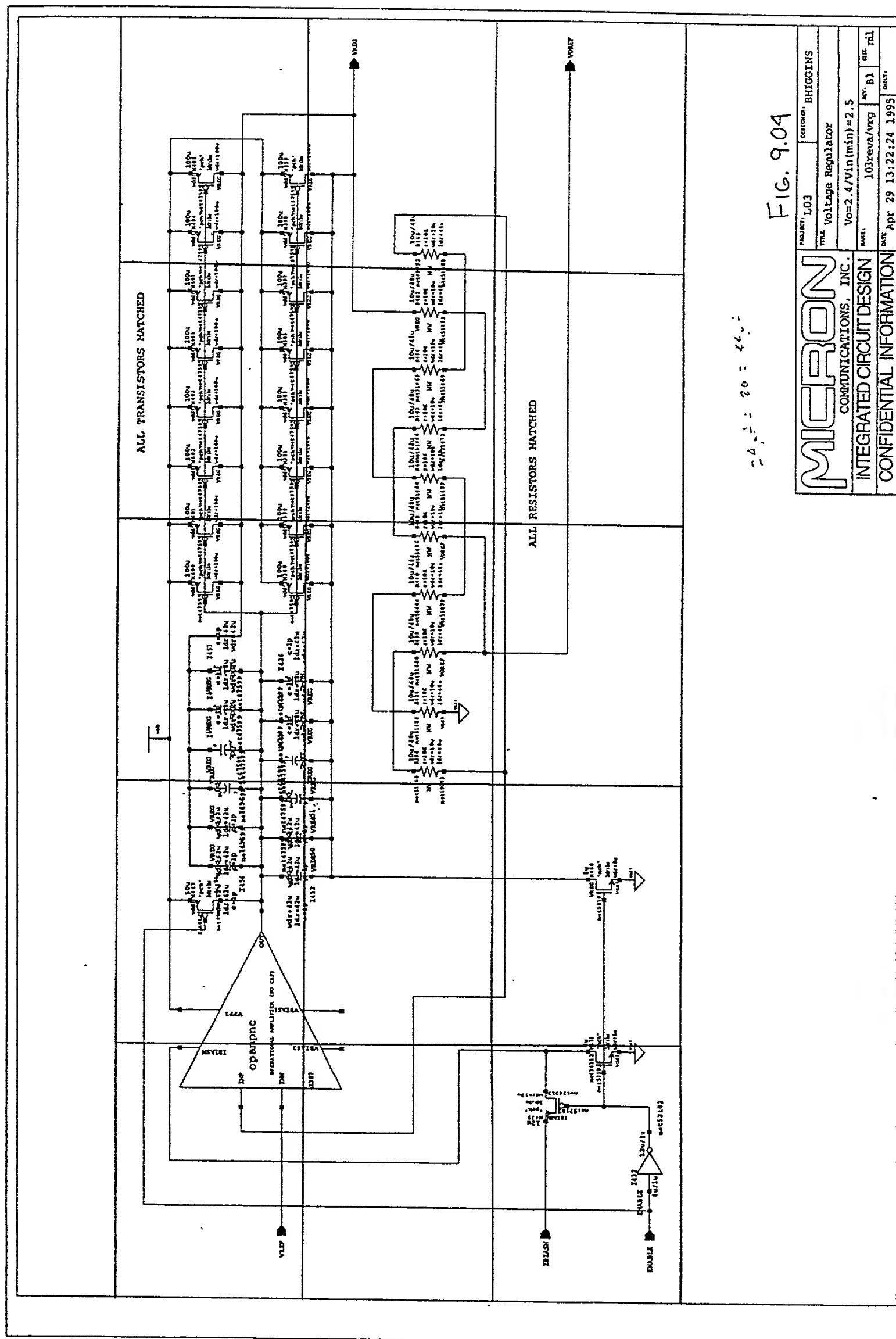
MI40-030

9.0303AA	9.0303AB	9.0303AC	9.0303AD	9.0303AE	9.0303AF
9.0303BA	9.0303BB	9.0303BC	9.0303BD	9.0303BE	9.0303BF
	9.0303CB	9.0303CC	9.0303CD	9.0303CE	9.0303CF

II II III IIII

9.04AA	9.04AB	9.04AC	9.04AD	9.04AE
9.04BA	9.04BB	9.04BC	9.04BD	9.04BE
9.04CA	9.04CB	9.04CC	9.04CD	9.04CE

II II III



9.05AA	9.05AB	9.05AC	9.05AD	9.05AE
9.05BA	9.05BB	9.05BC	9.05BD	9.05BE
9.05CA	9.05CB	9.05CC	9.05CD	9.05CE
9.05DA	9.05DB	9.05DC	9.05DD	9.05DE
9.05EA	9.05EB	9.05EC	9.05ED	9.05EE
9.05FA	9.05FB	9.05FC	9.05FD	9.05FE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

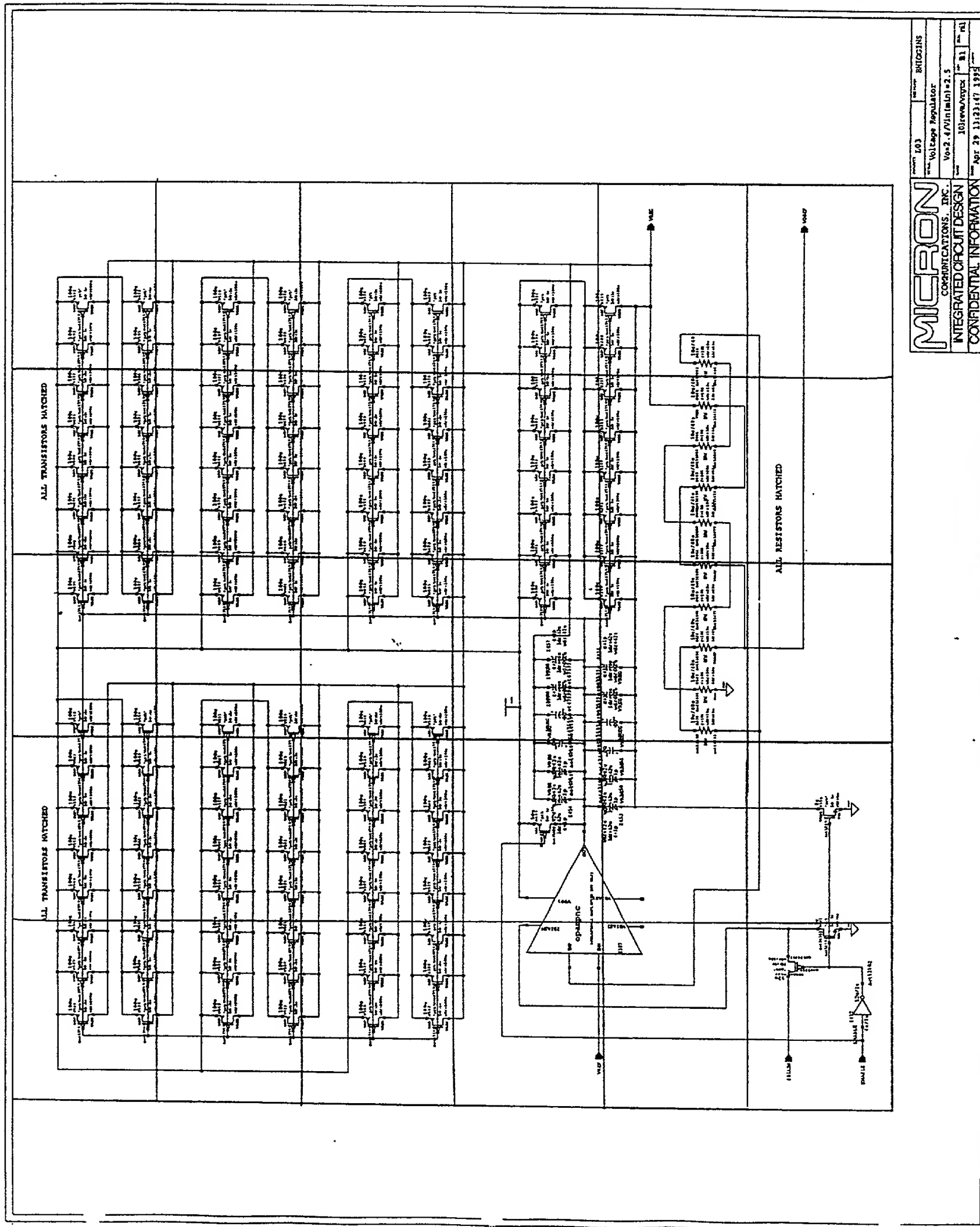
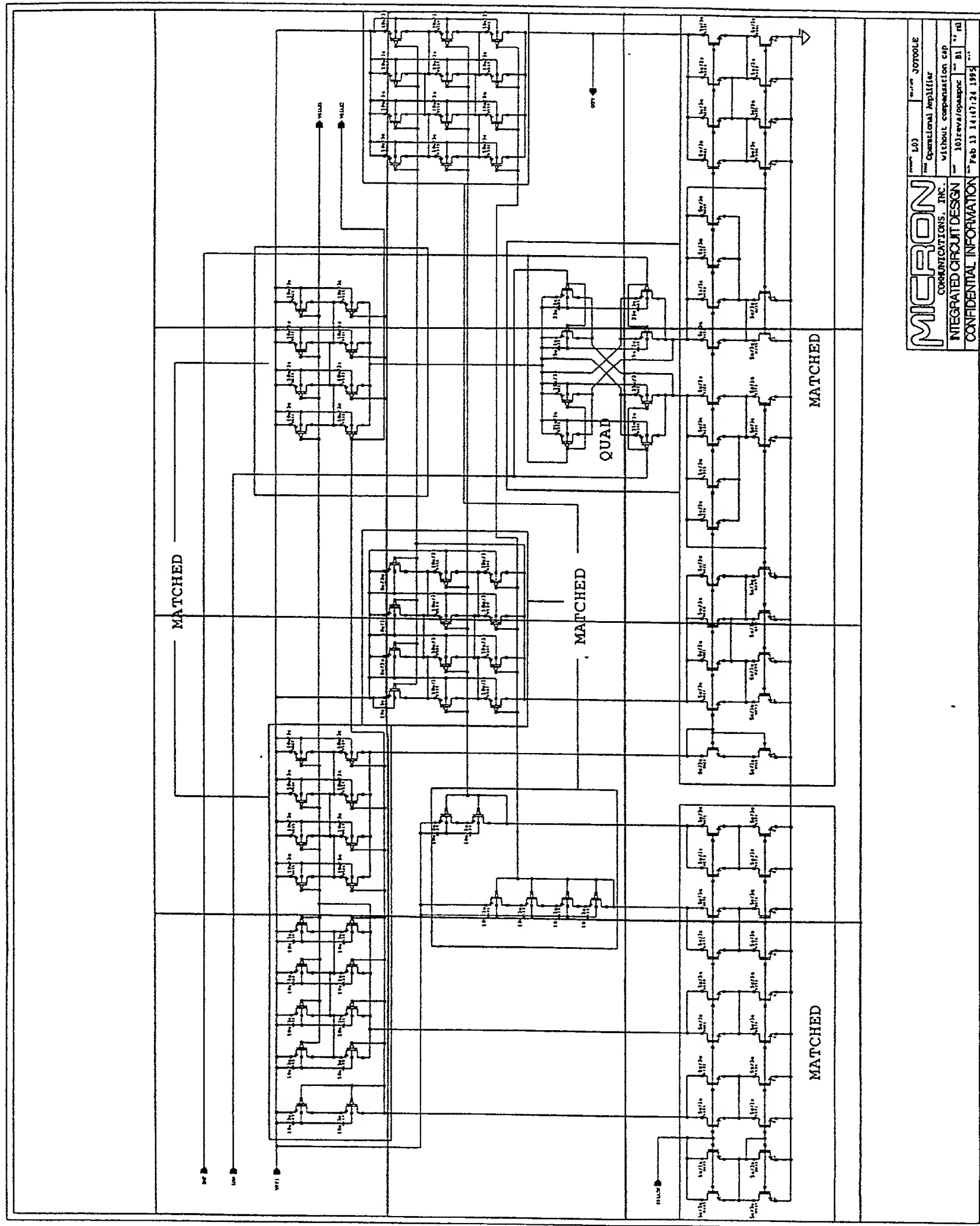


Fig. 9.05

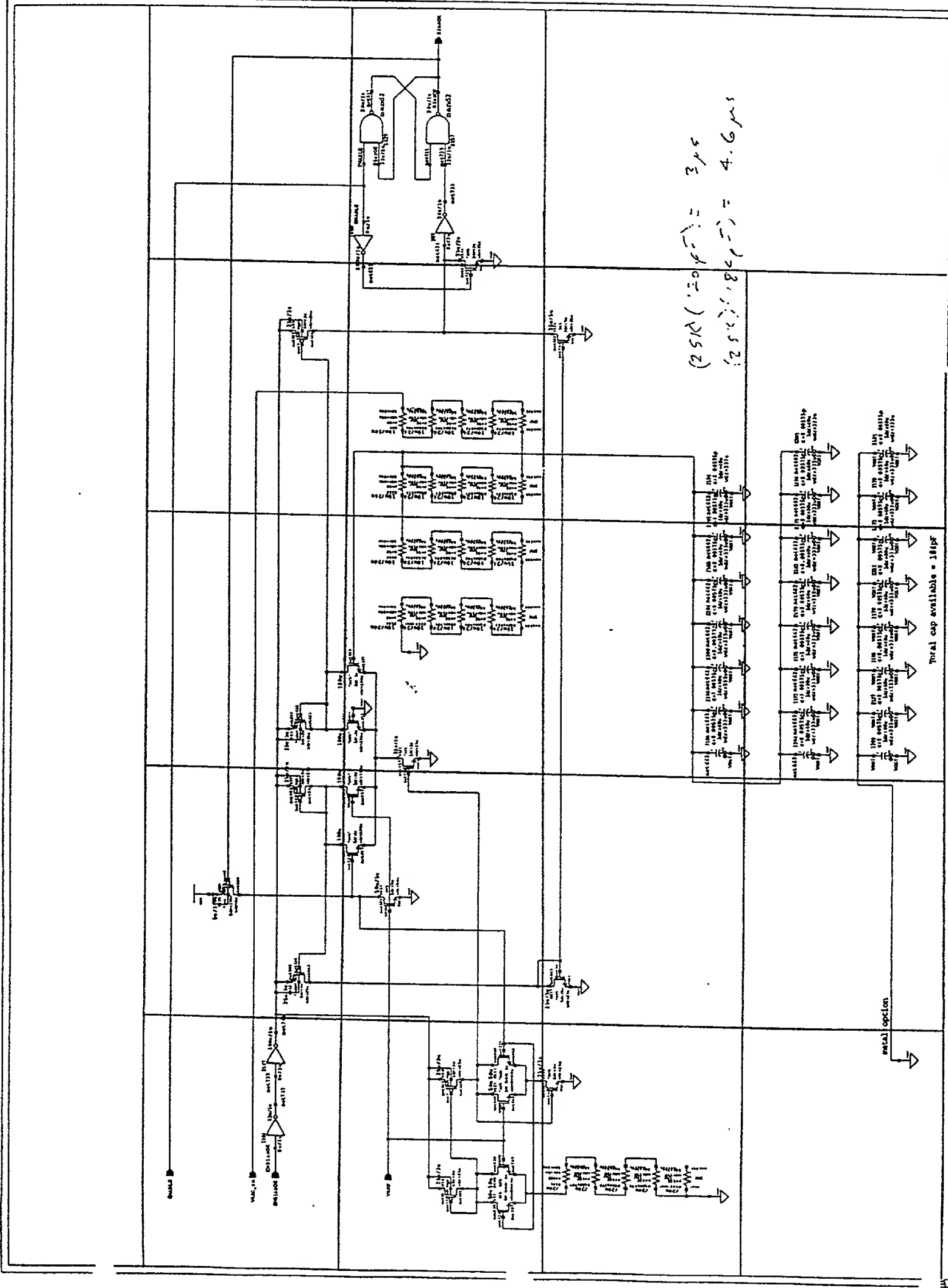
9.0501AA	9.0501AB	9.0501AC	9.0501AD
9.0501BA	9.0501BB	9.0501BC	9.0501BD
9.0501CA	9.0501CB	9.0501CC	9.0501CD

Year	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	



9.06AA	9.06AB	9.06AC	9.06AD	9.06AE
9.06BA	9.06BB	9.06BC	9.06BD	9.06BE
9.06CA	9.06CB	9.06CC	9.06CD	
9.06DA	9.06DB	9.06DC	9.06DD	

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MICRON COMMUNICATIONS, INC.
 INTEGRATED CIRCUIT DESIGN
 CONFIDENTIAL INFORMATION
 L01
 B15 OK Detector
 1010000/010000
 Jul 28 10:23:35 1993

B2: added caps from ballopfiler
 added logic to shut off current

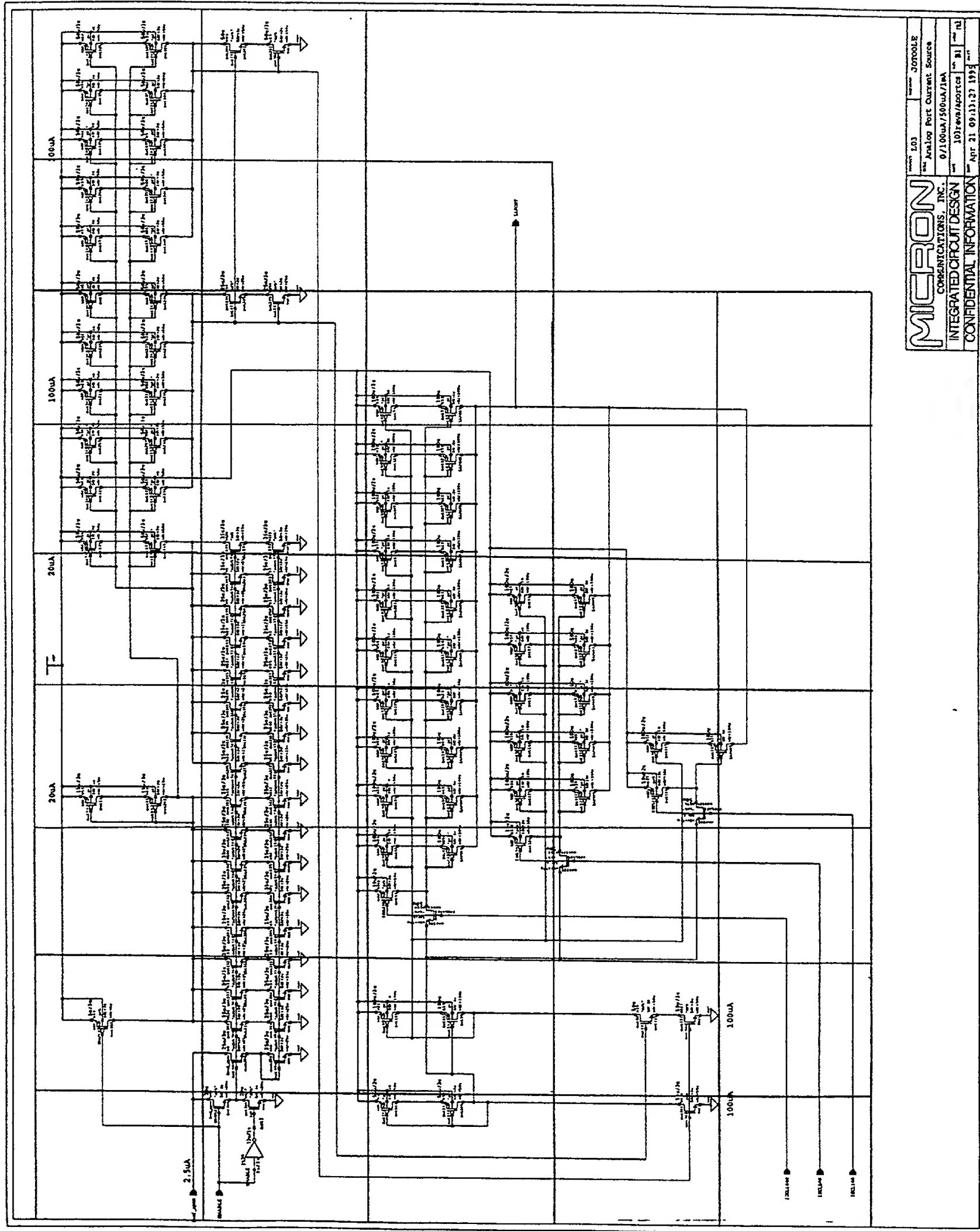
Thral cap available = 18pF

metal option

FIG. 9.06

9.07AA	9.07AB	9.07AC	9.07AD	9.07AE	9.07AF	9.07AG	9.07AH	9.07AI
9.07BA	9.07BB	9.07BC	9.07BD	9.07BE	9.07BF	9.07BG	9.07BH	9.07BI
9.07CA	9.07CB	9.07CC	9.07CD	9.07CE	9.07CF	9.07CG	9.07CH	
9.07DA	9.07DB	9.07DC	9.07DD	9.07DE	9.07DF	9.07DG		
9.07EA	9.07EB	9.07EC	9.07ED	9.07EE	9.07EF	9.07EG		

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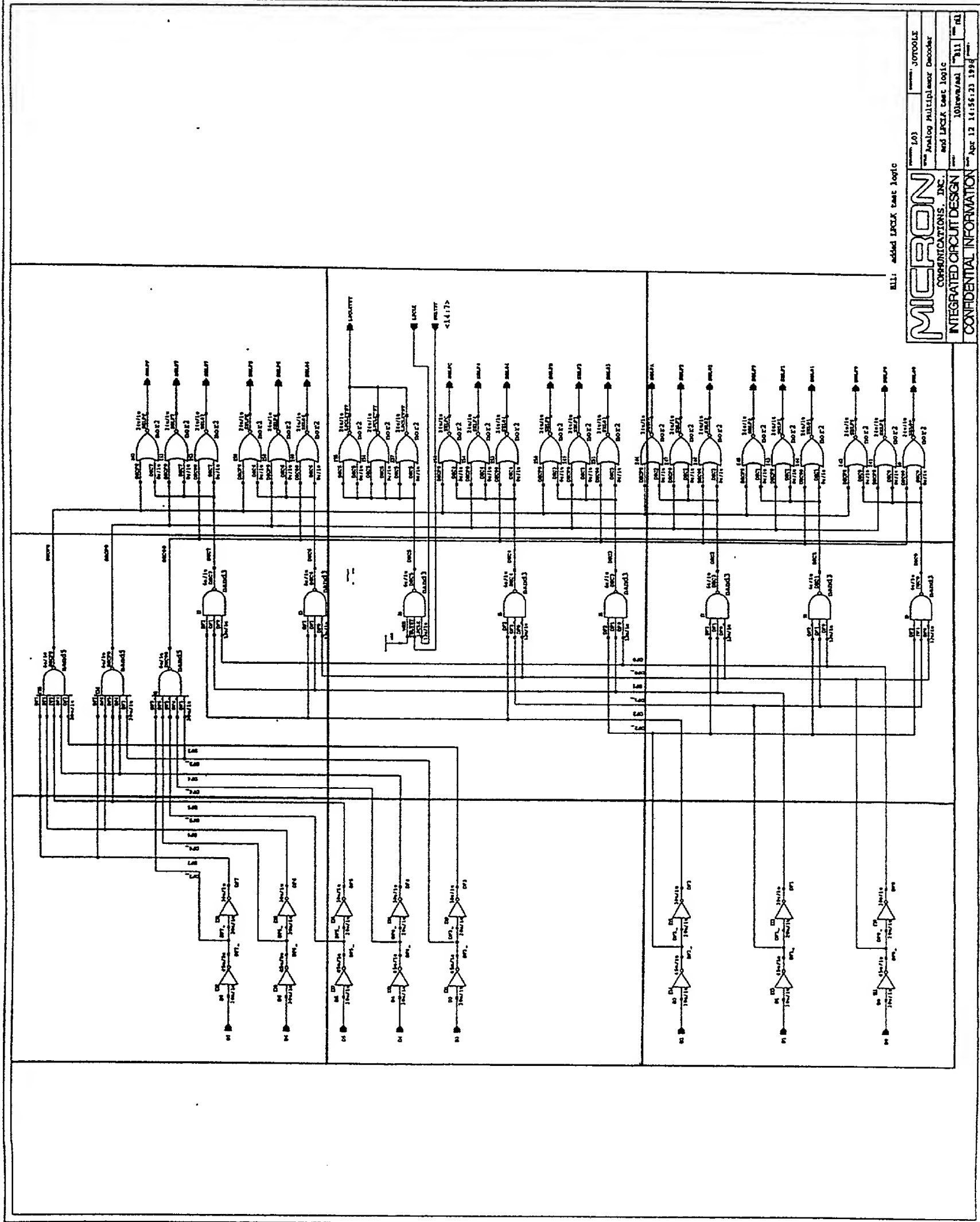


MICRON		30 PIN	300000
COMMUNICATIONS, INC.		Analog Port Current Source	
INTEGRATED CIRCUIT DESIGN		0.100uA/500uA/10uA	
CONFIDENTIAL INFORMATION		101rev/a/portca	
		Apr 21 09:11:27 1975	

Fig. 9.07

9.08AA	9.08AB	9.08AC
9.08BA	9.08BB	9.08BC
9.08CA	9.08CB	9.08CC

100% test coverage achieved for all logic functions in this design.

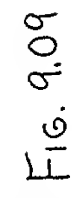


ELL: added LPOX test logic

MICRON		LOG	JTAG00LE
COMMUNICATIONS, INC.		Analog Multiplexer Decoder and LPOX test Logic	
INTEGRATED CIRCUIT DESIGN		10/19/94	ELL
CONFIDENTIAL INFORMATION		Apr 12 14:56:23 1994	

Fig. 9.08

9.09AA	9.09AB
9.09BA	9.09BB



9.0901AA 9.0901AB 9.0901AC 9.0901AD 9.0901AE 9.0901AF 9.0901AG 9.0901AH

9.0901BA 9.0901BB 9.0901BC 9.0901BD 9.0901BE 9.0901BF 9.0901BG 9.0901BH

9.0901CA 9.0901CB 9.0901CC 9.0901CD 9.0901CE 9.0901CF 9.0901CG 9.0901CH

MI40-030

9.0901AA	9.0901AB	9.0901AC	9.0901AD	9.0901AE	9.0901AF	9.0901AG	9.0901AH
9.0901BA	9.0901BB	9.0901BC	9.0901BD	9.0901BE	9.0901BF	9.0901BG	9.0901BH
9.0901CA	9.0901CB	9.0901CC	9.0901CD	9.0901CE	9.0901CF	9.0901CG	9.0901CH

II II III IIII

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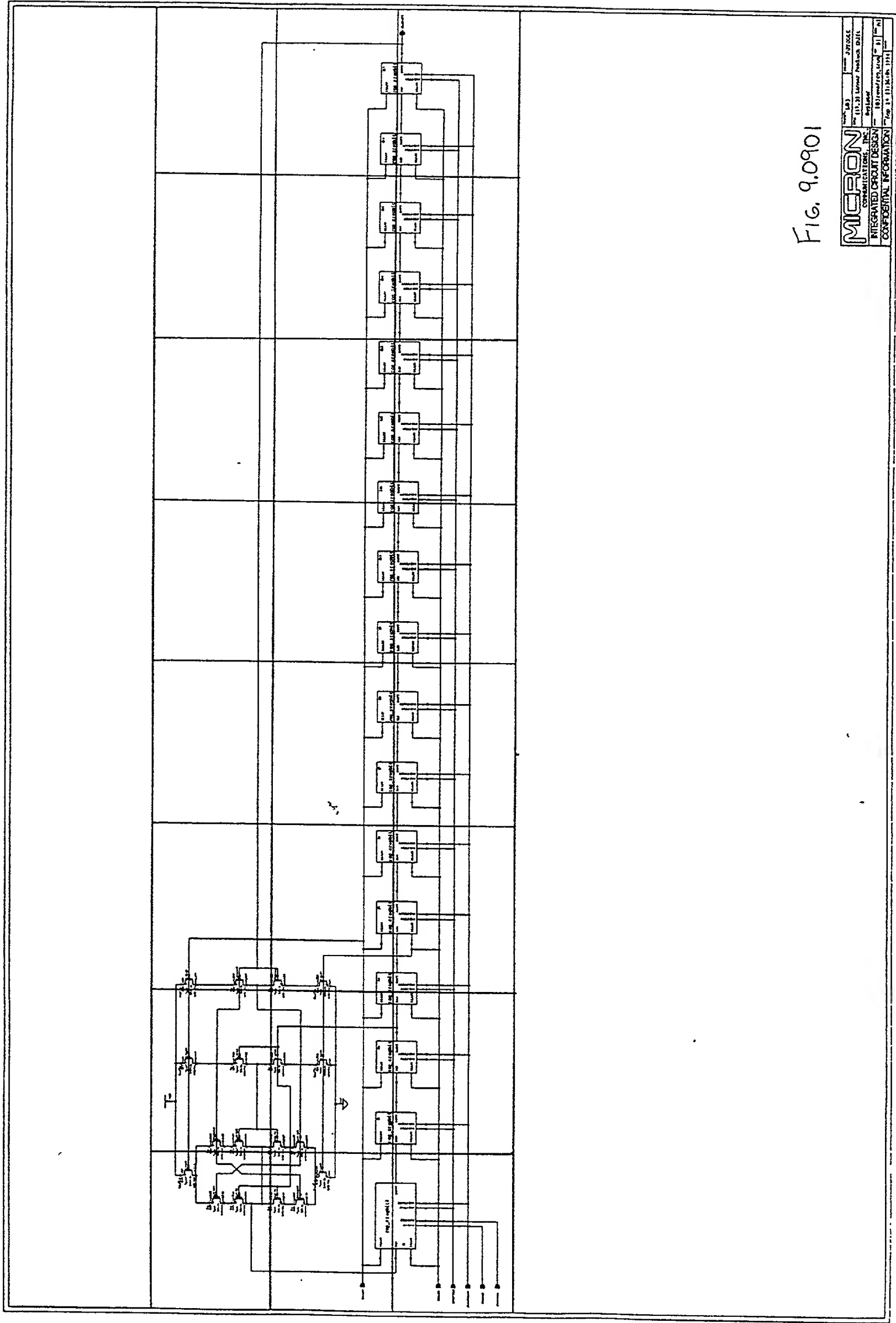


FIG. 9.0901

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
Doc. No.	9.0901
Rev.	1.0
Date	10/10/70
By	J. J. [illegible]
For	111-21 Lunar Module Data

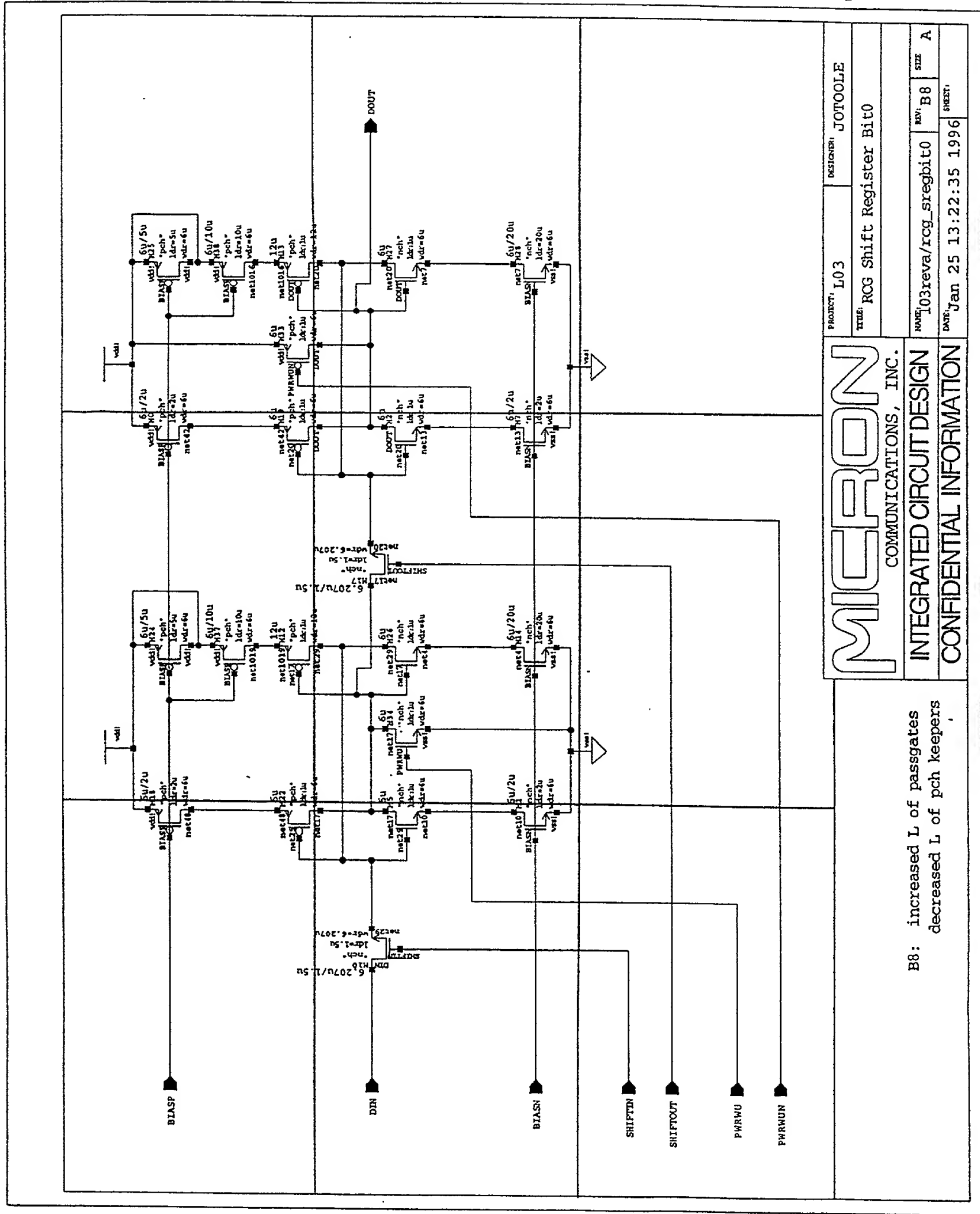
9.090101AA 9.090101AB 9.090101AC 9.090101BA 9.090101BB 9.090101CB 9.090101CA 9.090101CC

MI40-030

9.090101AA	9.090101AB	9.090101AC
9.090101BA	9.090101BB	9.090101BC
9.090101CA	9.090101CB	9.090101CC

II II II II II II II II

THIS DOCUMENT IS UNCLASSIFIED
DATE 08-01-2001 BY 60322 UCBAW/BJS



PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: RC Shift Register Bit0			
NAME: l03rev0/rcg_sregbit0		REV: B8	SIZE: A
DATE: Jan 25 13:22:35 1996		SHEET: 1	

MICRON
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

B8: increased L of passgates
decreased L of pch keepers

FIG. 9.090101

9.090102AA	9.090102AB
9.090102BA	9.090102BB

9.090102

THIS DOCUMENT IS UNCLASSIFIED
DATE 08-01-2001 BY 60322 UCBAW/BJS/STP

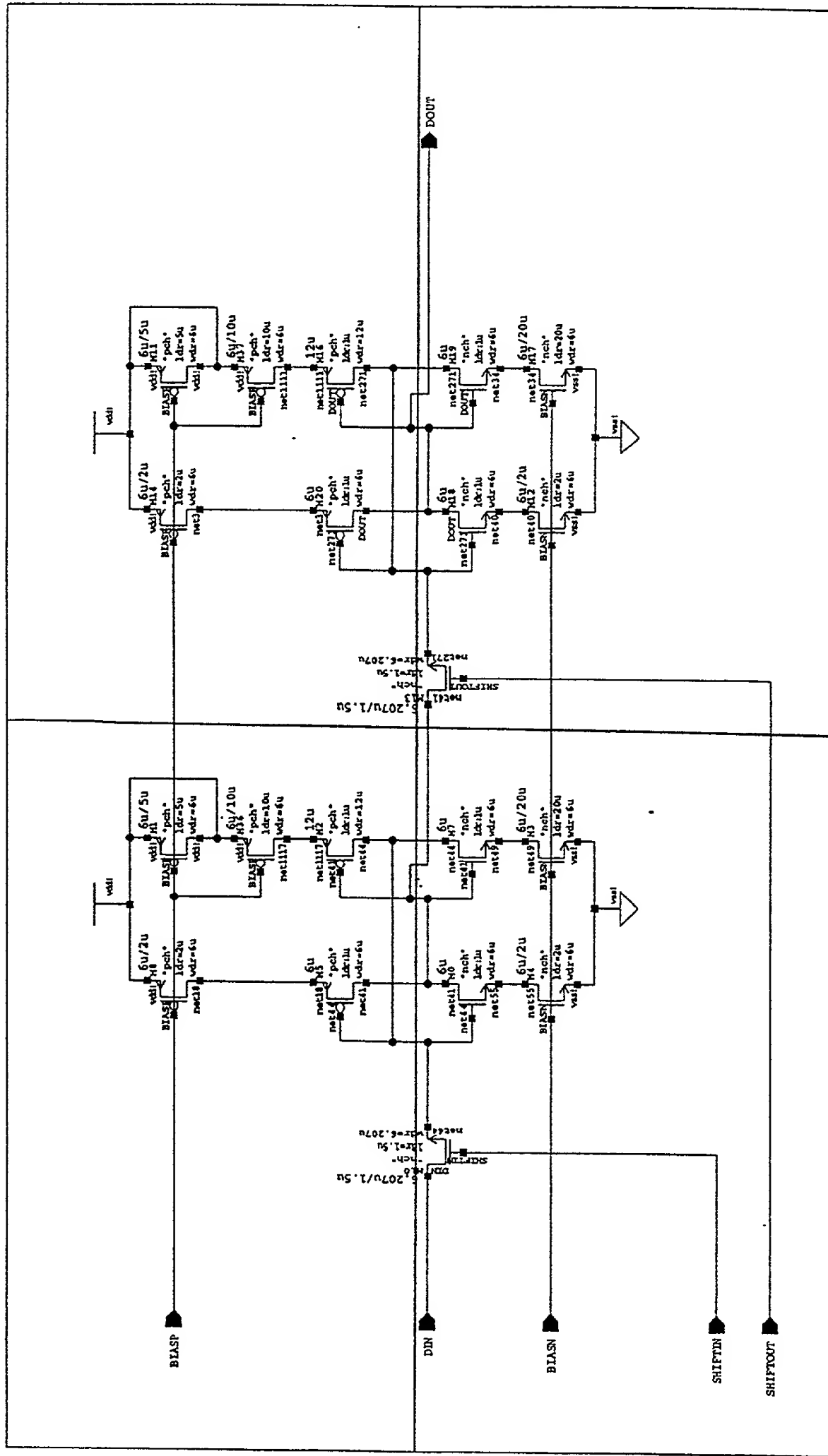


Fig. 9,090102

MICRON			PROJECT: L03		DESIGNER: JOTOOLE			
COMMUNICATIONS, INC.			TITLE: ROG Shift Register Bit					
INTEGRATED CIRCUIT DESIGN			NAME: 103reva/rog_sregbit		REV: B8		SIZE: A	
CONFIDENTIAL INFORMATION			DATE: Jan 25 13:25:16 1996		SHEET:			

B8: increased L of passgates
decreased L of pch keepers

9.0902AA	9.0902AB	9.0902AC	9.0902AD	9.0902AE	9.0902F	9.0902AG	9.0902AH	9.0902AI	9.0902AJ	9.0902AK	9.0902AL
9.0902BA	9.0902BB	9.0902BC	9.0902BD	9.0902BE	9.0902F	9.0902BG	9.0902BH	9.0902BI	9.0902BJ	9.0902BK	9.0902BL
		9.0902CC	9.0902CD	9.0902CE	9.0902F	9.0902CG	9.0902CH	9.0902CI	9.0902CJ	9.0902CK	9.0902CL
		9.0902DC	9.0902DD	9.0902DE	9.0902F						9.0902DL
9.0902EA	9.0902EB	9.0902EC	9.0902ED	9.0902EE	9.0902F	9.0902EG	9.0902EH	9.0902EI	9.0902EJ	9.0902EK	9.0902EL
					9.0902F	9.0902FG	9.0902FH	9.0902FI	9.0902FJ	9.0902FK	9.0902FL

9.0903AA	9.0903AB	9.0903AC
9.0903BA	9.0903BB	9.0903BC
9.0903CA	9.0903CB	9.0903CC

EX-9000

CONFIDENTIAL INFORMATION

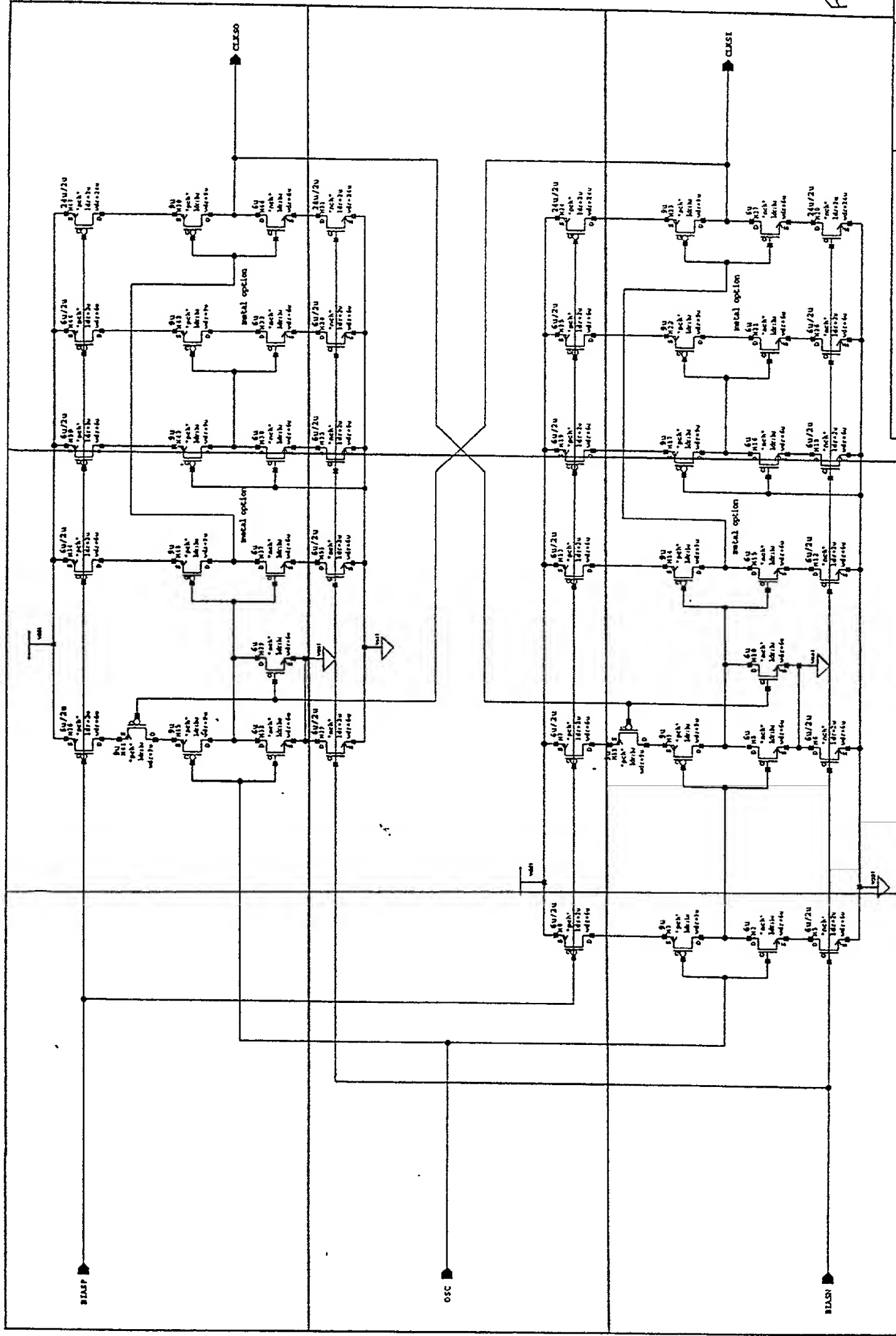


Fig. 9.0903

MICRON
COMMUNICATIONS, INC.

PROJECT: L03

DESCRIPTION: J0700LE
Title: Clock Generator

INTEGRATED CIRCUIT DESIGN

DATE: 103revA/rcg_clkgen

REV: B8

FILE: ml

CONFIDENTIAL INFORMATION

DATE: Jan 24 09:56:43 1996

B8: wired cross-couples to ground

10AA	10AB	10AC	10AD
10BA	10BB	10BC	10BD
10CA	10CB	10CC	10CD
10DA	10DB	10DC	10DD

II II II II

10.01AA 10.01AB 10.01AC 10.01AD 10.01AE 10.01AF 10.01AG

10.01AA	10.01AB	10.01AC	10.01AD	10.01AE	10.01AF	10.01AG			
10.01BA	10.01BB	10.01BC	10.01BD	10.01BE	10.01BF	10.01BG	10.01BH	10.01BI	10.01BJ
10.01CA	10.01CB	10.01CC	10.01CD	10.01CE	10.01CF	10.01CG	10.01CH	10.01CI	10.01CJ
	10.01DB	10.01DC	10.01DD	10.01DE	10.01DF	10.01DG	10.01DH	10.01DI	10.01DJ

FIG. 10.01

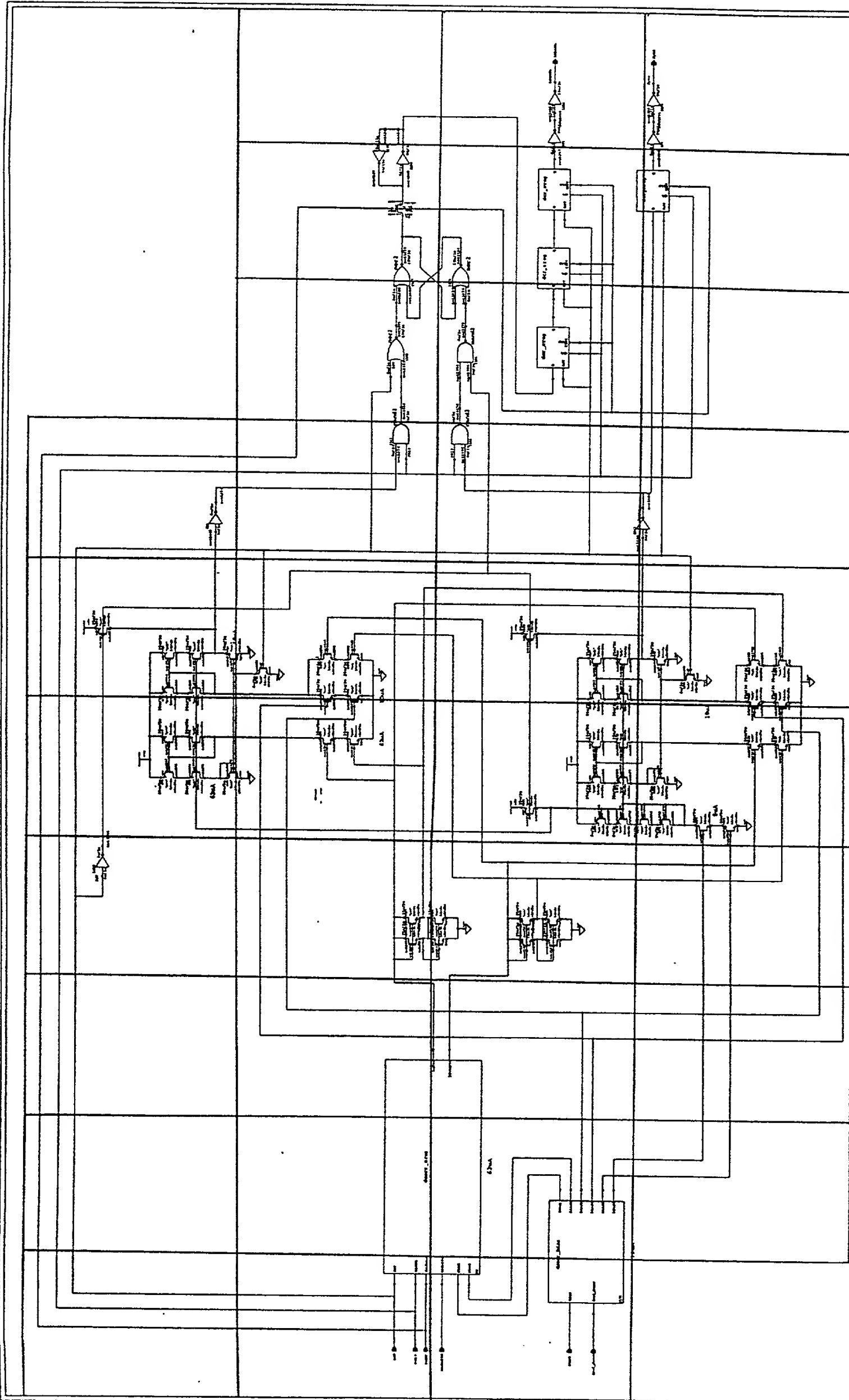


Fig. 10.01

MICRON		10.01	Symbolic
INTEGRATED CIRCUIT DESIGN		10.01	10.01
CONFIDENTIAL INFORMATION		10.01	10.01

10.0101AA	10.0101AB	10.0101AC	10.0101AD	10.0101AE	10.0101AF	10.0101AG
10.0101BA	10.0101BB	10.0101BC	10.0101BD	10.0101BE	10.0101BF	10.0101BG

II II III III III III

CONFIDENTIAL

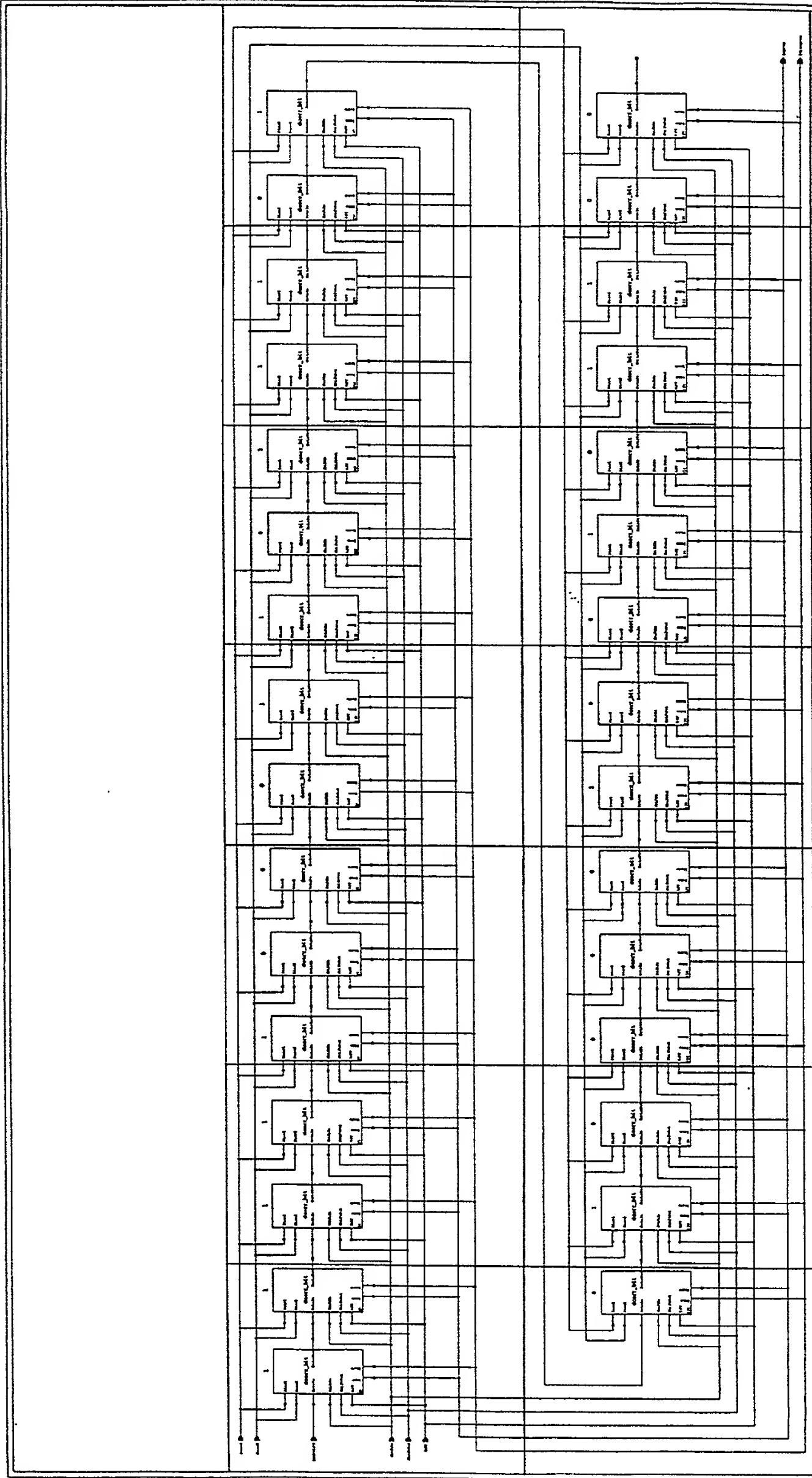


FIG. 10.0101

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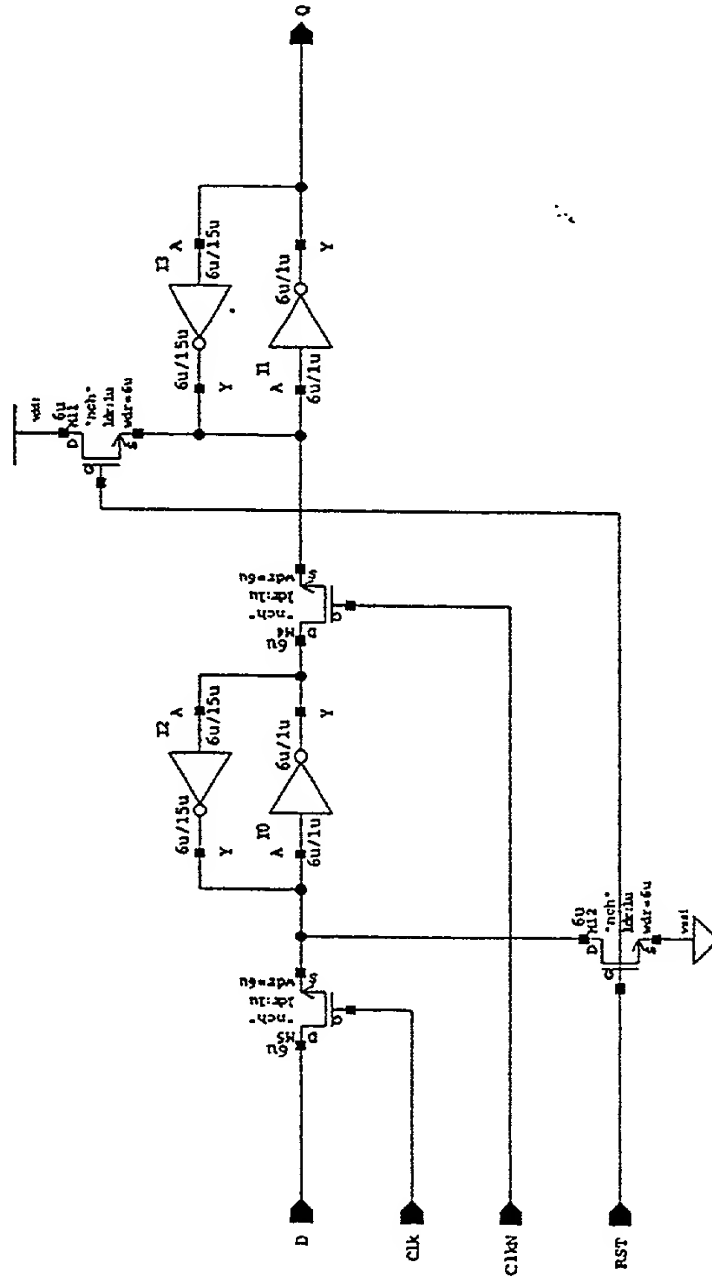


FIG. 10.01010101

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: I03reva/dcorr_sregbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 9 14:08:50 1994	SIZE: A
		SHEET:	

10.01.02

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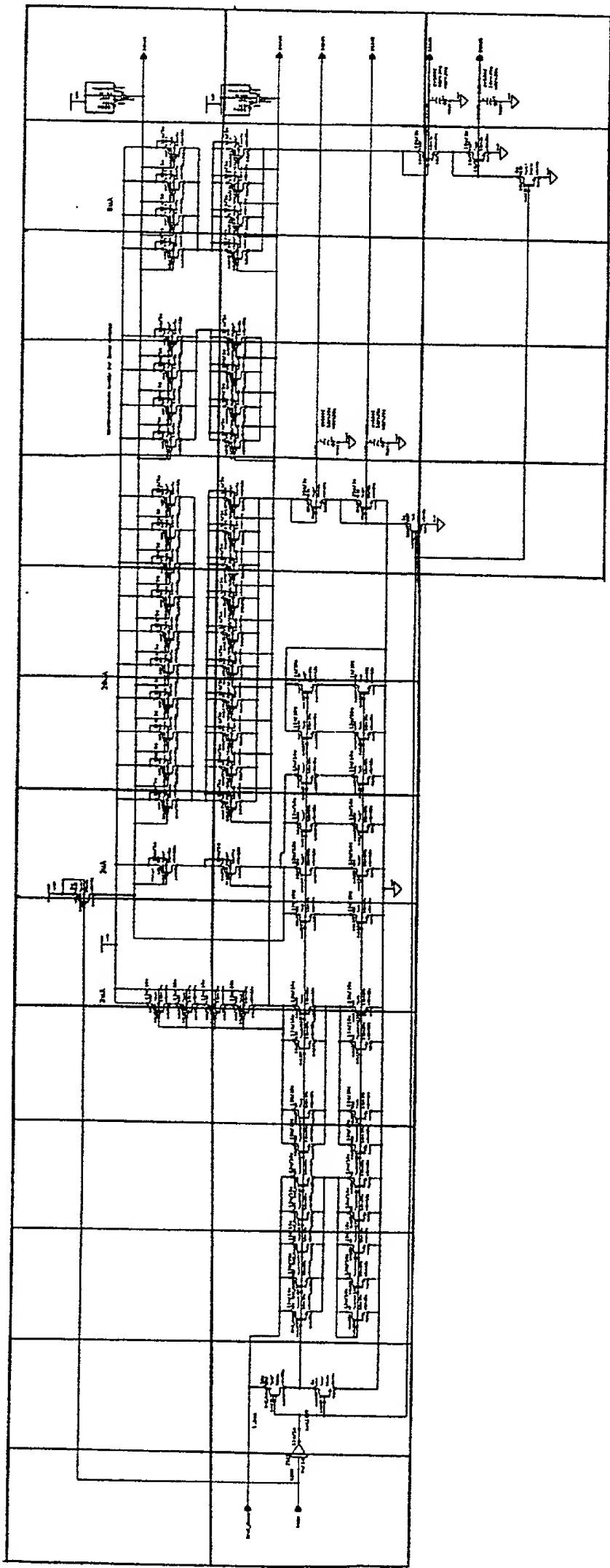


Fig. 10.0102

10.02AA 10.02AB 10.02AC 10.02AD 10.02AE
10.02BA 10.02BB 10.02BC 10.02BD 10.02BE

MI40-030

10.02AA	10.02AB	10.02AC	10.02AD	10.02AE
10.02BA	10.02BB	10.02BC	10.02BD	10.02BE

10.02 10.02

1. The circuit is designed to detect 4 consecutive 0's in a 3-bit counter.
 2. The circuit uses a 3-bit counter (A, B, C) and a 4-bit counter (D, E, F, G).
 3. The 3-bit counter is initialized to 000 and counts up to 111.
 4. The 4-bit counter is initialized to 0000 and counts up to 1111.
 5. The circuit outputs a signal when 4 consecutive 0's are detected.

Detects preamble by counting 4 consecutive 0's

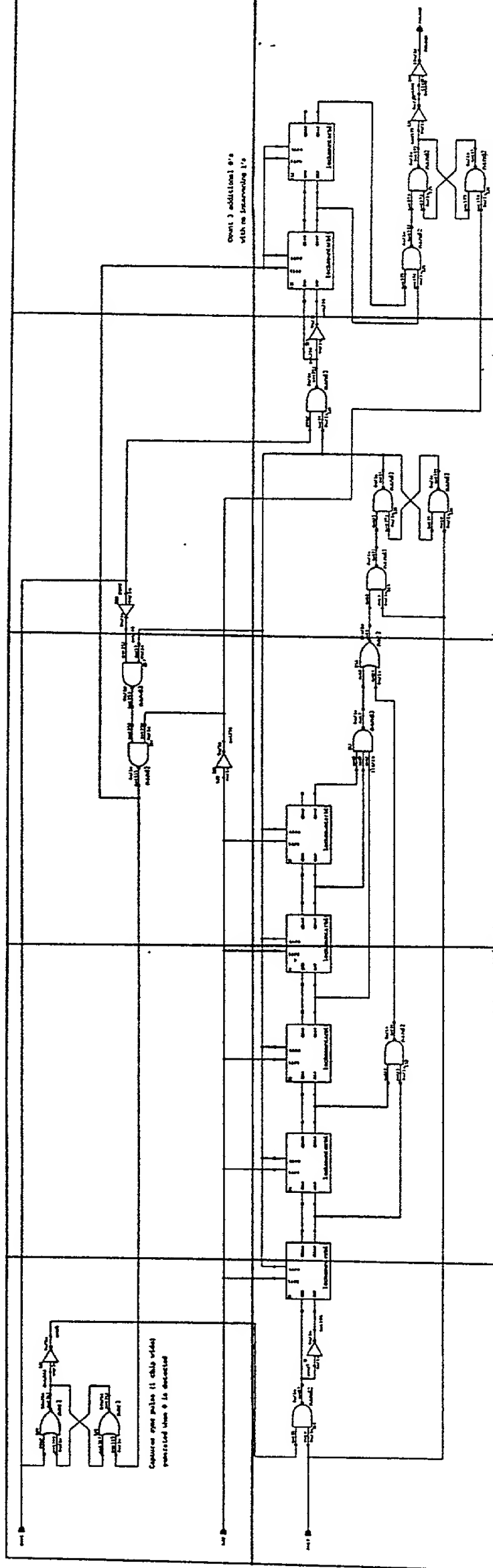
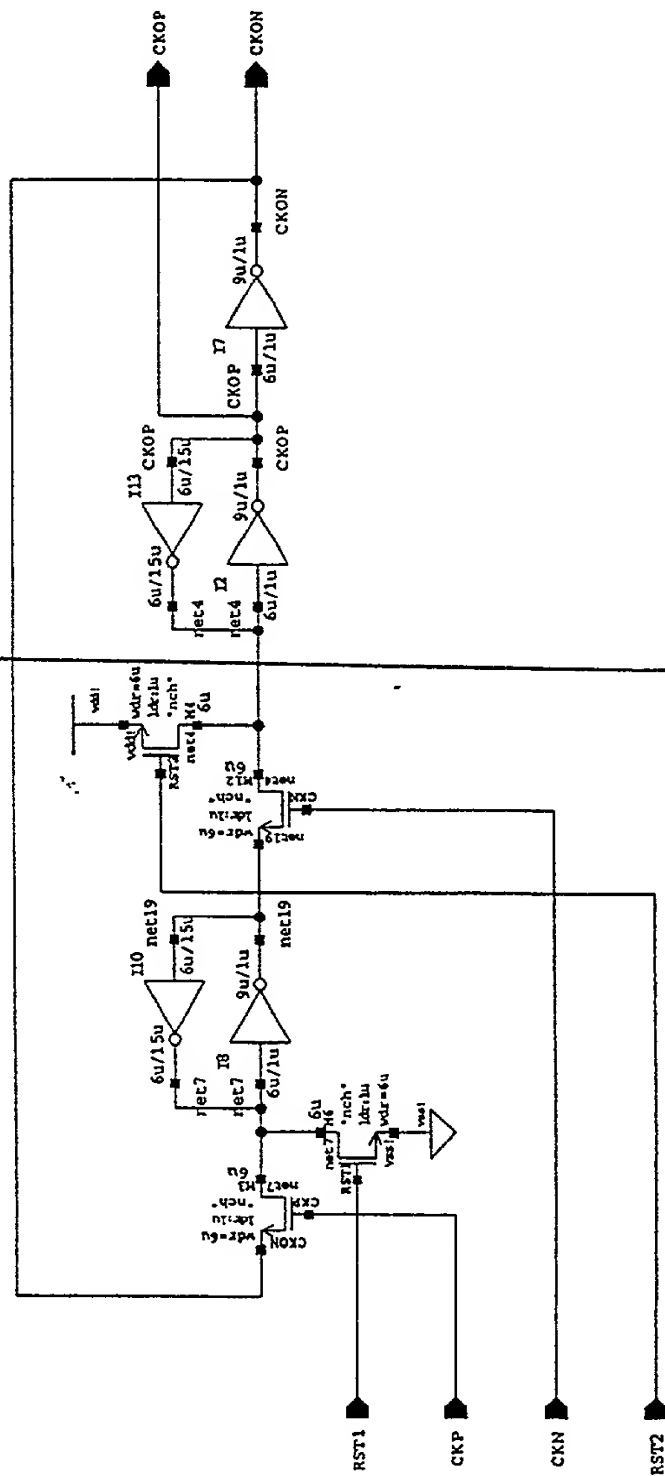


FIG. 10.02

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	



MICRON		PROJECT: L03		DESIGNER: JOTOOLE	
COMMUNICATIONS, INC.		TITLE: PN Lock Detector Counter Bit			
INTEGRATED CIRCUIT DESIGN		NAME: T03reva/lockcounterbit		REV: B1	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Aug 31 14:28:22 1994		SHEET:	

FIG. 10.0201

10.03AB

10.03AA

10.03

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DATE 08-01-2001 BY 60322 UCBAW/BJS

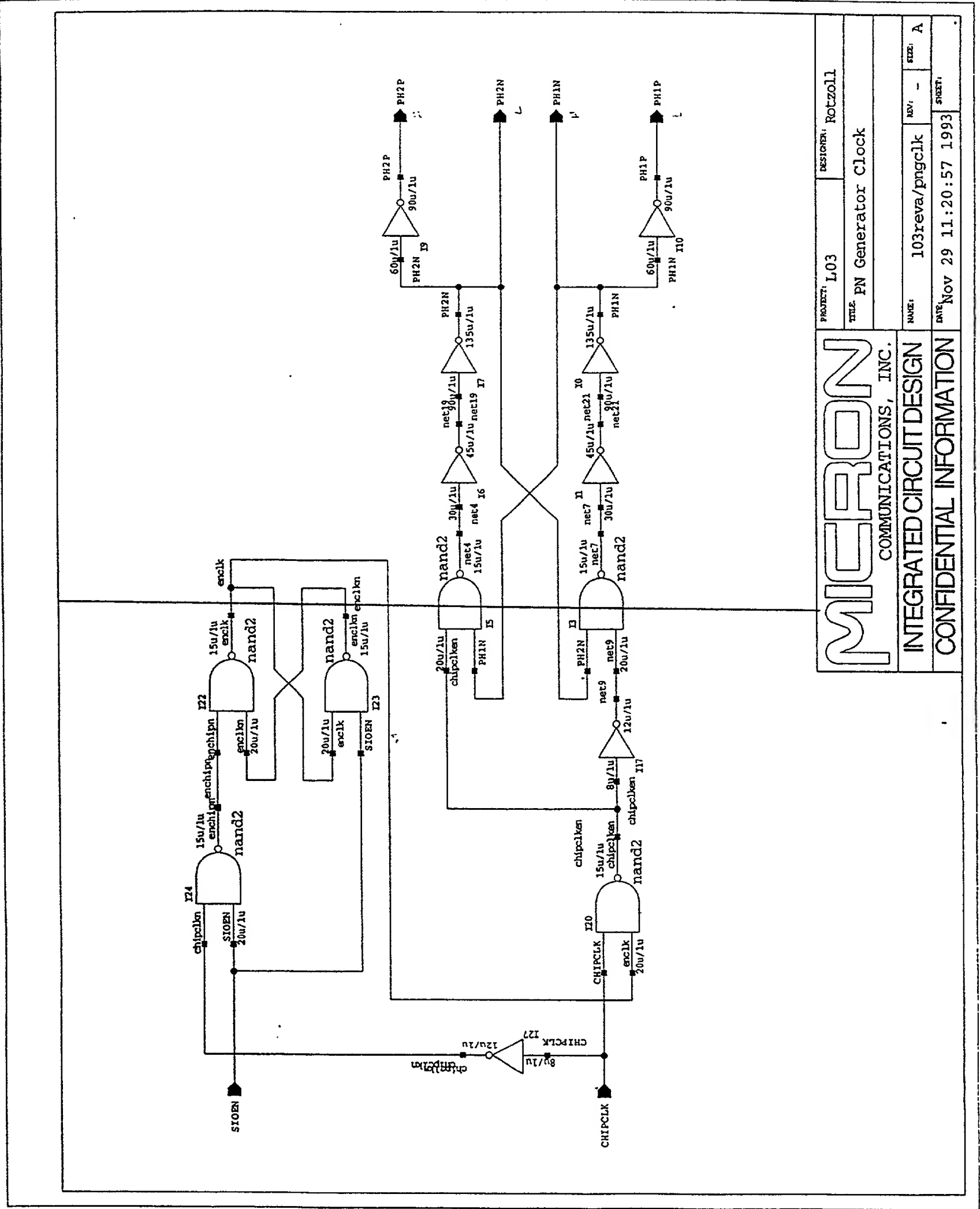


FIG. 10.03

10.04AA	10.04AB	10.04AC	10.04AD	10.04AE
10.04BA	10.04BB	10.04BC	10.04BD	10.04BE
10.04CA	10.04CB	10.04CC	10.04CD	10.04CE

II II III III III

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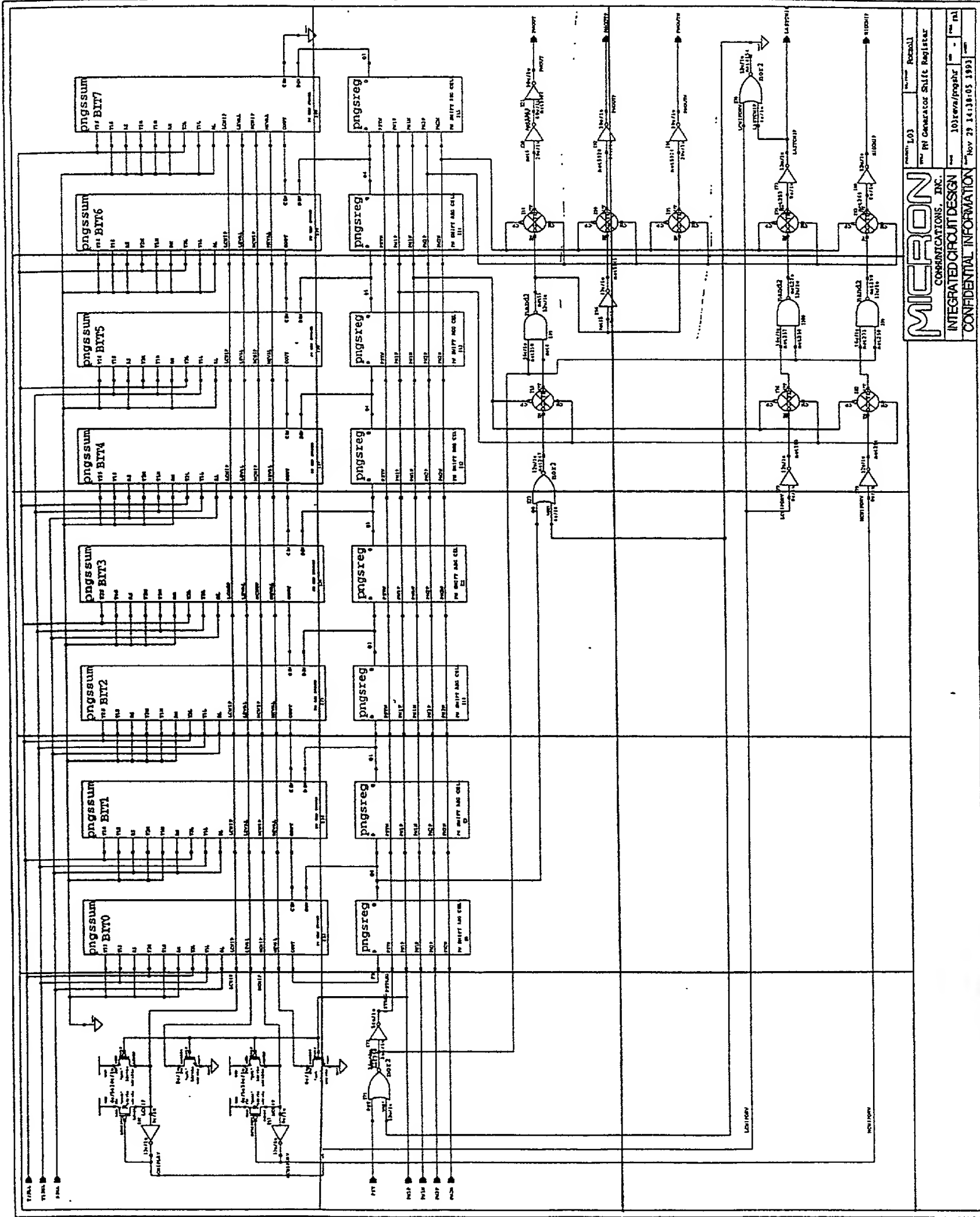
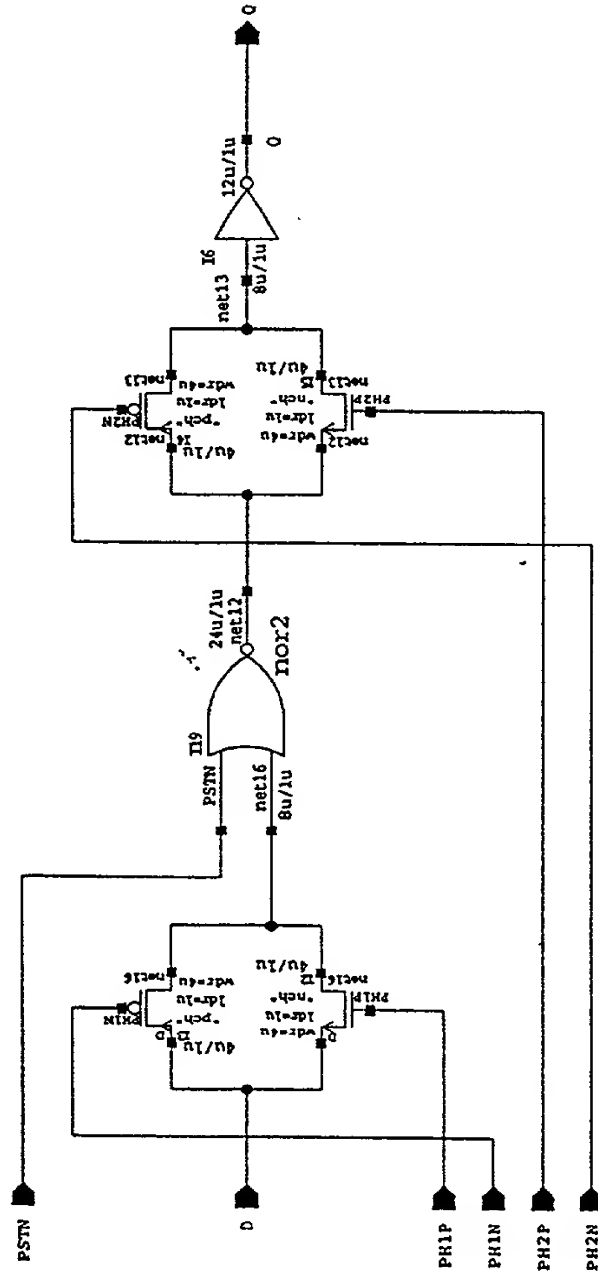


FIG. 10.04

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
Nov 29 14:38:05 1993

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EXCEPT WHERE SHOWN OTHERWISE



MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: PN Generator Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/pngsreg	REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 20 21:22:37 1993	SIZE: A
		SHEET: 1	

Fig. 10.0401

10.0402AA	10.0402AB
10.0402BA	10.0402BB
10.0402CA	10.0402CB

10.0402

三

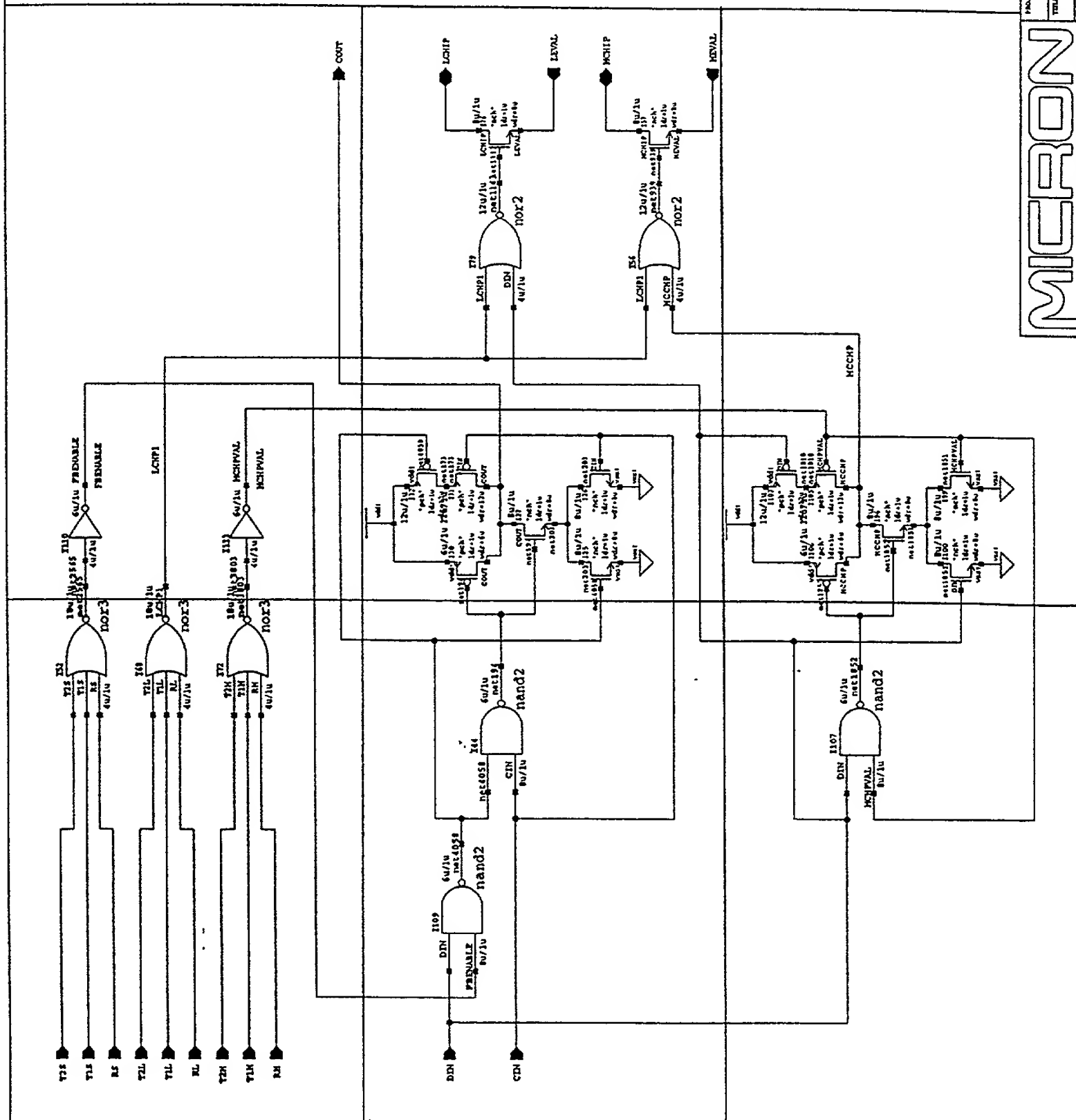
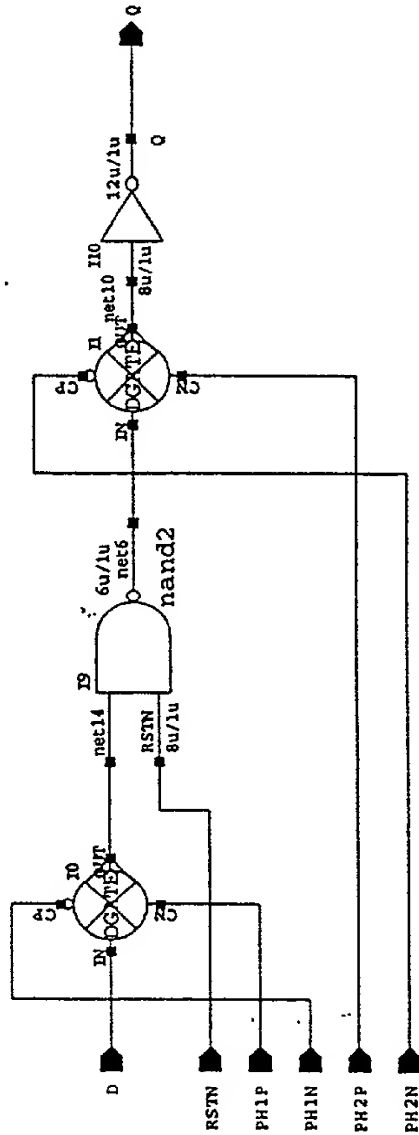


Fig. 10.0402

MICRON		PROJECT: L03		REVISOR: Rotzoll	
COMMUNICATIONS, INC.					
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					
DATE:		103reva/pngssum		REV: -	
DATE:		Nov 20 21:23:00 1993		SHEET:	

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PROJECT: L03	DESIGNER: Rotzoll
TITLE: PN Controller D Flip-Flop	
NAME: 103reva/pnddff	REV: -
DATE: Nov 26 18:12:59 1993	SHEET: A

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Fig. 10.05

10.06AA	10.06AB	10.06AC	10.06AD							
10.06BA	10.06BB	10.06BC	10.06BD	10.06BE	10.06BF	10.06BG	10.06BH	10.06BI	10.06BJ	10.06BK
10.06CA	10.06CB	10.06CC	10.06CD	10.06CE	10.06CF	10.06CG	10.06CH	10.06CI	10.06CJ	10.06CK
10.06DA	10.06DB	10.06DC	10.06DD	10.06DE	10.06DF	10.06DG	10.06DH			

CONFIDENTIAL AND PROPRIETARY INFORMATION

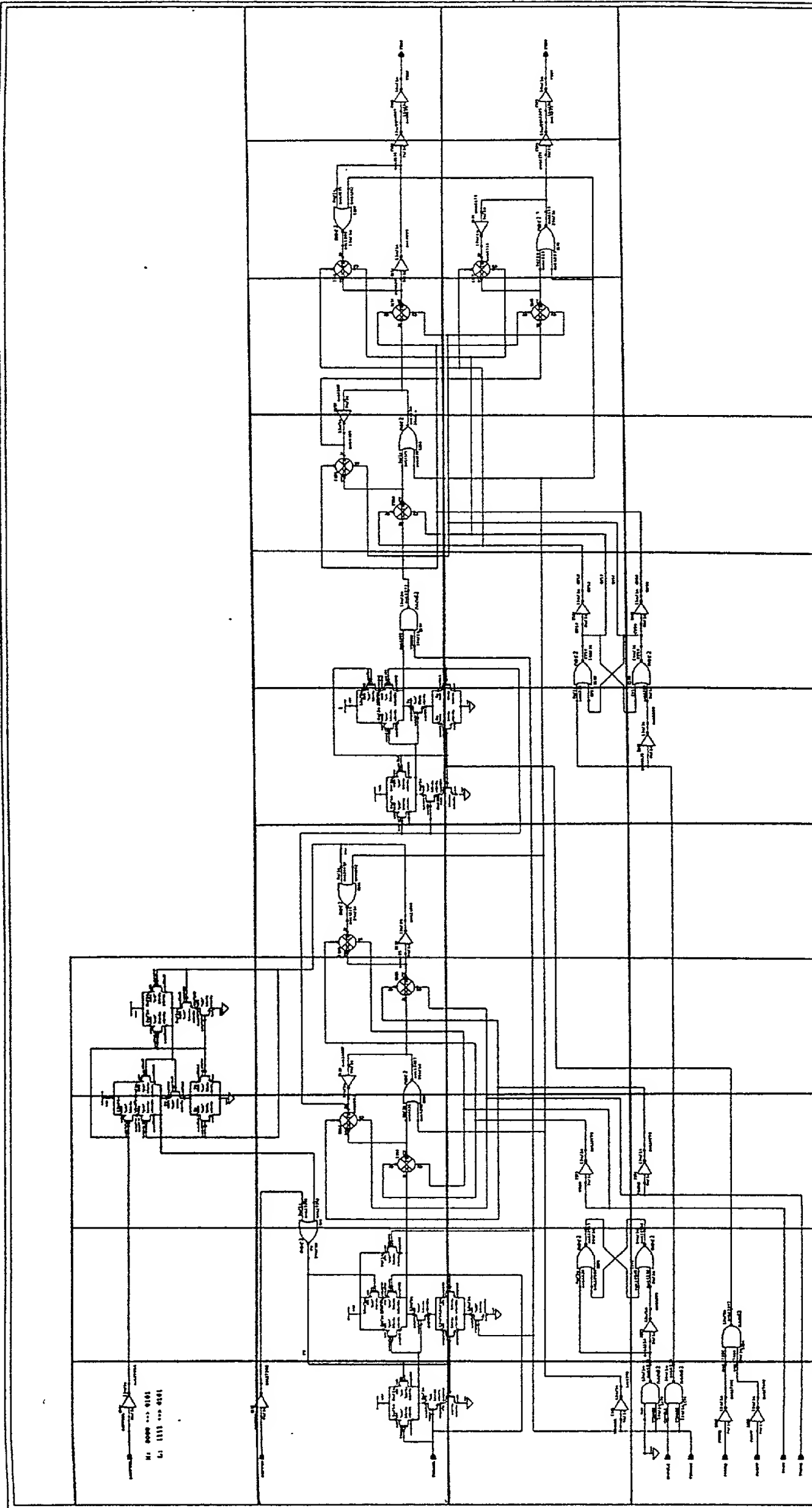


Fig. 10.06

811. Example of a microprocessor circuit with 100 gates

MICRON		JOYCE
INTEGRATED CIRCUIT DESIGN		DIFFERENTIAL AND DE BRUIN
CONFIDENTIAL INFORMATION		11-11-1974

10.07AA	10.07AB	10.07AC	10.07AD
10.07BA	10.07BB	10.07BC	10.07BD
10.07CA	10.07CB	10.07CC	10.07CD

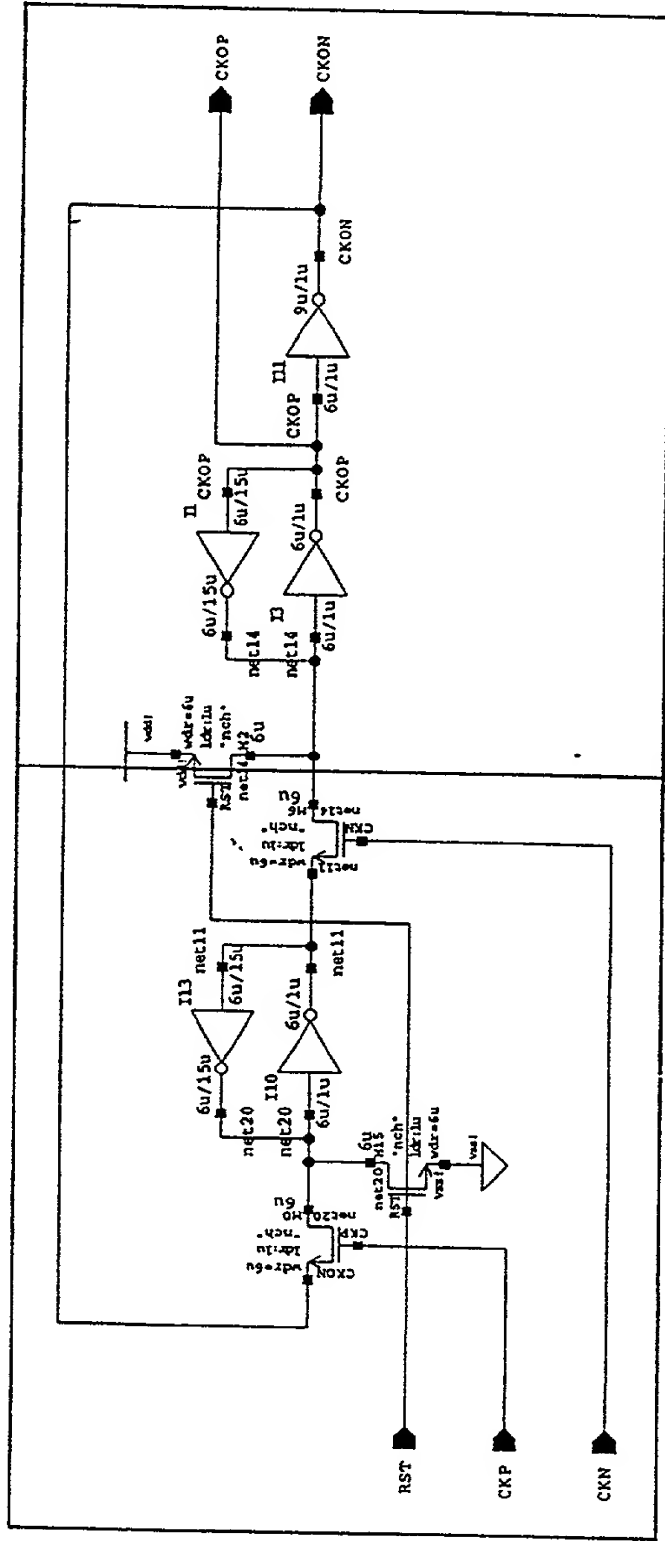
II. II. II. II. II

10.0701AB

10.0701AA

10.0701AB

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MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: FSK Counter Bit	
INTEGRATED CIRCUIT DESIGN		Same as wuabot_cbit	
CONFIDENTIAL INFORMATION		NAME: 103reva/fskcbit	REV: B1
		DATE: Apr 17 15:42:44 1995	SIZE: A
		SHEET:	

Fig. 10.0701

11AB

11AA

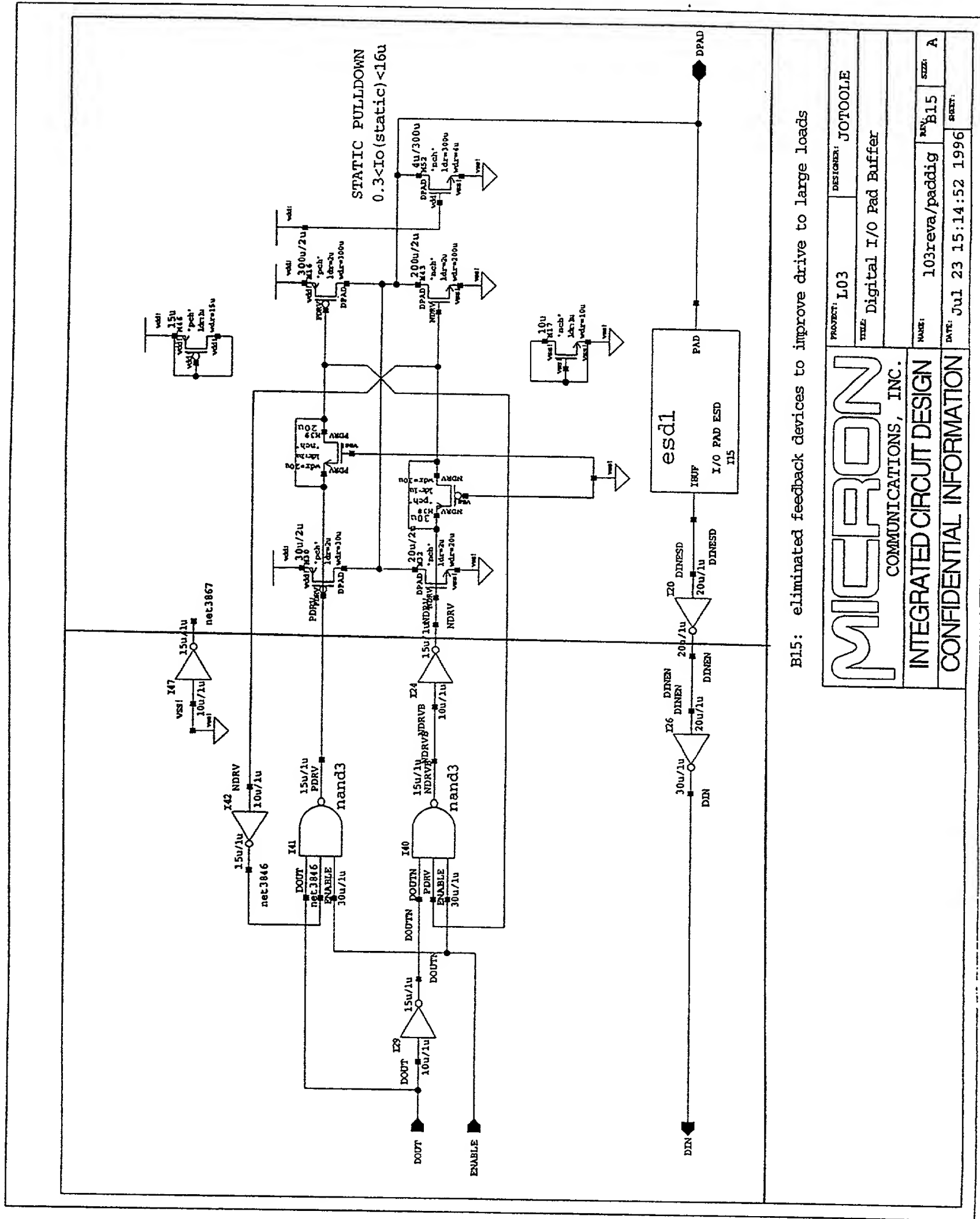
11 11

12AB

12AA

$$\frac{\mathbb{Z}[\frac{1}{2}]}{\mathbb{Z}[\frac{1}{2}]/\mathbb{Z}}$$

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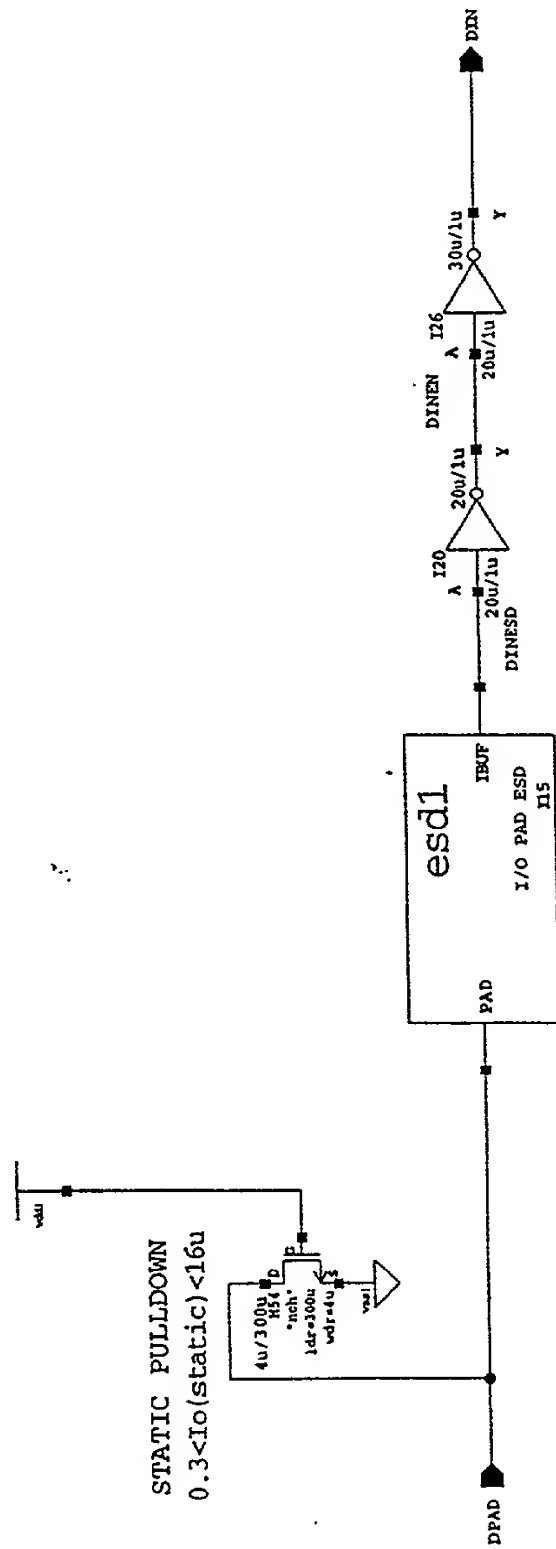


B15: eliminated feedback devices to improve drive to large loads

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital I/O Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/padding	REV: B15
CONFIDENTIAL INFORMATION		DATE: Jul 23 15:14:52 1996	SIZE: A

Fig 12AA-AB

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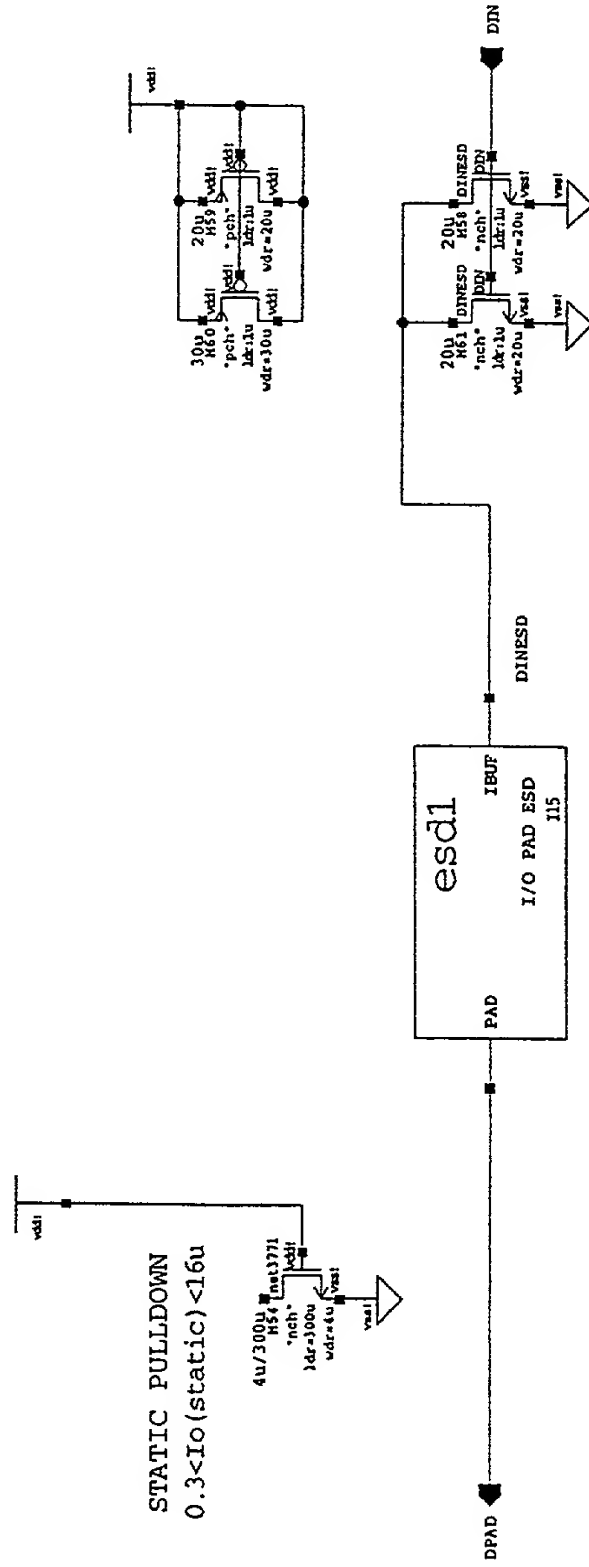


STATIC PULLDOWN
0.3<Io(static)<16u

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital Input Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/paddigin	REV: B1
CONFIDENTIAL INFORMATION		DATE: Apr 11 11:10:35 1995	SIZE: A

FIG. 13

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DATE 08-01-2001 BY 60322 UCBAW/BJS/STP

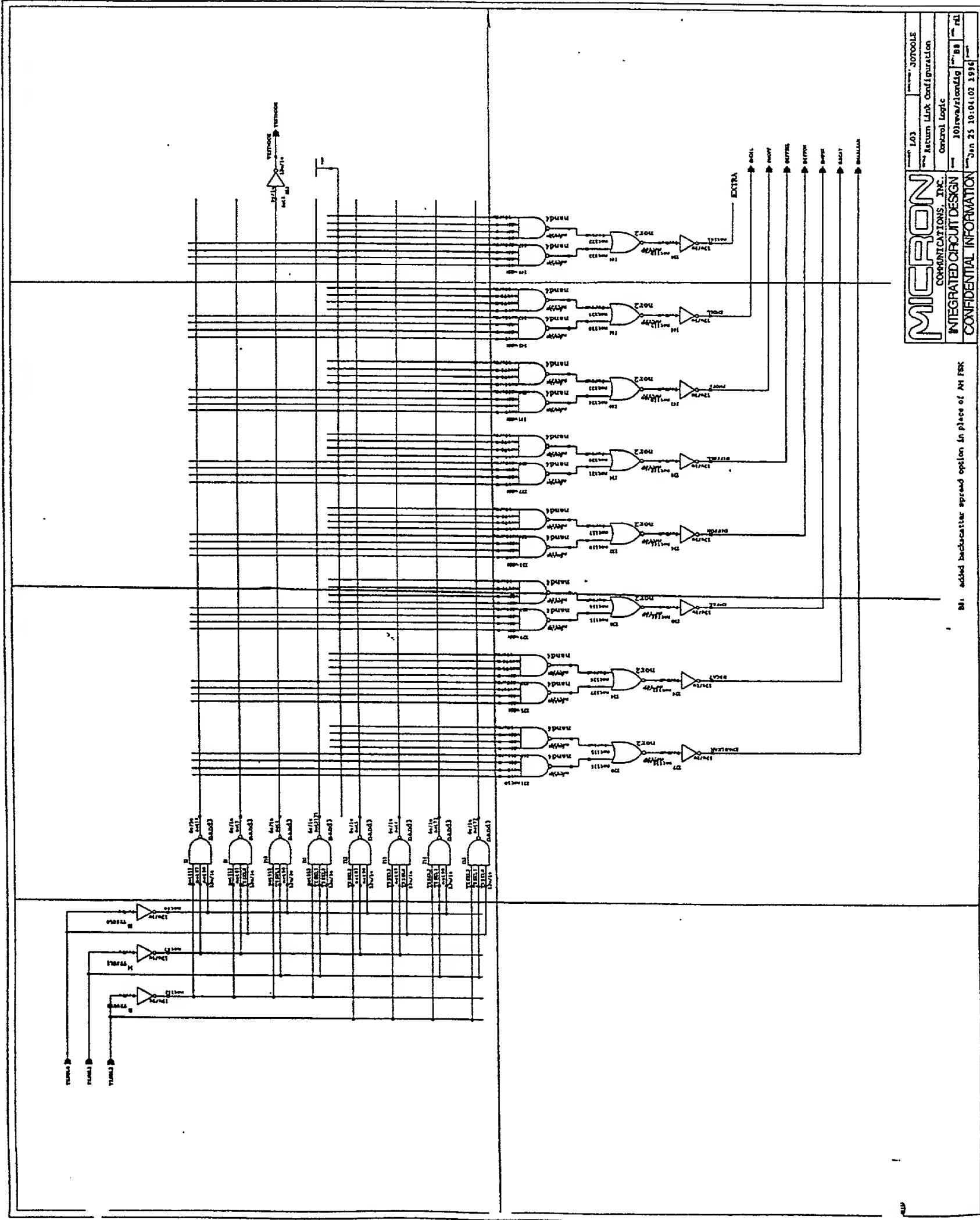


MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital Input Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/paddigin2	REV: B13
CONFIDENTIAL INFORMATION		DATE: May 24 18:28:29 1996	SIZE: A

B13: new cell for WAKEUP* output

Fig 13.5

15AA	15AB	15AC	15AD
	15BA	15BB	15BC



5/6.15

DD: added backscatter spread option in place of AH PSX

MICRON		part no.	103	part no.	J07000LE
COMMUNICATIONS, INC.					
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					
		part	101revs/10end/ig		part no.
		88		rd	
		Jan 25 10:04:02 1996		date	
		General Logic			
		Return Link Configuration			

16AA	16AB	16AC	16AD	16AE	16AF	16AG	16AH
16BA	16BB	16BC	16BD	16BE	16BF	16BG	16BH
16CA	16CB	16CC	16CD	16CE	16CF	16CG	16CH
16DA	16DB	16DC	16DD	16DE	16DF	16DG	16DH
16EA	16EB	16EC	16ED	16EE	16EF	16EG	16EH

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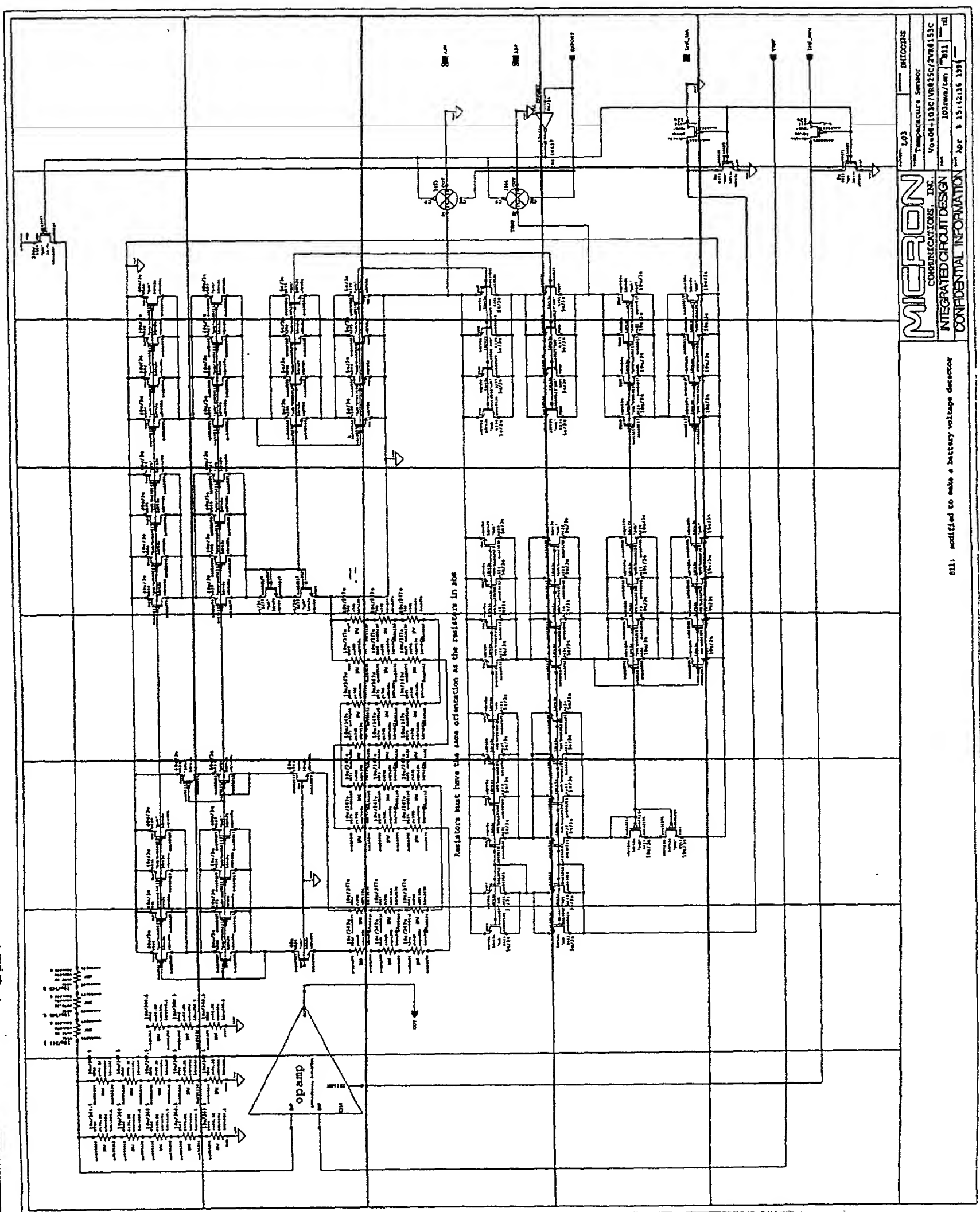


FIG. 16

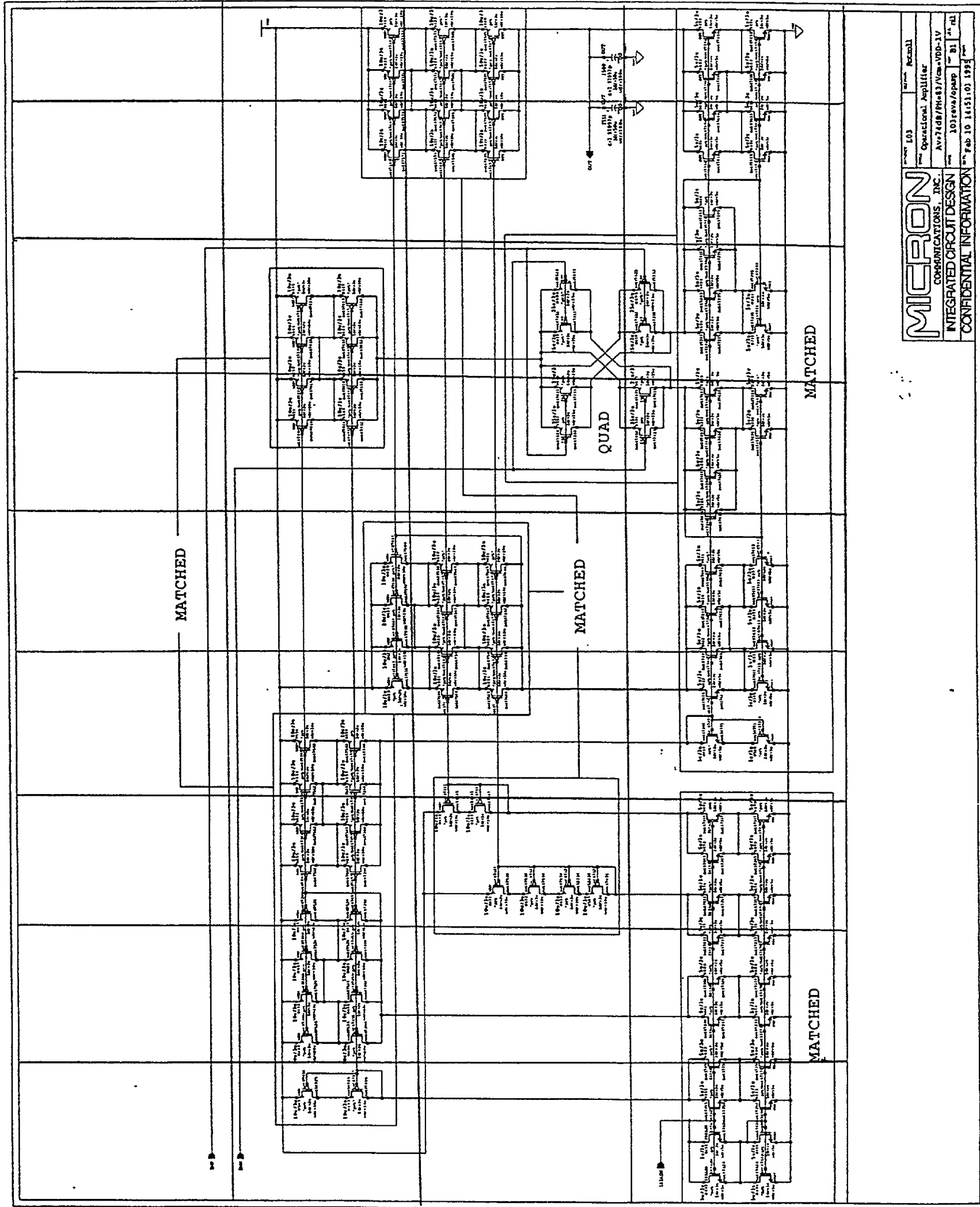
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

NO. 103
TEMPERATURE SENSOR
V₀-08-103C/NR025C/2VR0151C
101ms/cm
111
NOV 8 1982

811: modified to make a battery voltage detector

16.01AA	16.01AB	16.01AC	16.01AD	16.01AE	16.01AF	16.01AG	
16.01BA	16.01BB	16.01BC	16.01BD	16.01BE	16.01BF	16.01BG	16.01BH 16.01BI
16.01CA	16.01CB	16.01CC	16.01CD	16.01CE	16.01CF	16.01CG	16.01CH 16.01CI
16.01DA	16.01DB	16.01DC	16.01DD	16.01DE	16.01DF	16.01DG	16.01DH 16.01DI

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MICRON
 COMMUNICATIONS, INC.
 INTEGRATED CIRCUIT DESIGN
 CONFIDENTIAL INFORMATION

Part 103
 Operational Amplifier
 AV7408/PH-83/VCM-VDD-1V
 103 revs/comp
 Feb 10 14:51:01 1998

FIG. 16.01

17AA	17AB
17BA	17BB

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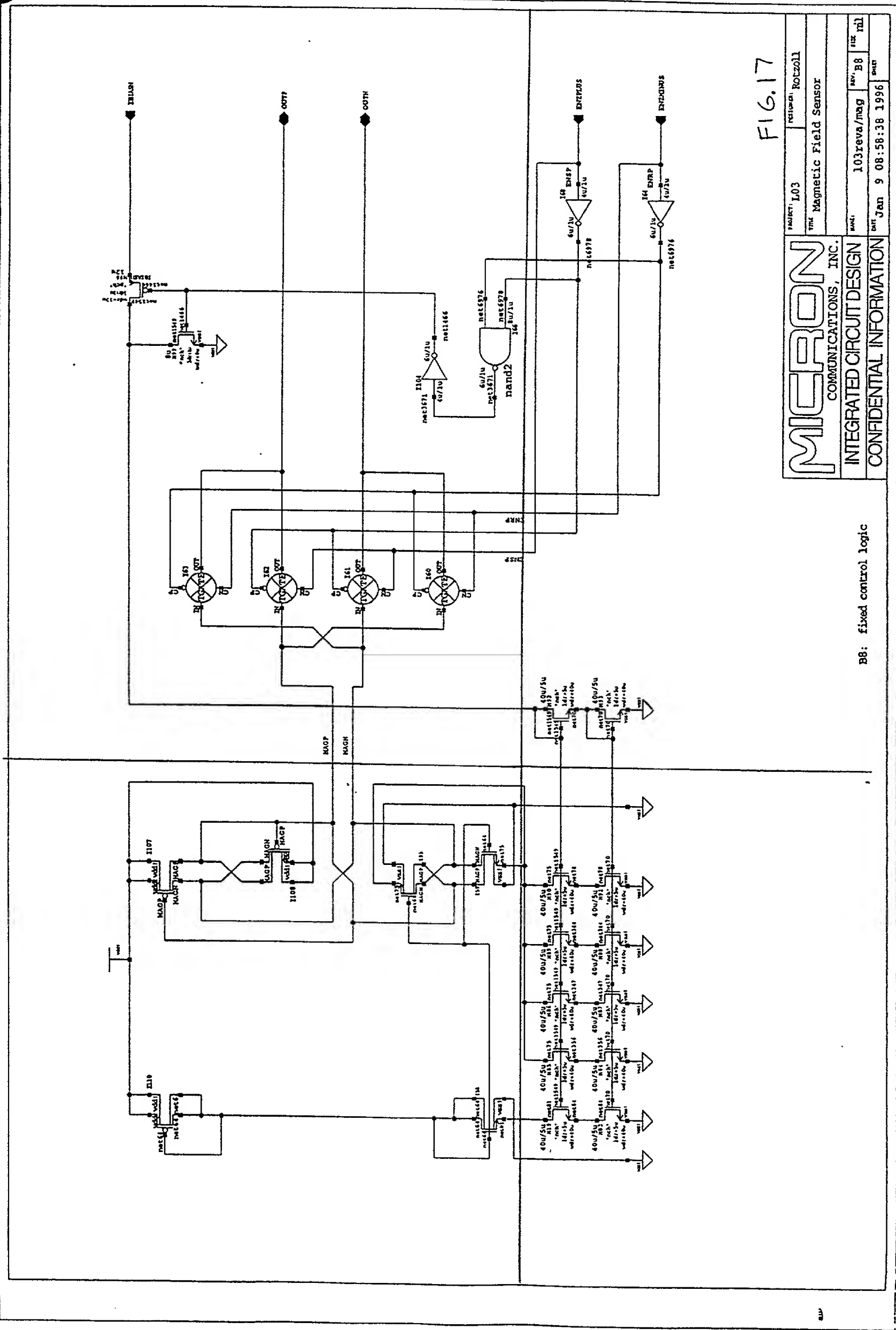


FIG. 17

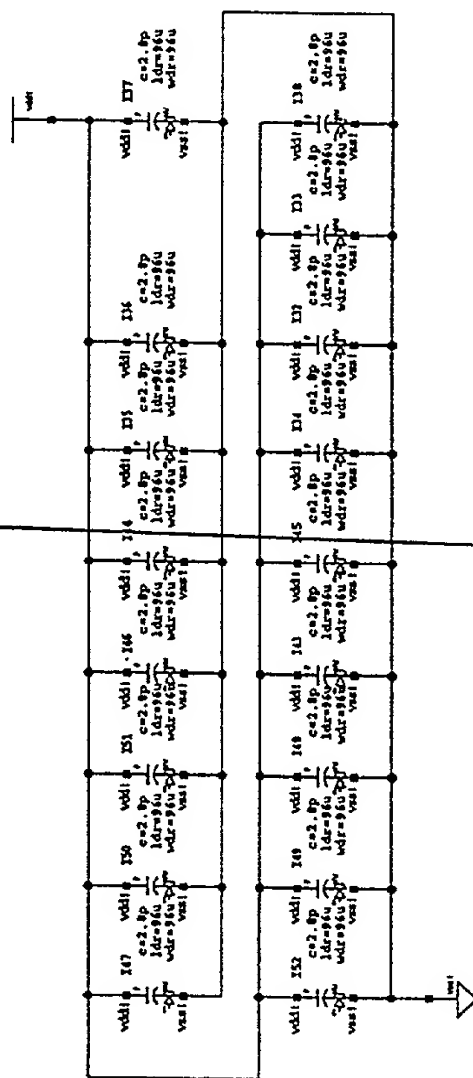
MICRON		PROJECT: L03	DESIGNED BY: Rotzoll
COMMUNICATIONS, INC.		TITLE: Magnetic Field Sensor	
INTEGRATED CIRCUIT DESIGN		DATE: 103revA/mag	REV: B8
CONFIDENTIAL INFORMATION		DATE: Jan 9 08:58:38 1996	BY: ml

B8: fixed control logic

18AB

18AA

18AA 18BB



١٥٧

MICRON		PROJECT: L03	DATE/REV: J0700LE
COMMUNICATIONS, INC.		TITLE	
INTEGRATED CIRCUIT DESIGN		Chip Bypass Capacitor	
CONFIDENTIAL INFORMATION		Ct = pF	
NAME:	103reva./byrcap3	REV: B2	FILE: ml
DATE	Jul 28 17:43:25 1995	DSKT	

B2: deleted one cap

19AA	19AB	19AC	19AD	19AE	19AF	19AG	19AH	19AI	19AJ	19AK
19BA	19BB	19BC	19BD	19BE	19BF	19BG	19BH	19BI	19BJ	19BK
19CA	19CB	19CC	19CD	19CE	19CF	19CG	19CH	19CI	19CJ	19CK
19DA	19DB	19DC	19DD	19DE	19DF	19DG	19DH	19DI	19DJ	19DK
19EA	19EB	19EC	19ED	19EE	19EF	19EG	19EH	19EI	19EJ	19EK

II II II II

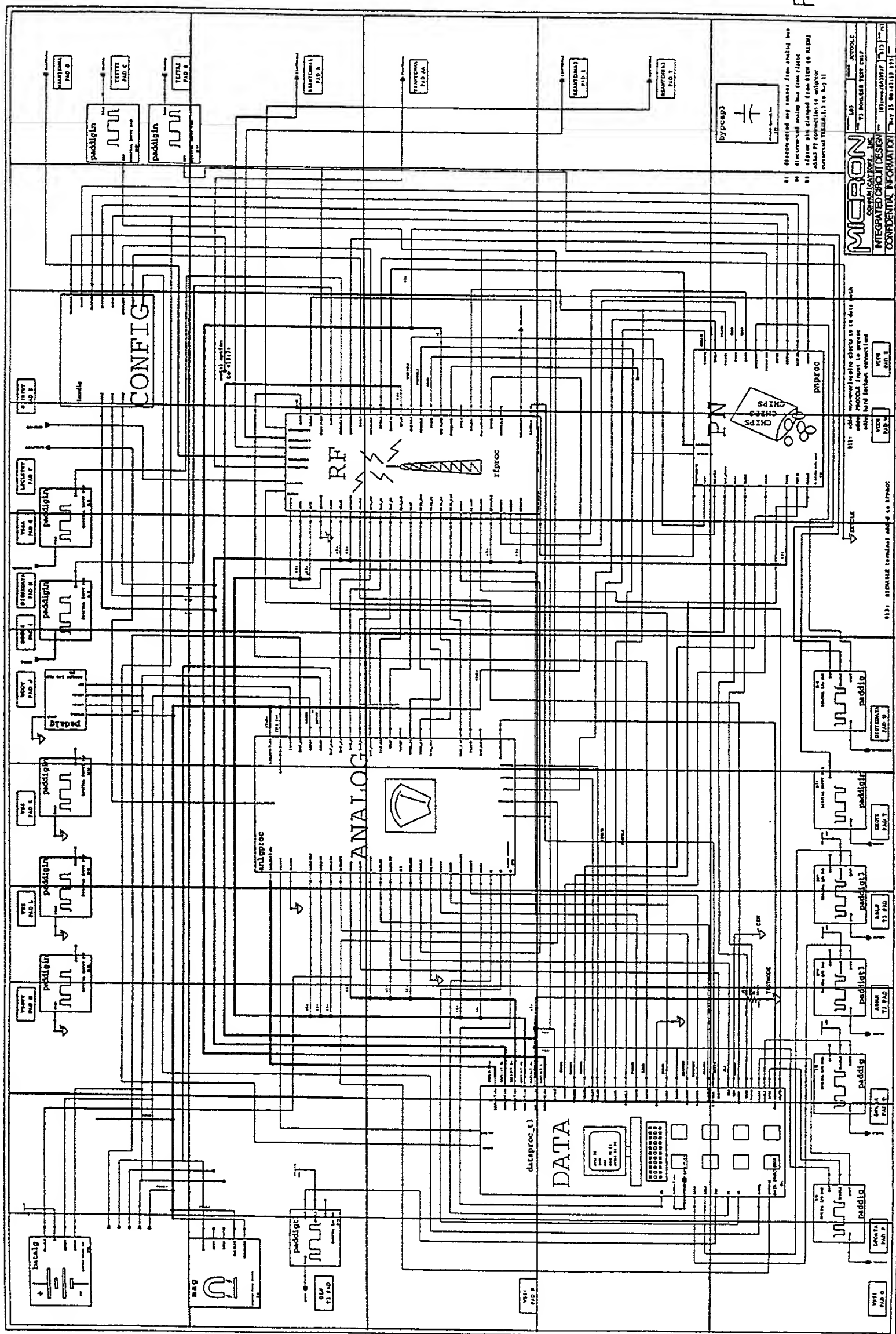


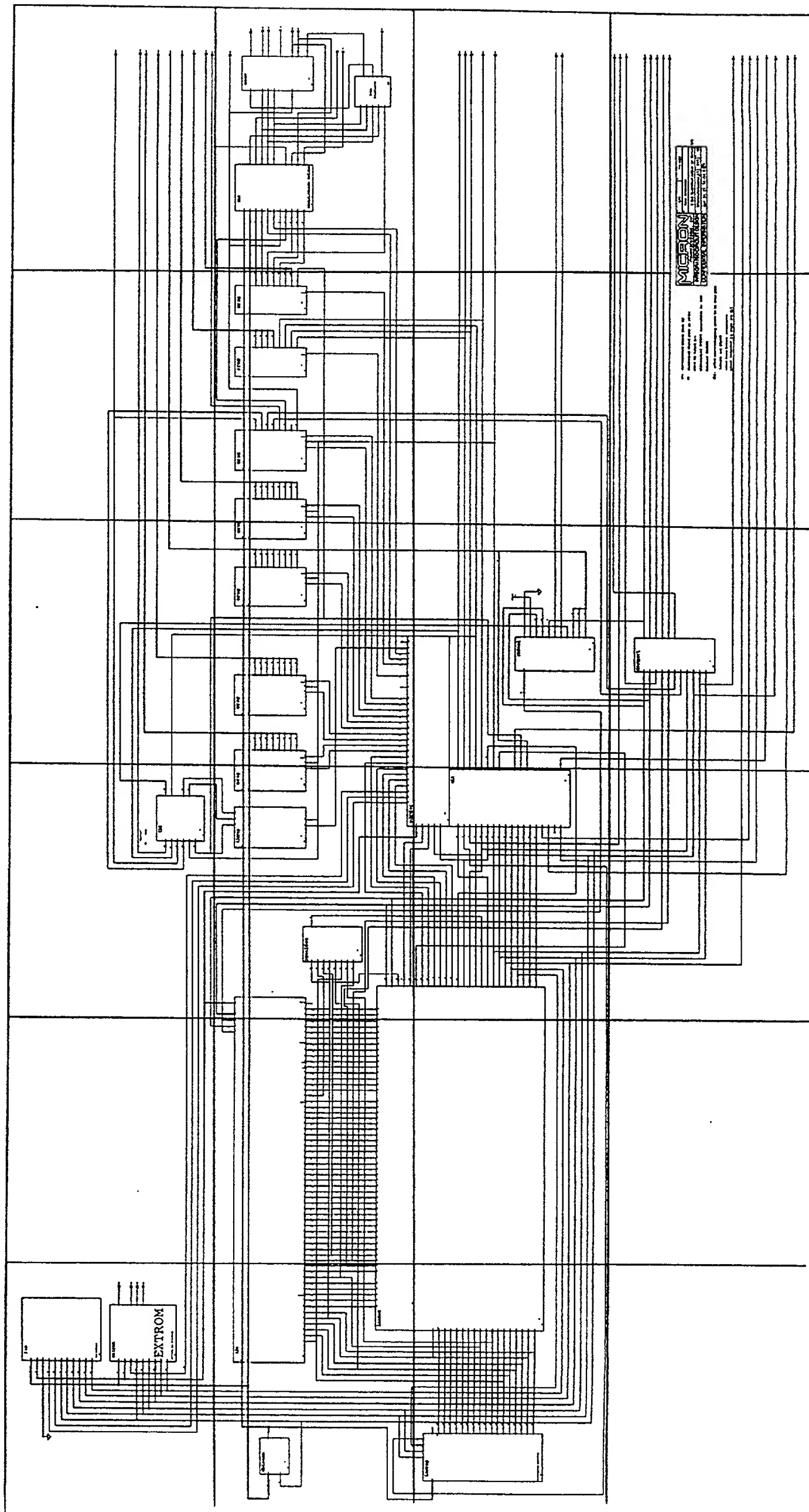
FIG. 19. AA-EK

20AA	20AB	20AC	20AD	20AE	20AF
20BA	20BB	20BC	20BD	20BE	20BF
20CA	20CB	20CC	20CD	20CE	20CF
		20DC	20DD	20DE	20DF

II II II II II

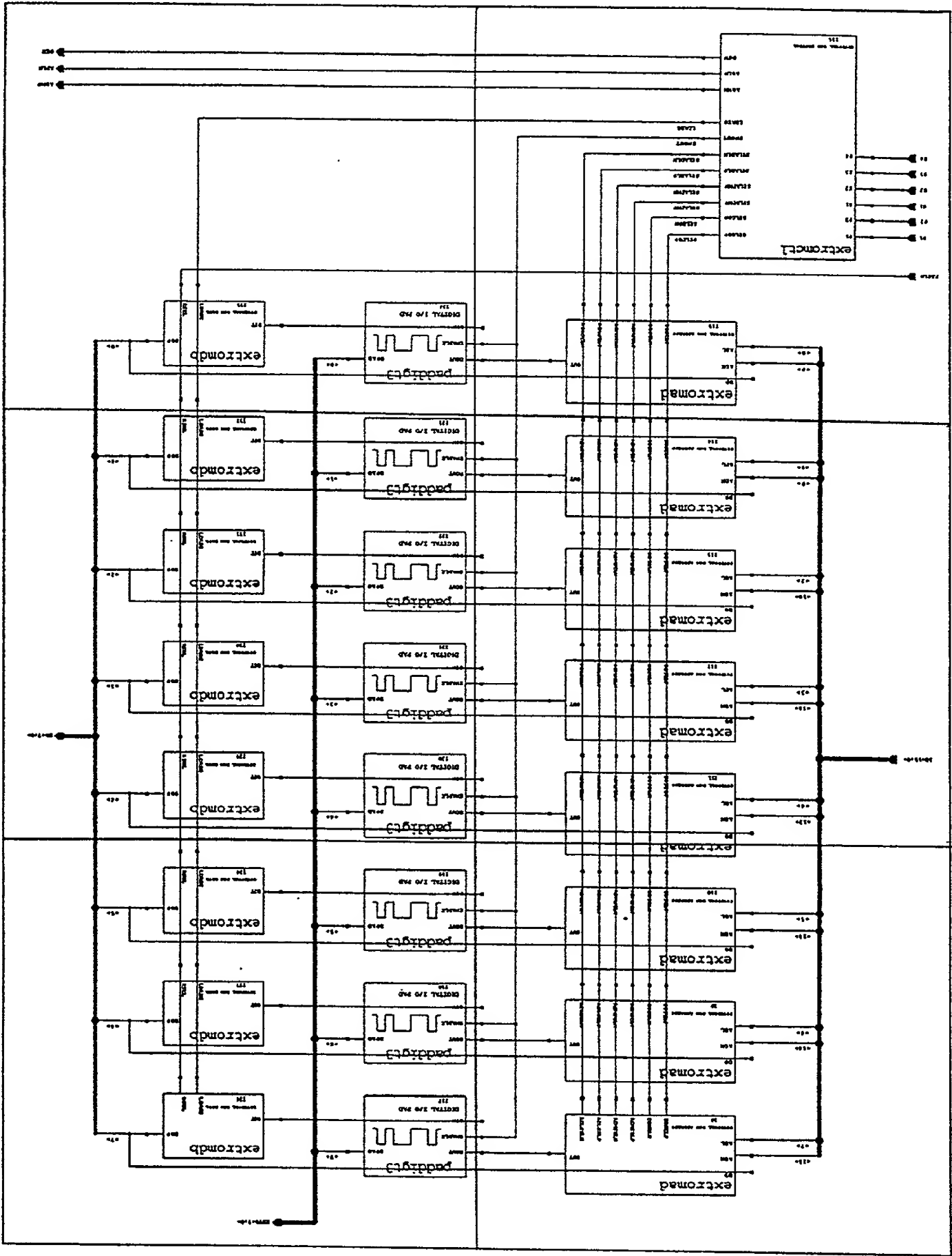
[illegible]

Fig. 20



20.01AA	20.01AB
20.01BA	20.01BB
20.01CA	20.01CB

Fig. 20.01



This diagram is a schematic representation of the internal circuitry of the NORCOM device. It shows the interconnection of various functional blocks, including digital I/O pads and extromad blocks, which are used for data processing and communication. The diagram is a high-level overview and does not show the detailed internal structure of the individual components.

20.0101AA	20.0101AB
20.0101BA	20.0101BB

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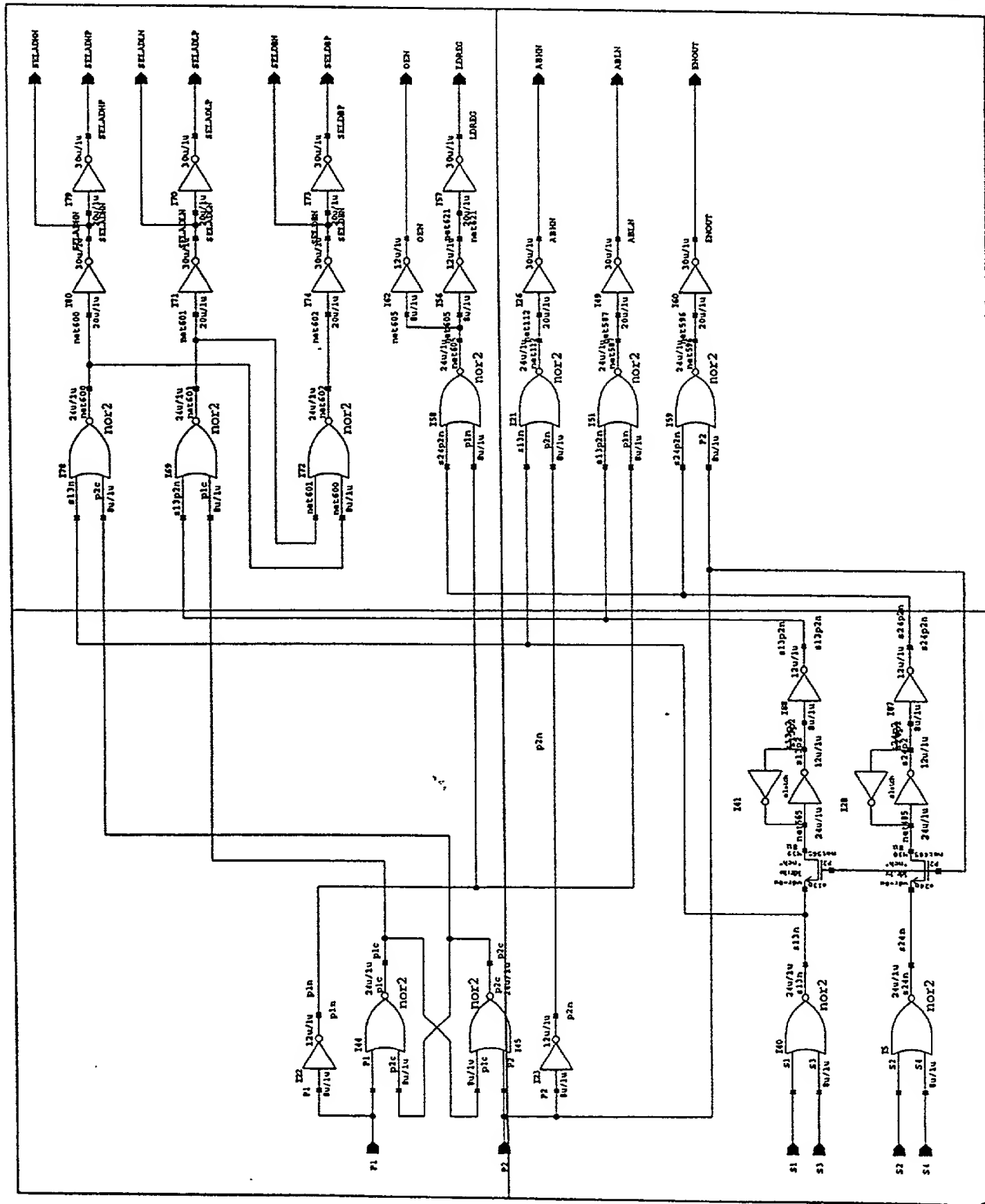


FIG. 20.0101

PROJECT L03		DESIGNER	Rotzoll
TITLE		External ROM Control Logic	
DATE:	103revA/extract1	REV	-
DATE:	Dec 11 21:56:41 1993	REV	nil
CONFIDENTIAL INFORMATION		PAGE: 1	

MICRON
 COMMUNICATIONS, INC.
 INTEGRATED CIRCUIT DESIGN
 CONFIDENTIAL INFORMATION

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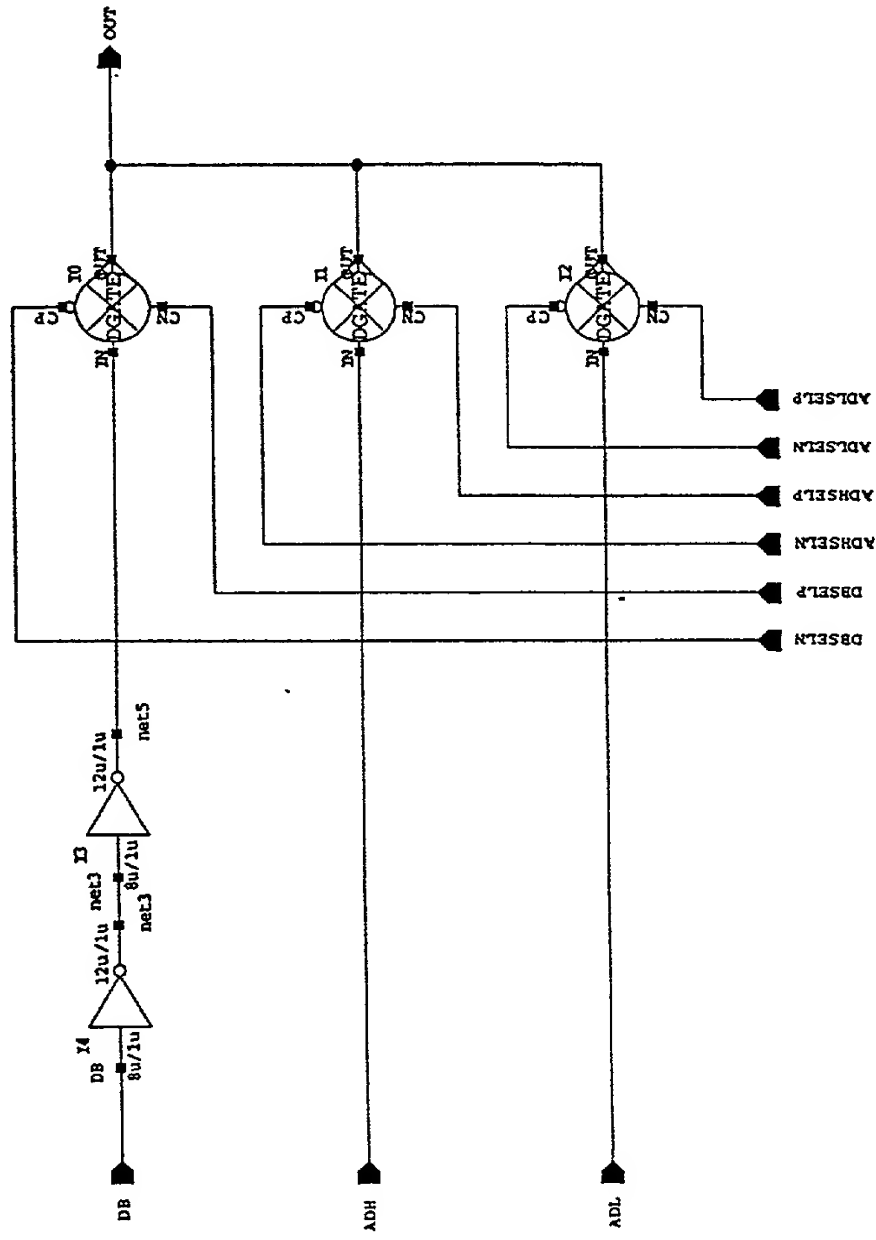


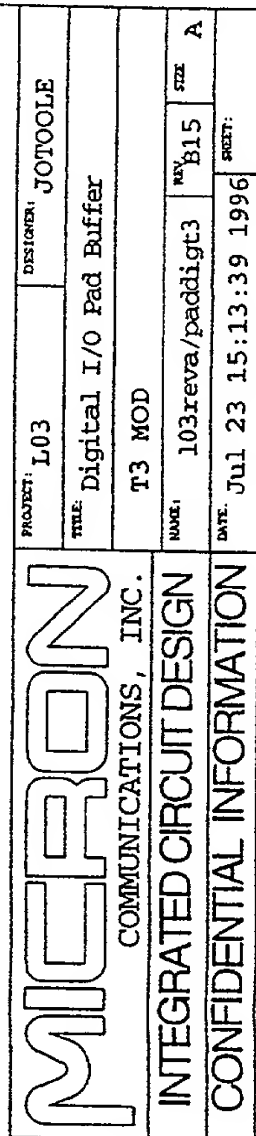
Fig. 20.0102

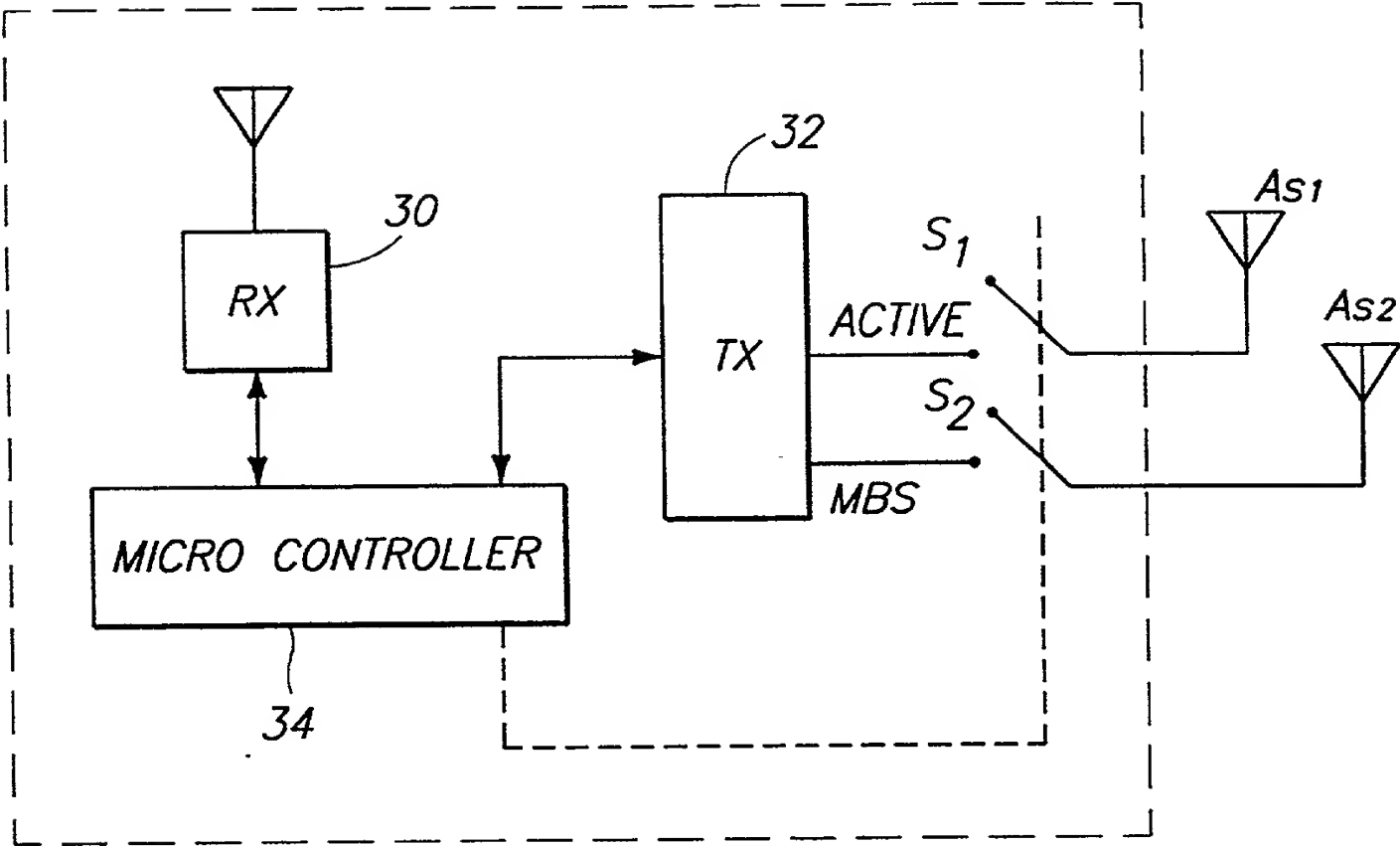
MICRON				DESIGNER: Rotzoll	
COMMUNICATIONS, INC.				PROJECT: L03	
INTEGRATED CIRCUIT DESIGN				TITLE: External ROM Address Interface	
CONFIDENTIAL INFORMATION					
NAME: 103reva/extromad		REV: -		SIZE: A	
DATE: Dec 11 01:09:14 1993		SHEET:			

MICRON
 COMMUNICATIONS, INC.
 INTEGRATED CIRCUIT DESIGN
 CONFIDENTIAL INFORMATION

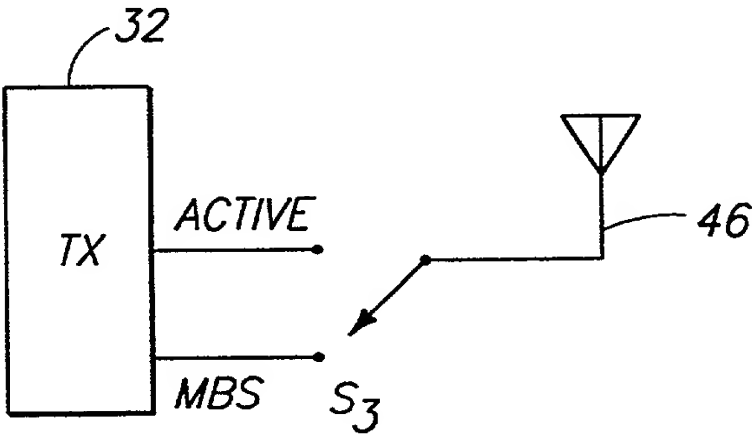
20.0103AA	20.0103AB	20.0103AC
-----------	-----------	-----------

EMITTING

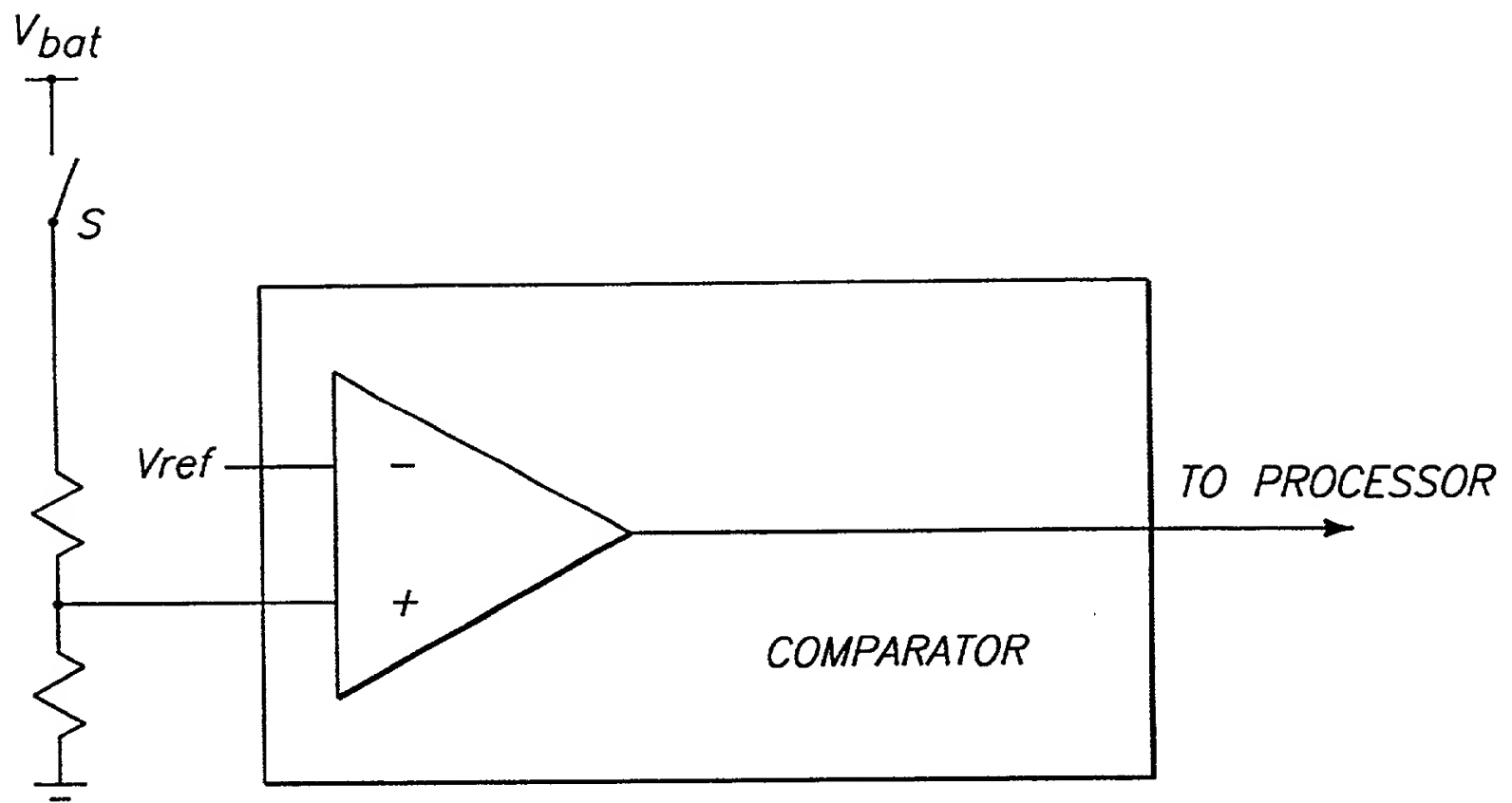




II II II II II

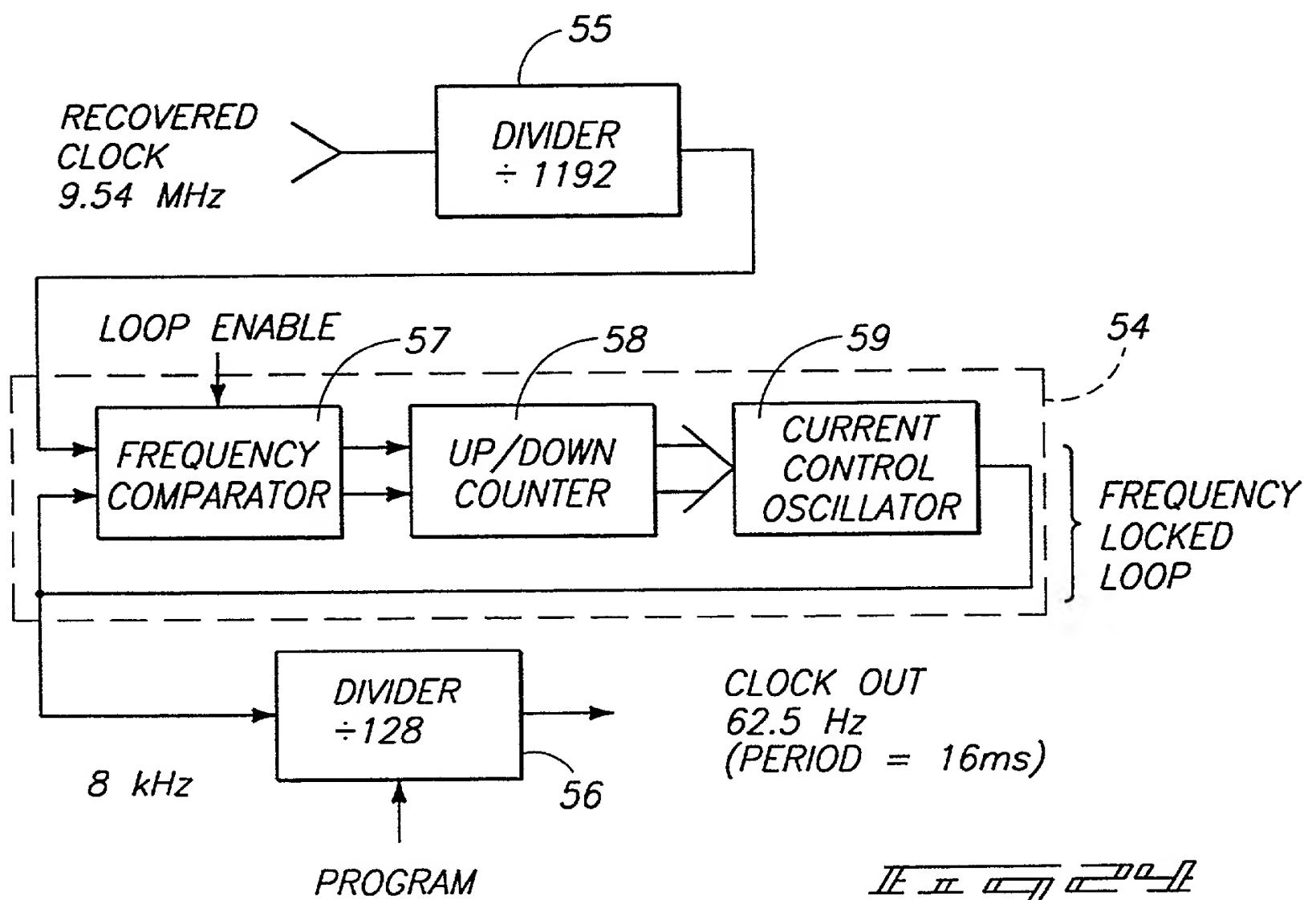


II II II II II



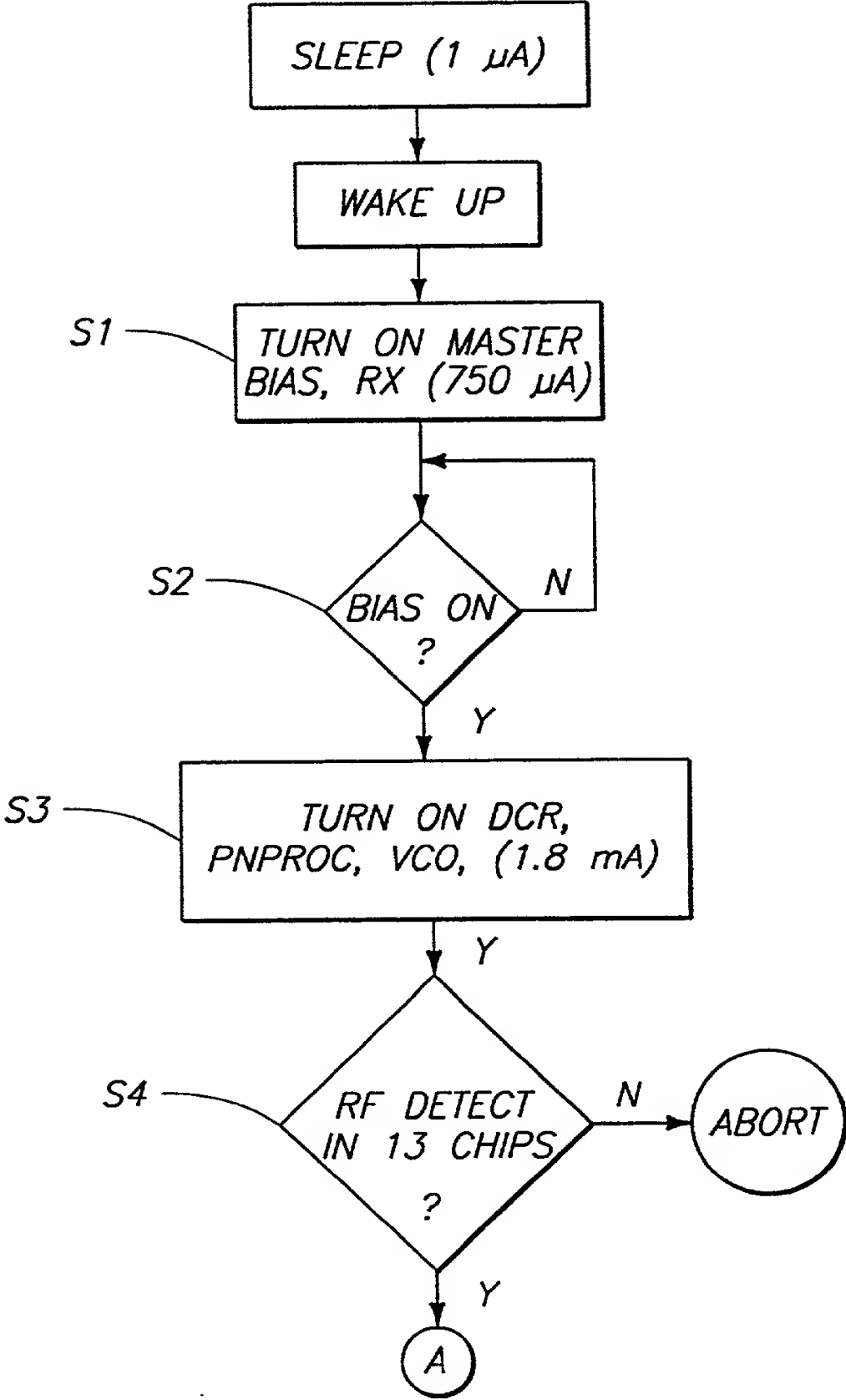
$V_{ref} = \text{bandgap voltage} \approx 1.2 \text{ V for silicon}$

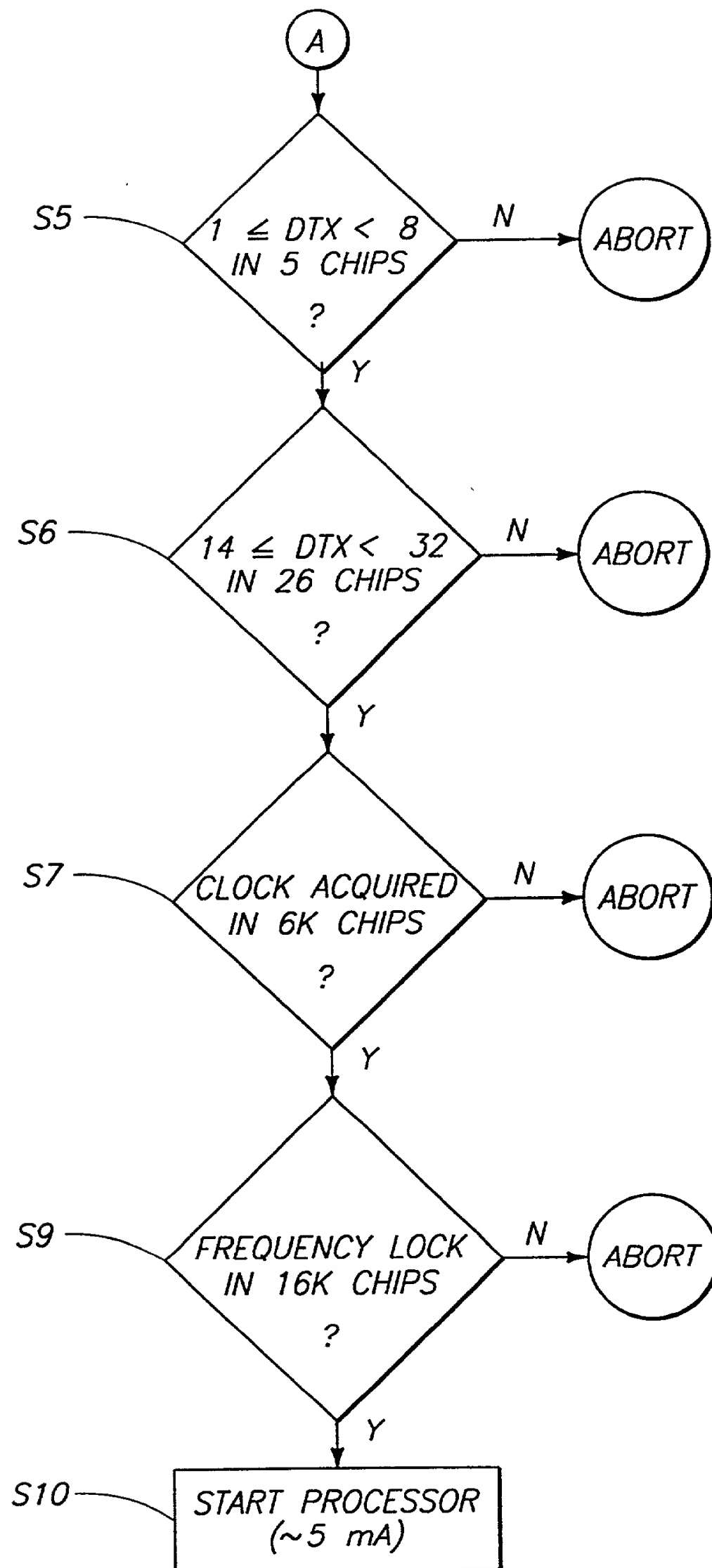
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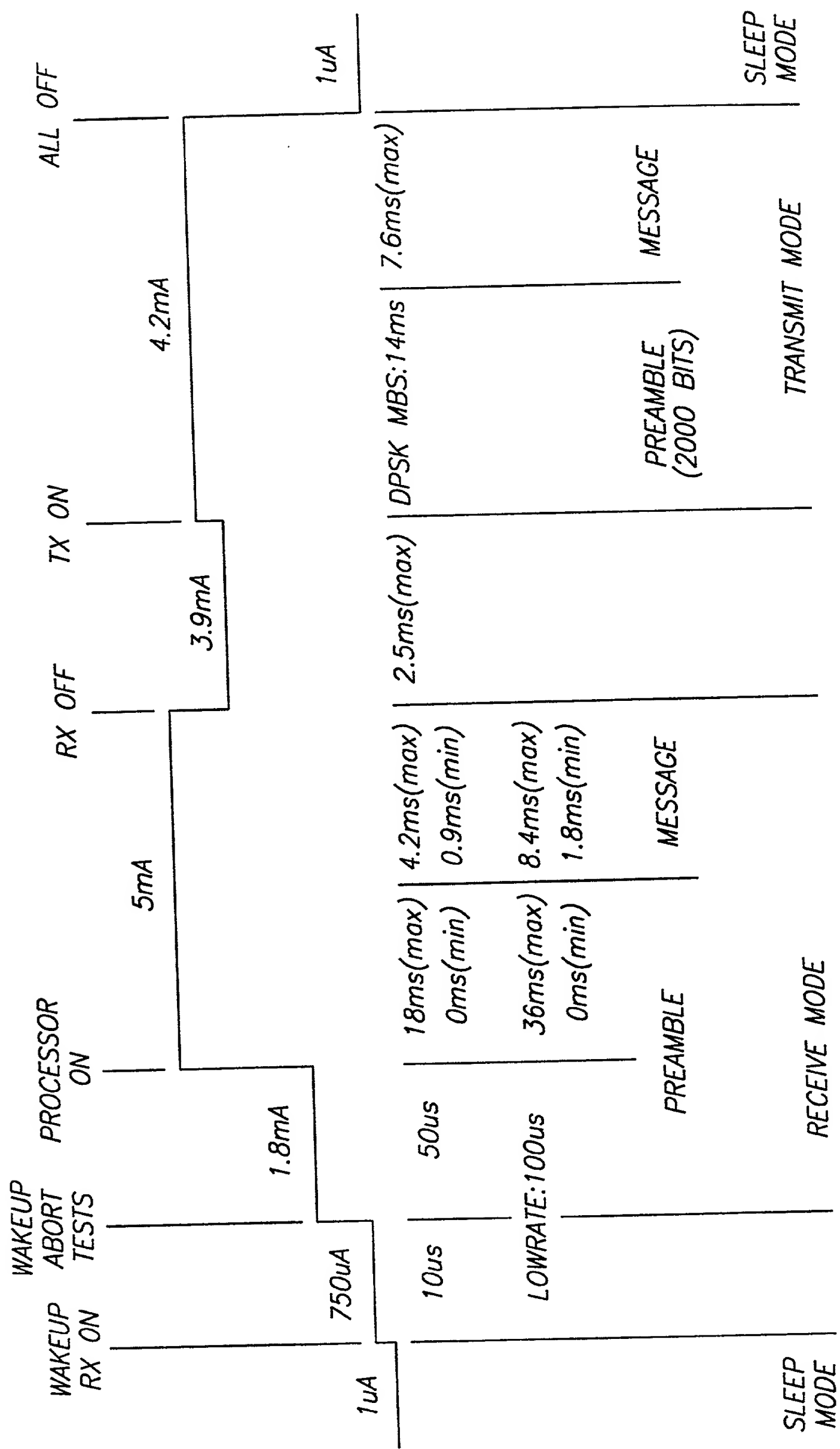


II II II II II

WAKEUP SEQUENCE







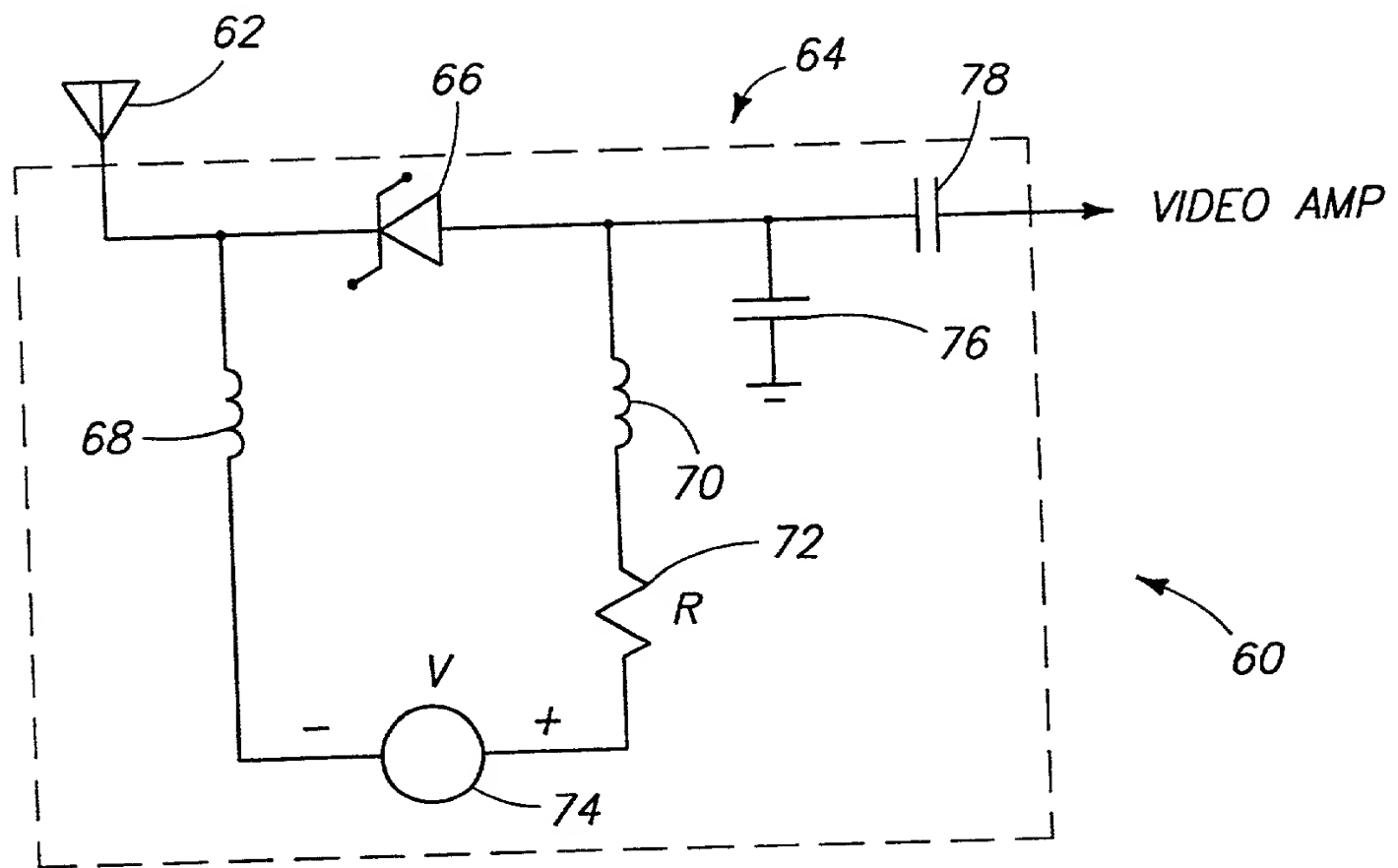


FIG. 2

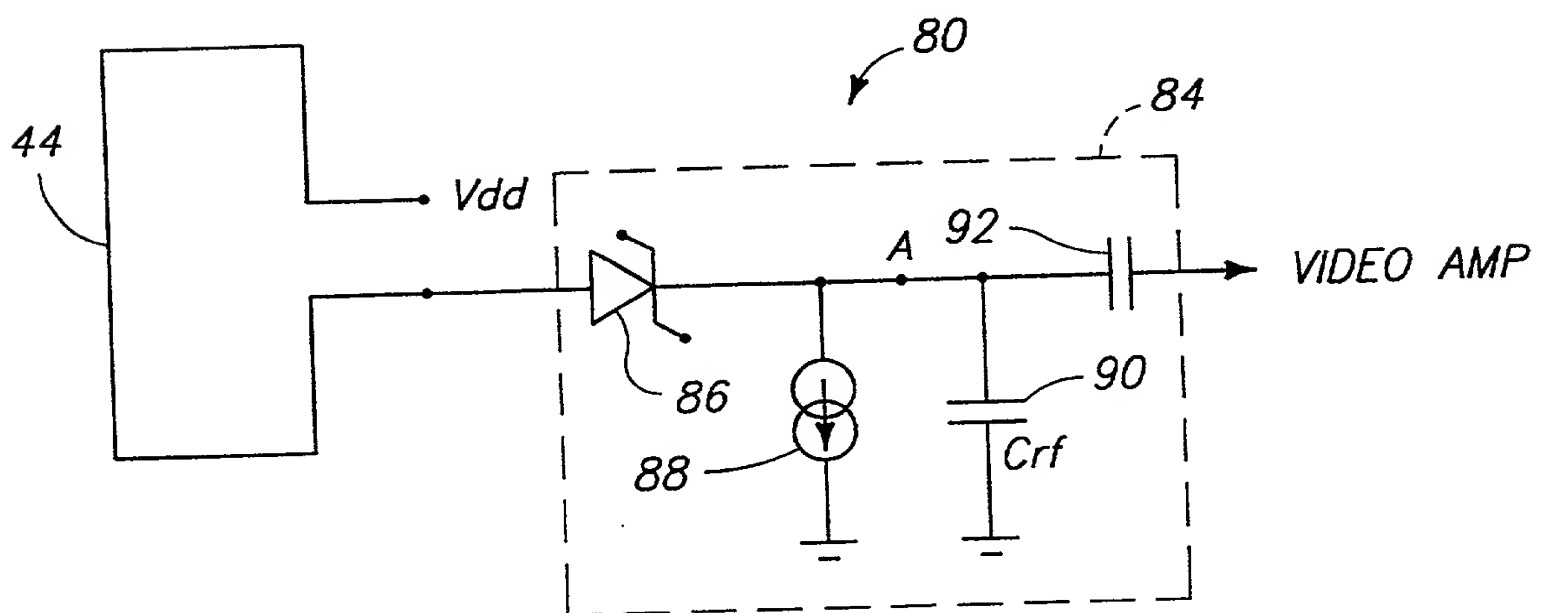
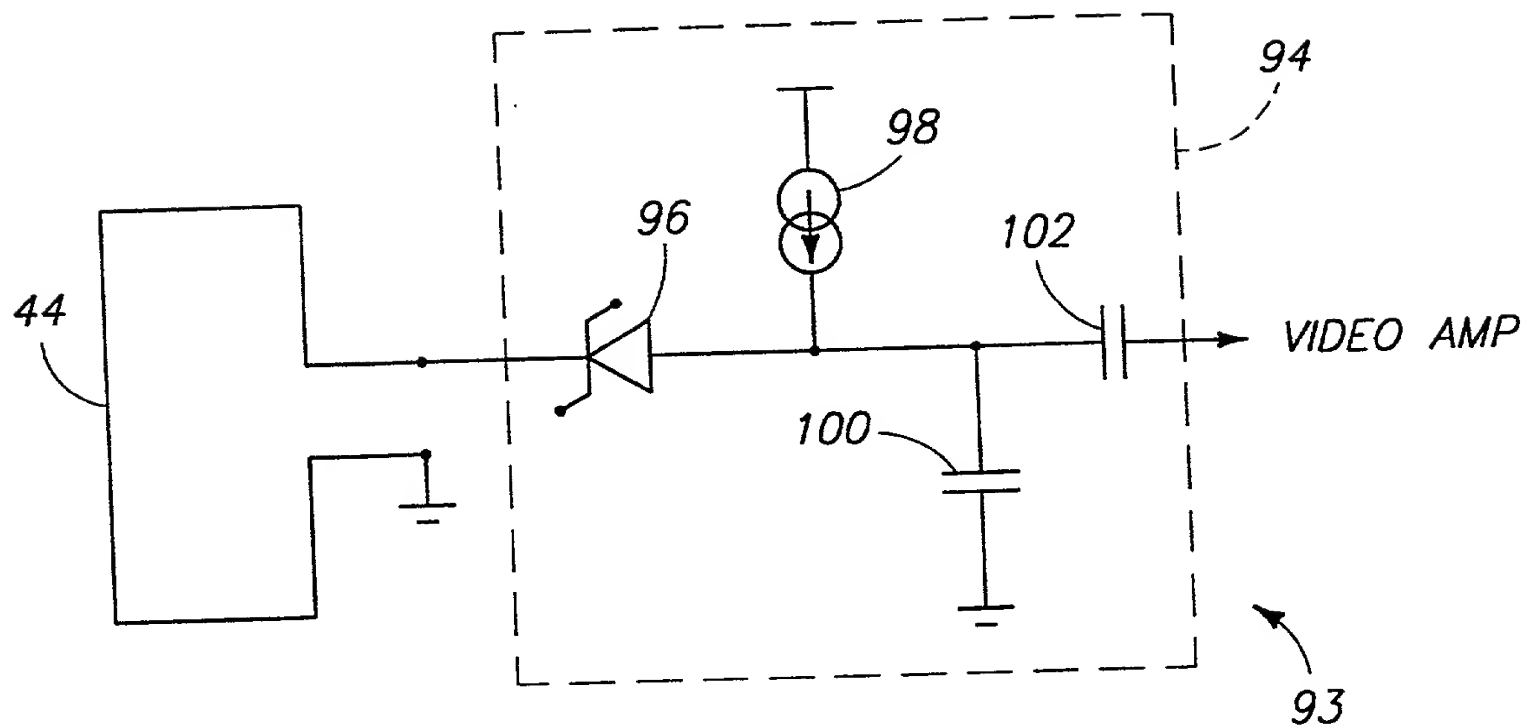
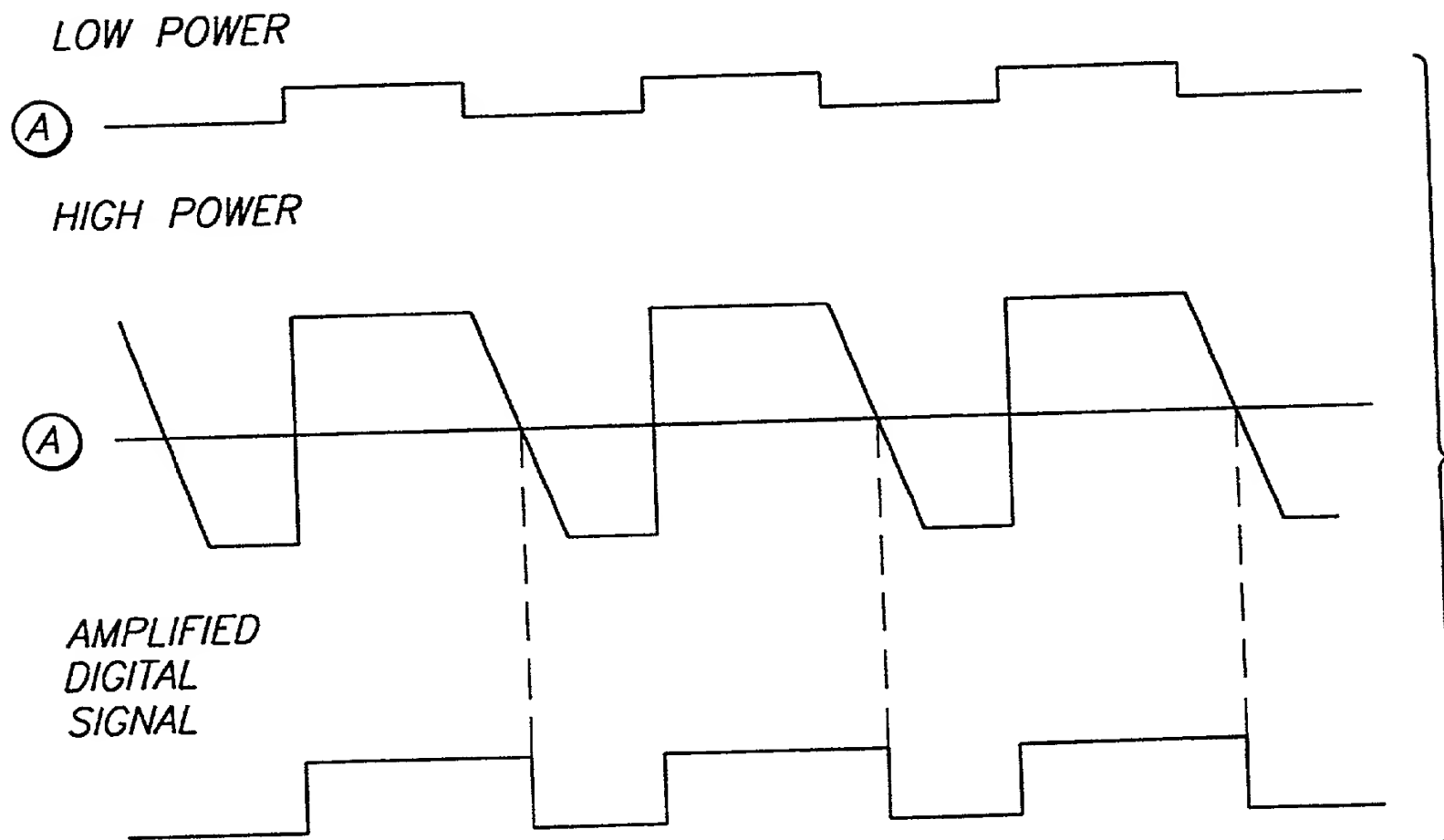


FIG. 3



IF II III



IF II III



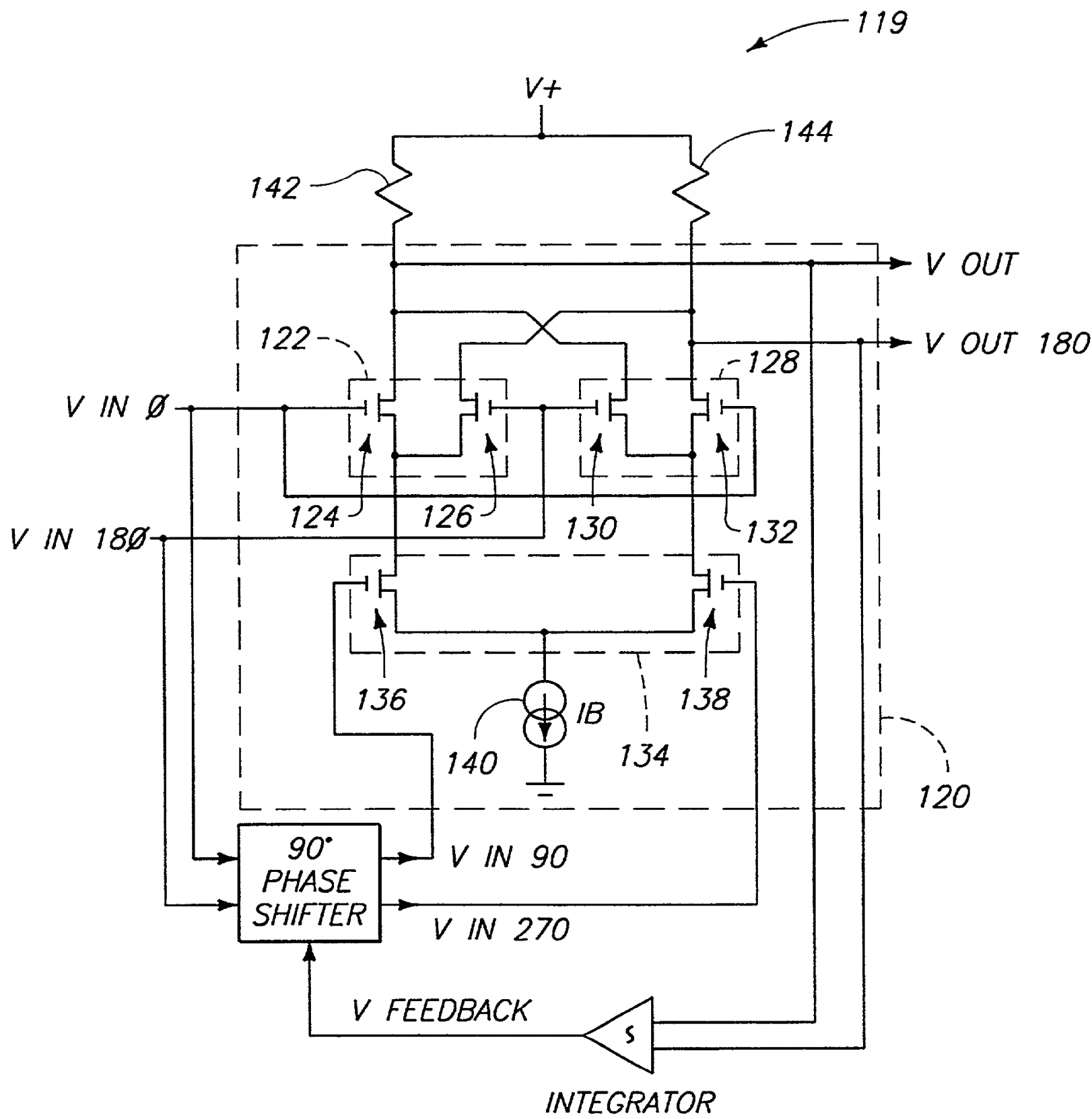


FIG. 1

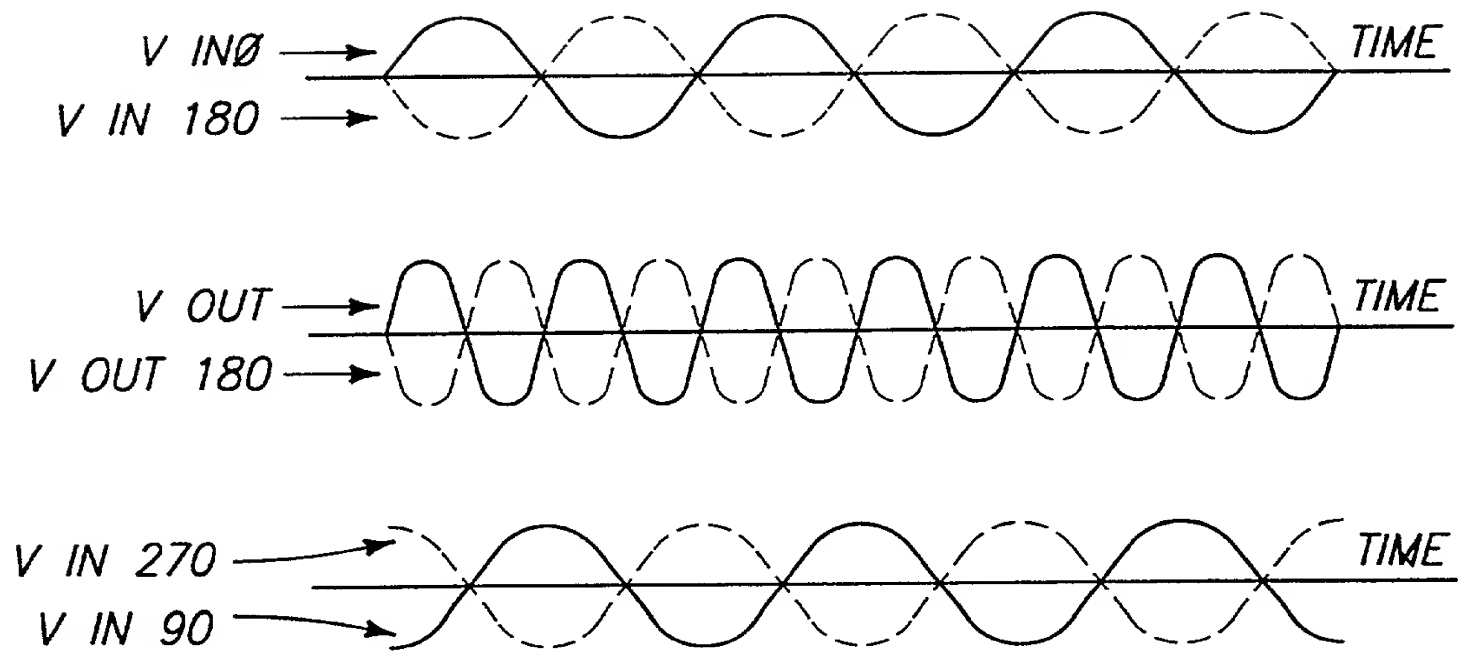


FIG. 35

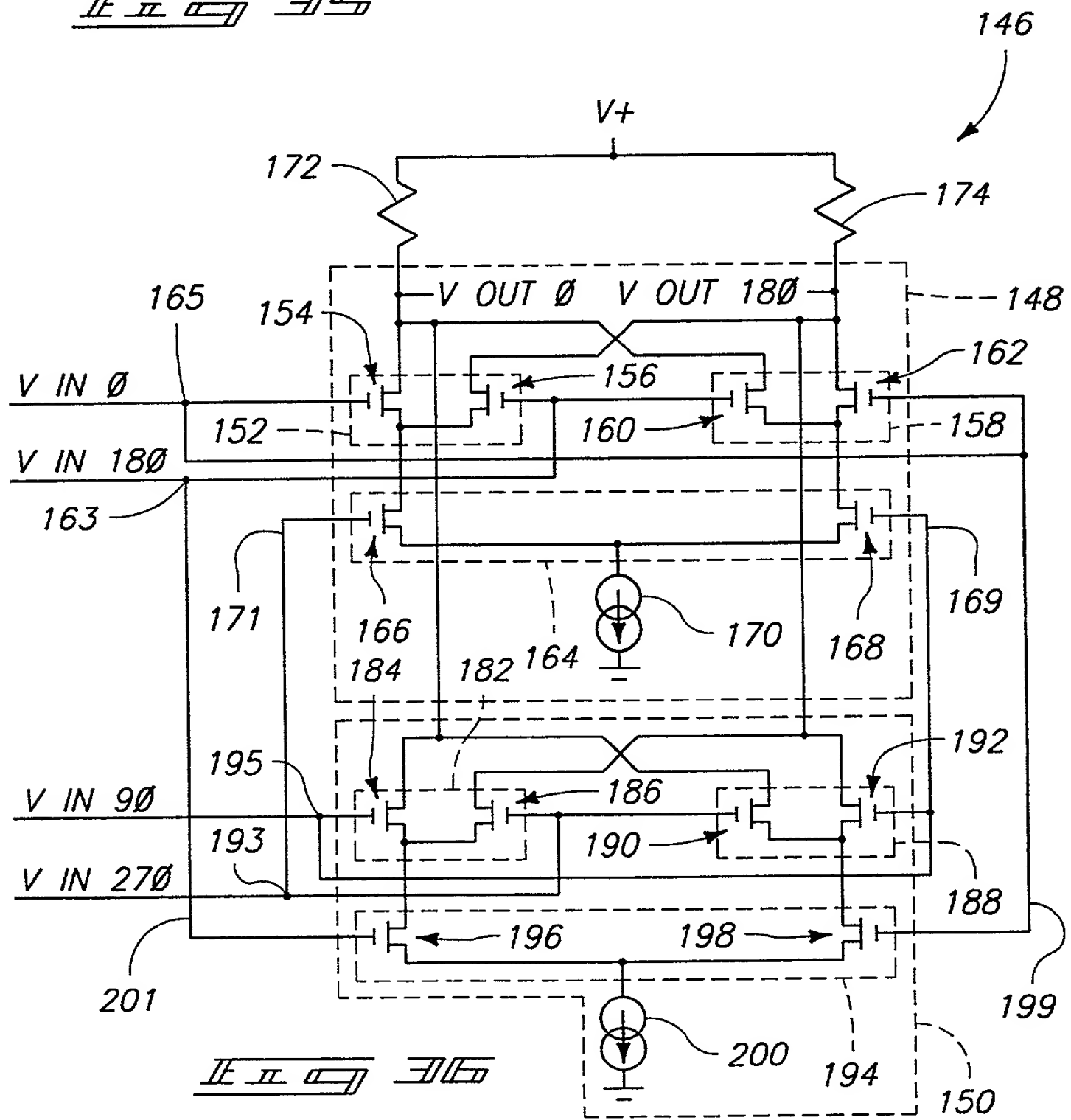
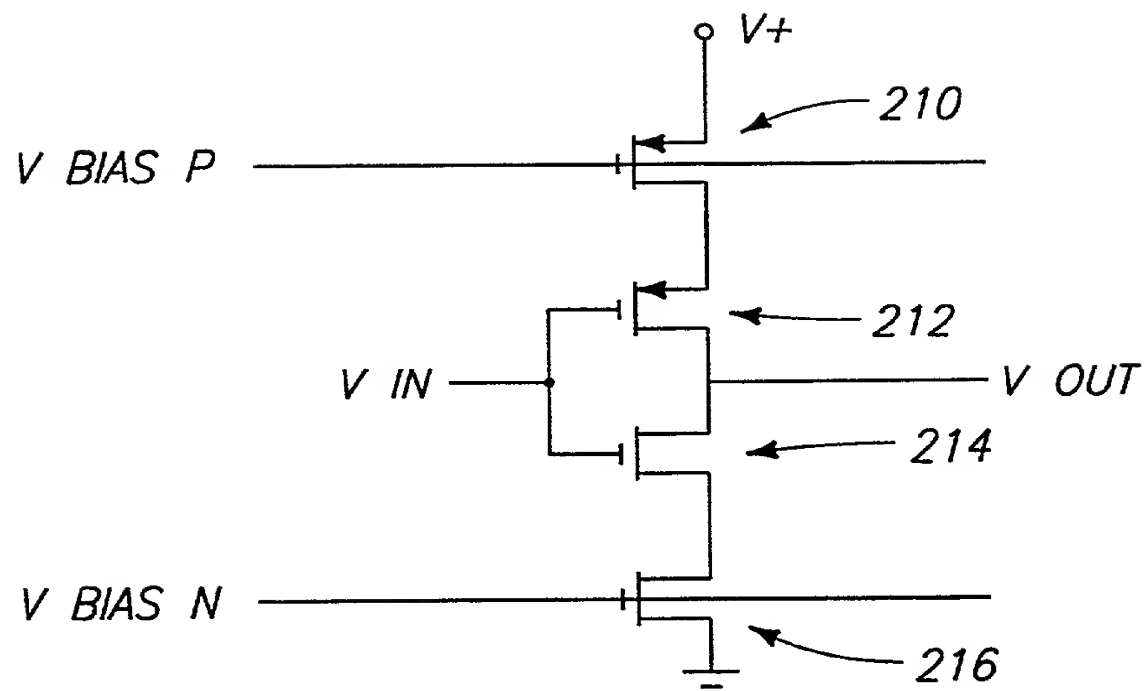
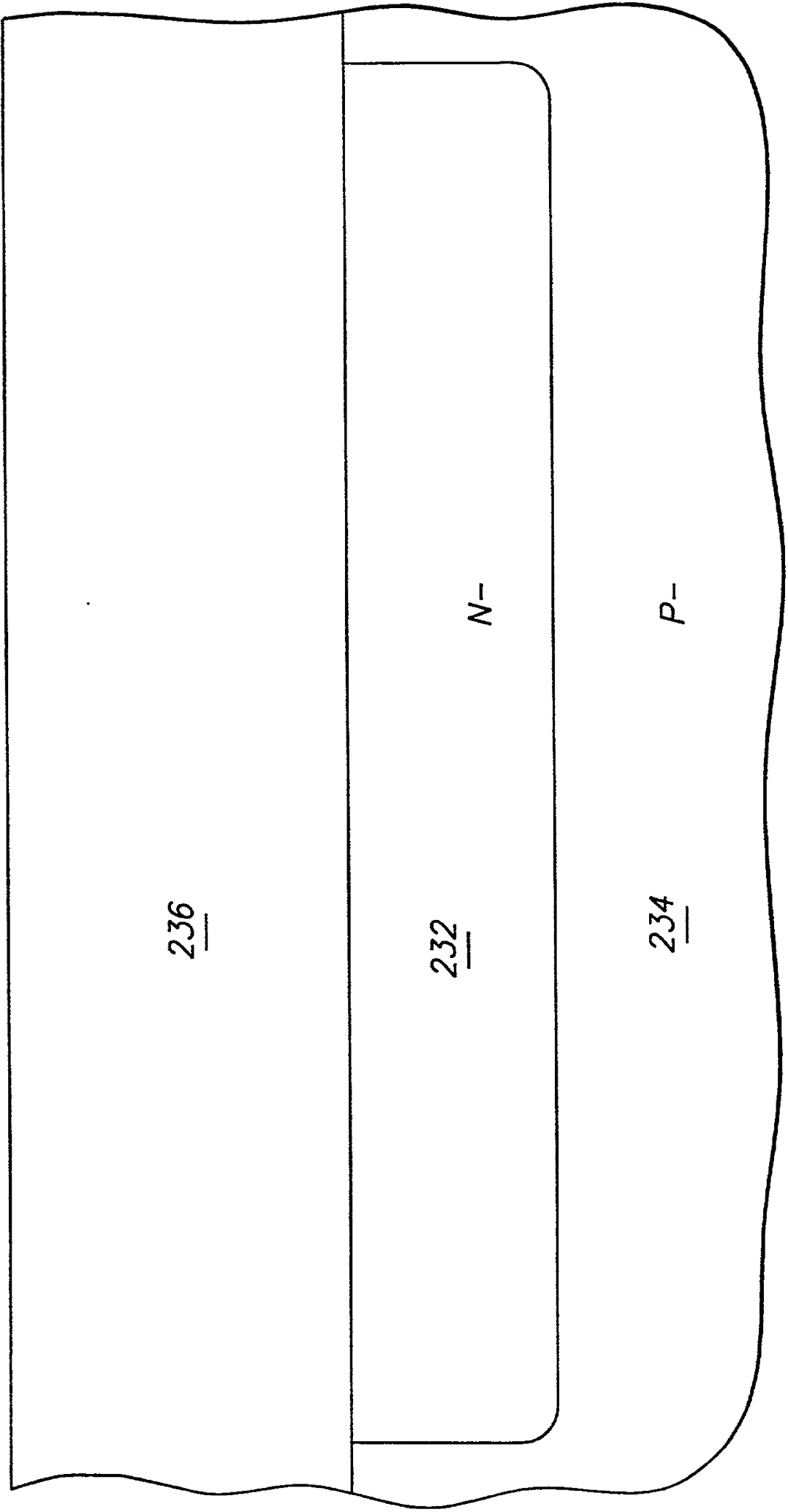


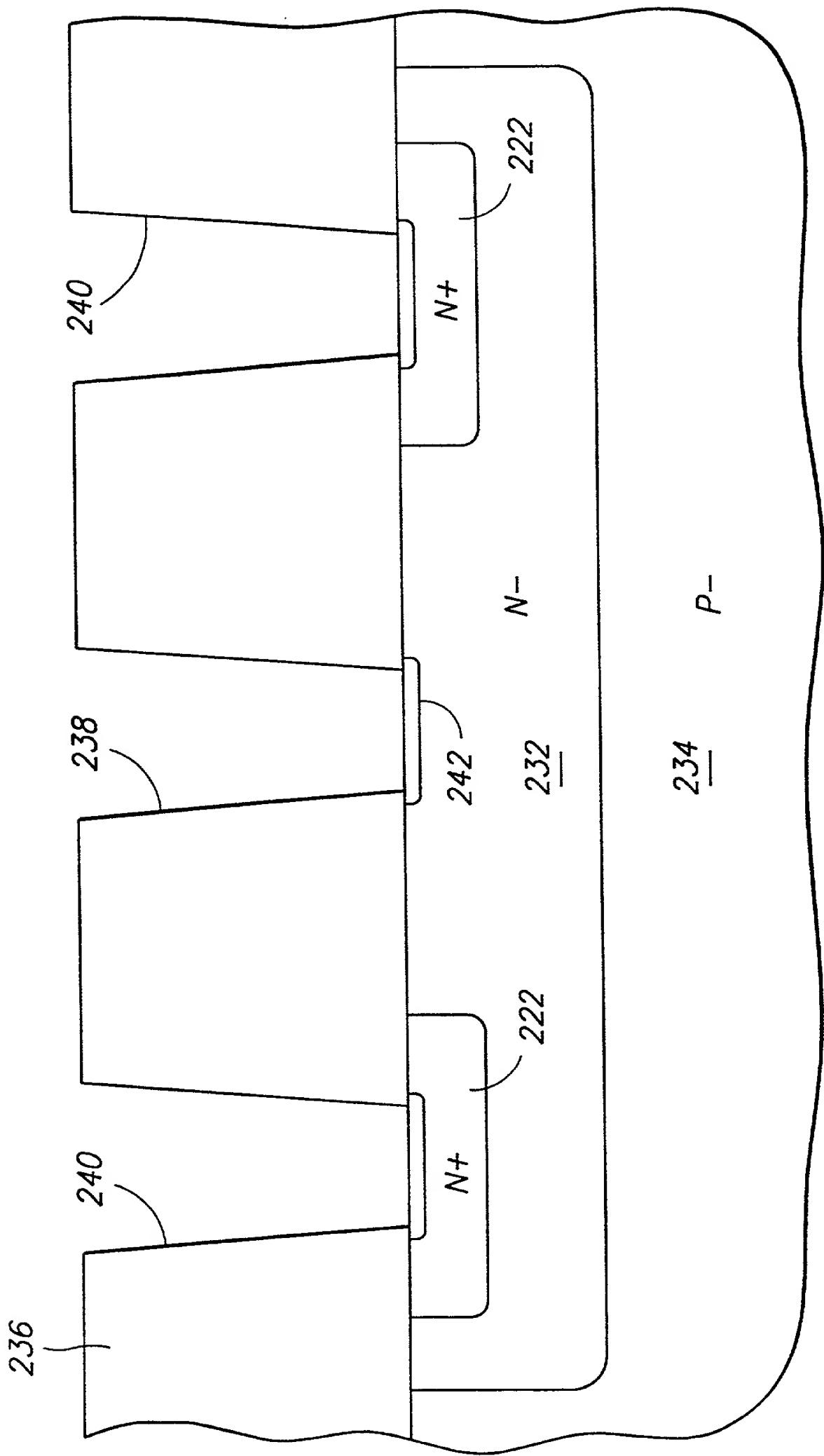
FIG. 36



II π □ ∇ ∇ ∇



II II III III



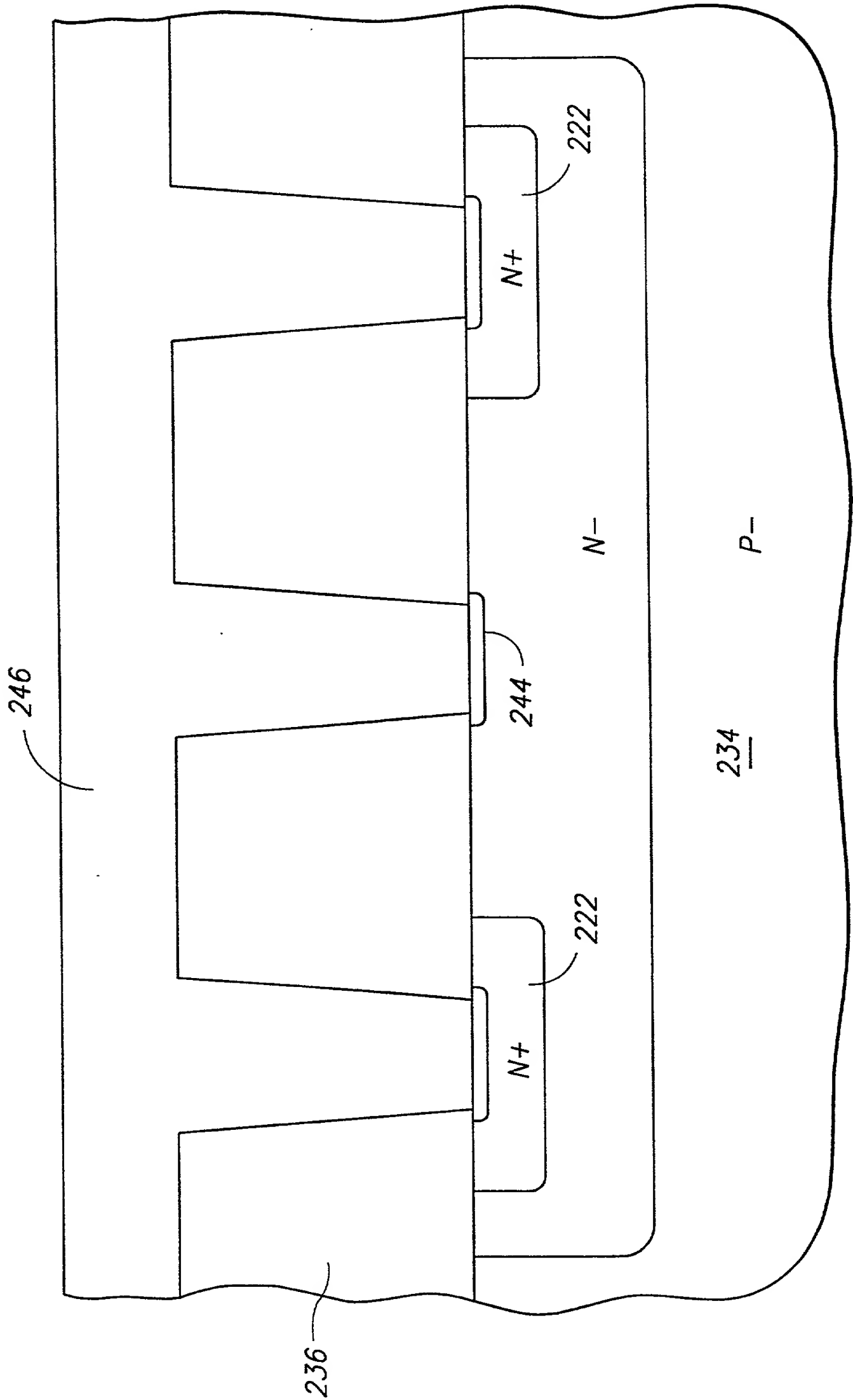
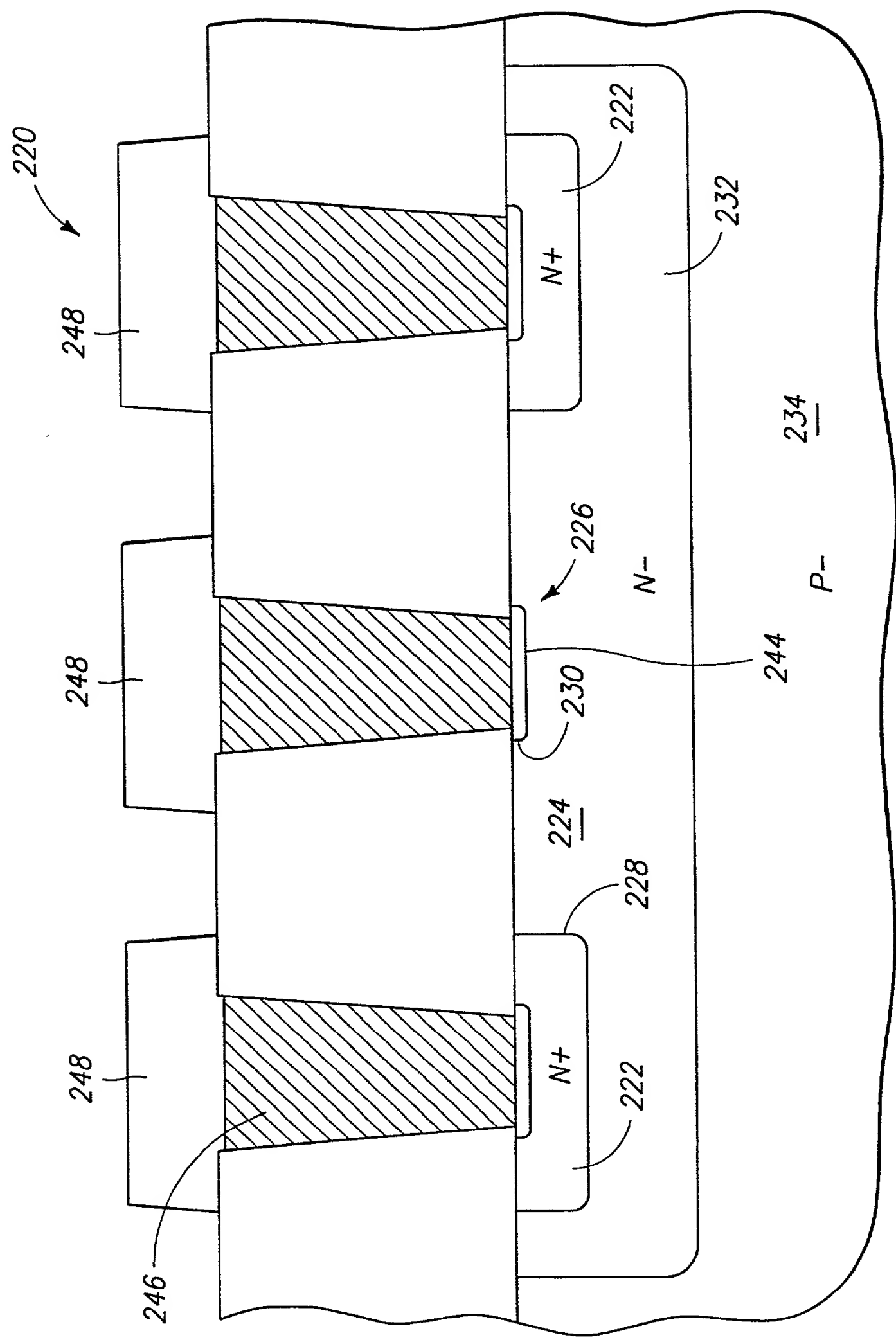


FIG. 1



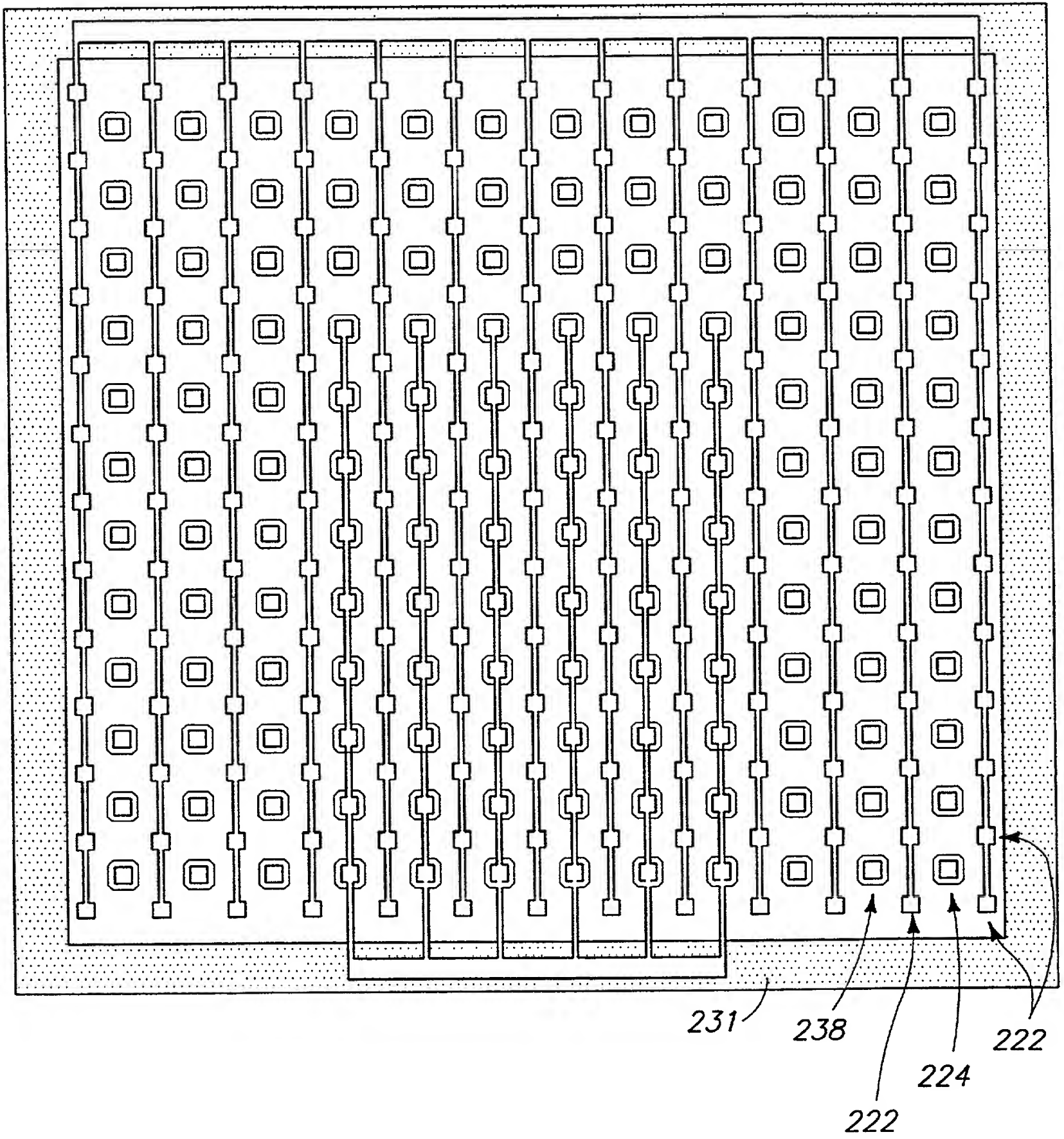
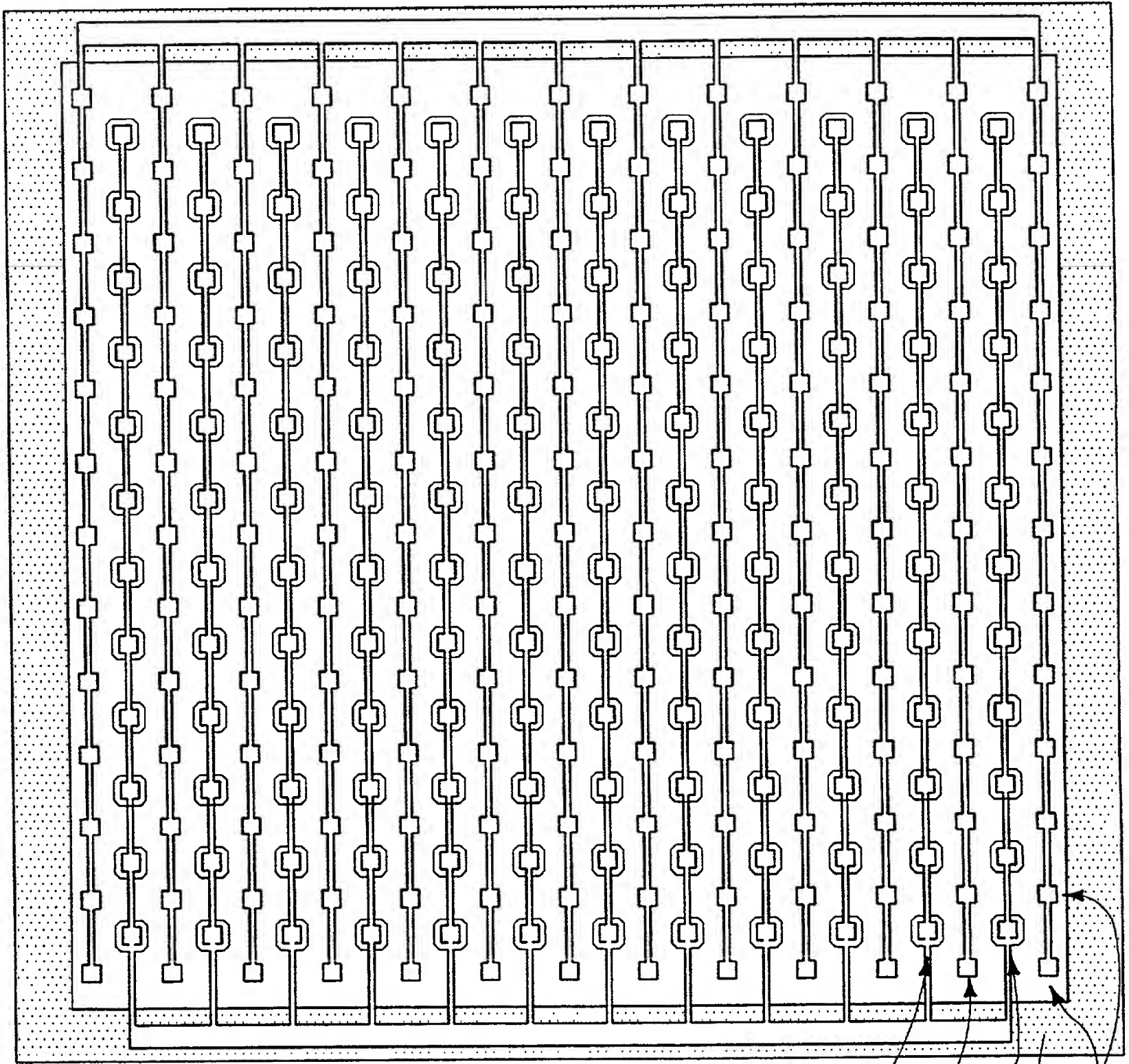


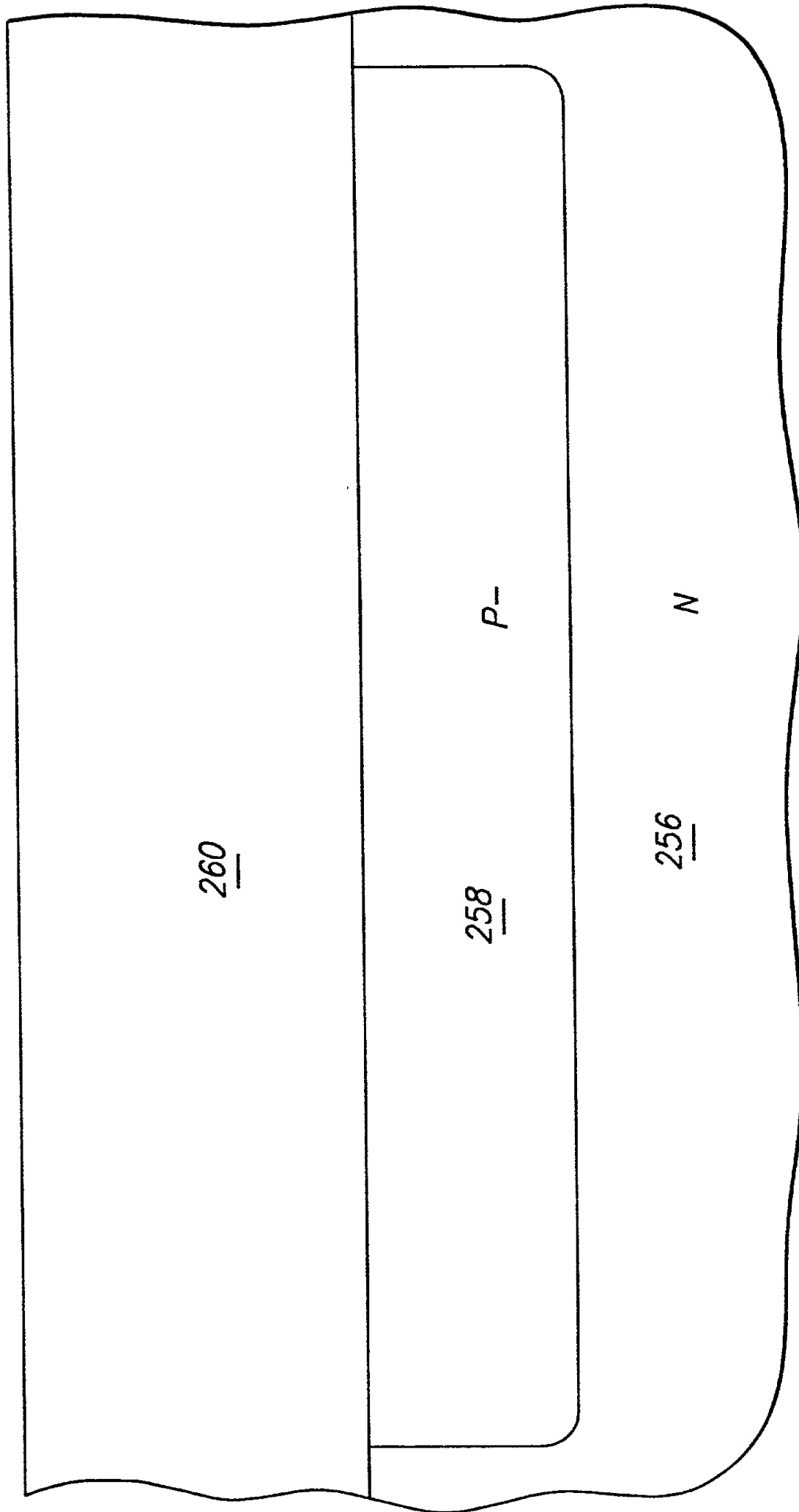
Figure 1



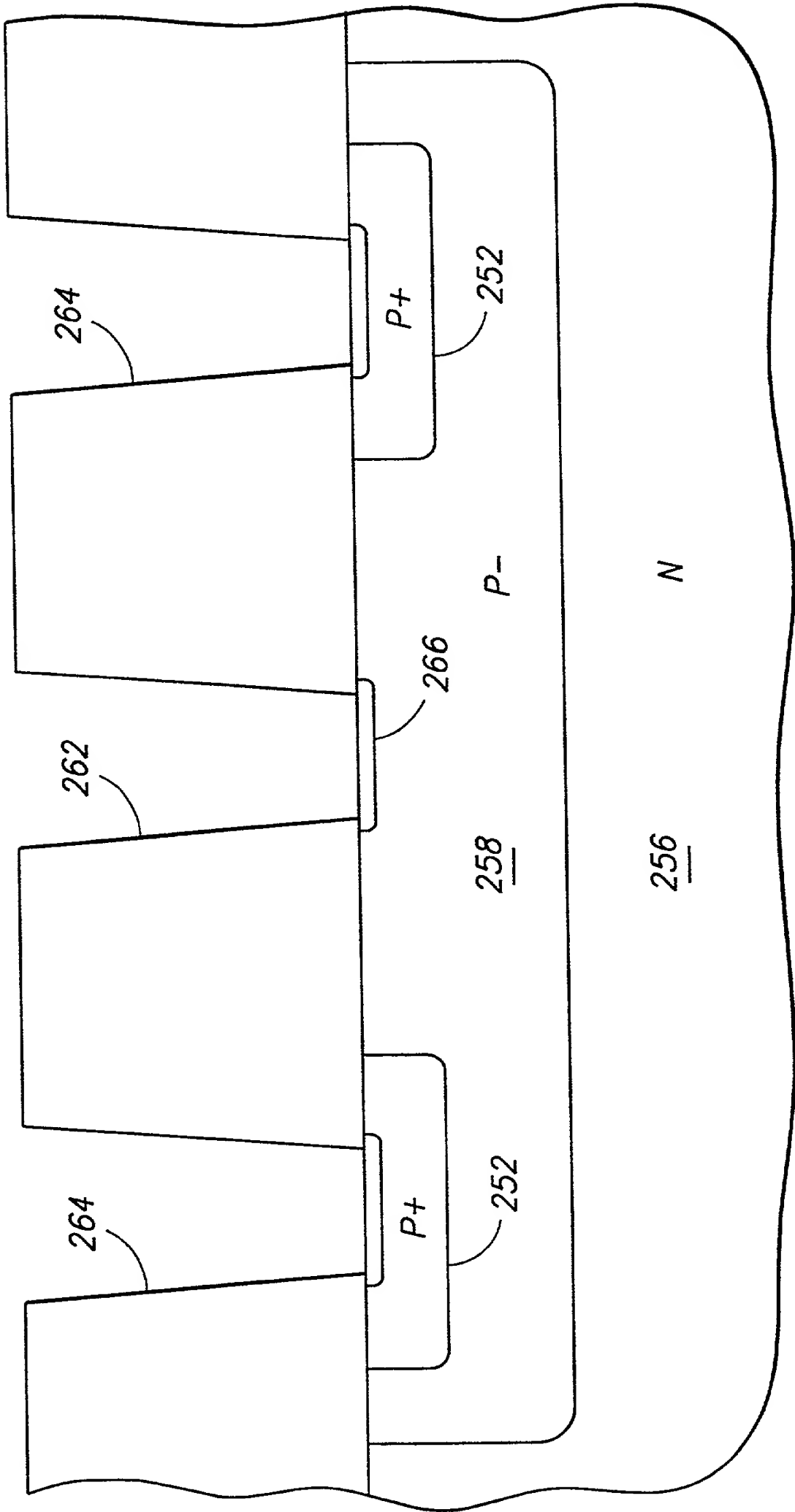
238
224
222
231
222

FIG. 10

FIG. 10 is a schematic diagram of a rectangular array of interconnected components. The array consists of 10 vertical columns and 10 horizontal rows. Each column contains a series of 10 square components, each with a smaller square inside. These components are connected by horizontal lines. Vertical lines connect the components in each column. The entire array is enclosed in a rectangular frame with a dotted border. Labels 222, 231, 224, and 238 are located at the bottom right of the diagram, with arrows pointing to specific components or lines.



IT II a-Ha-H



MI 40-030

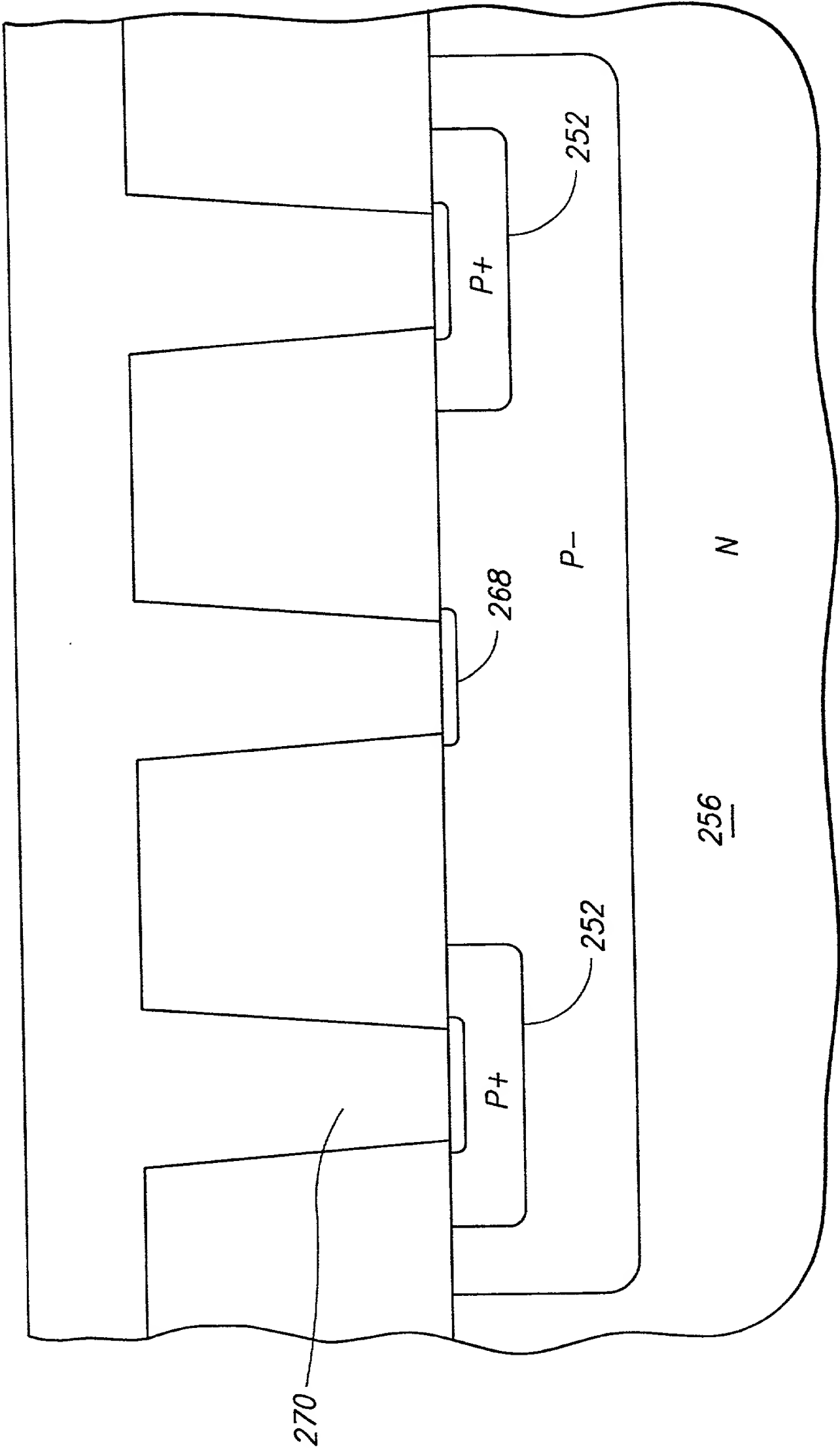
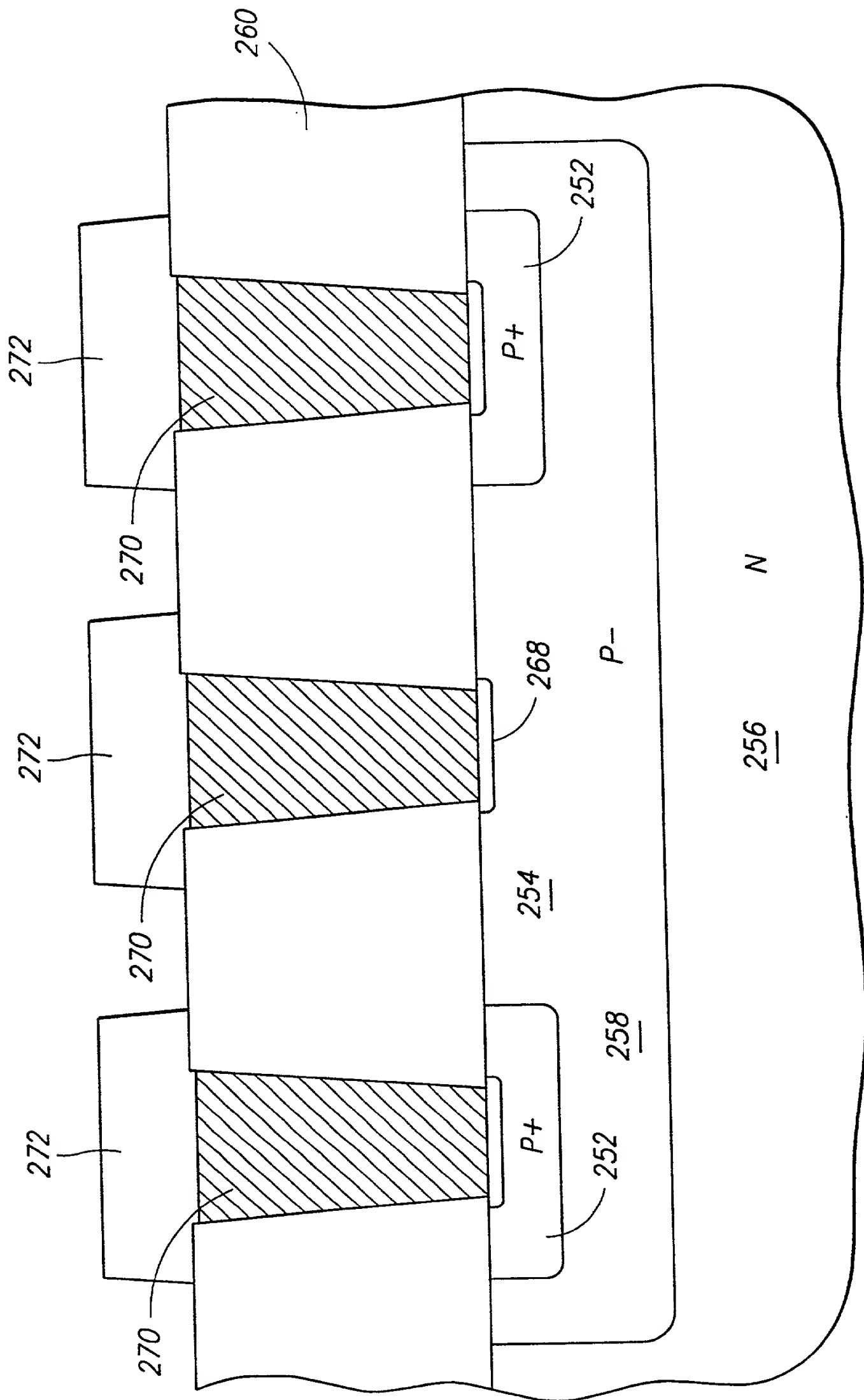


FIG. 10



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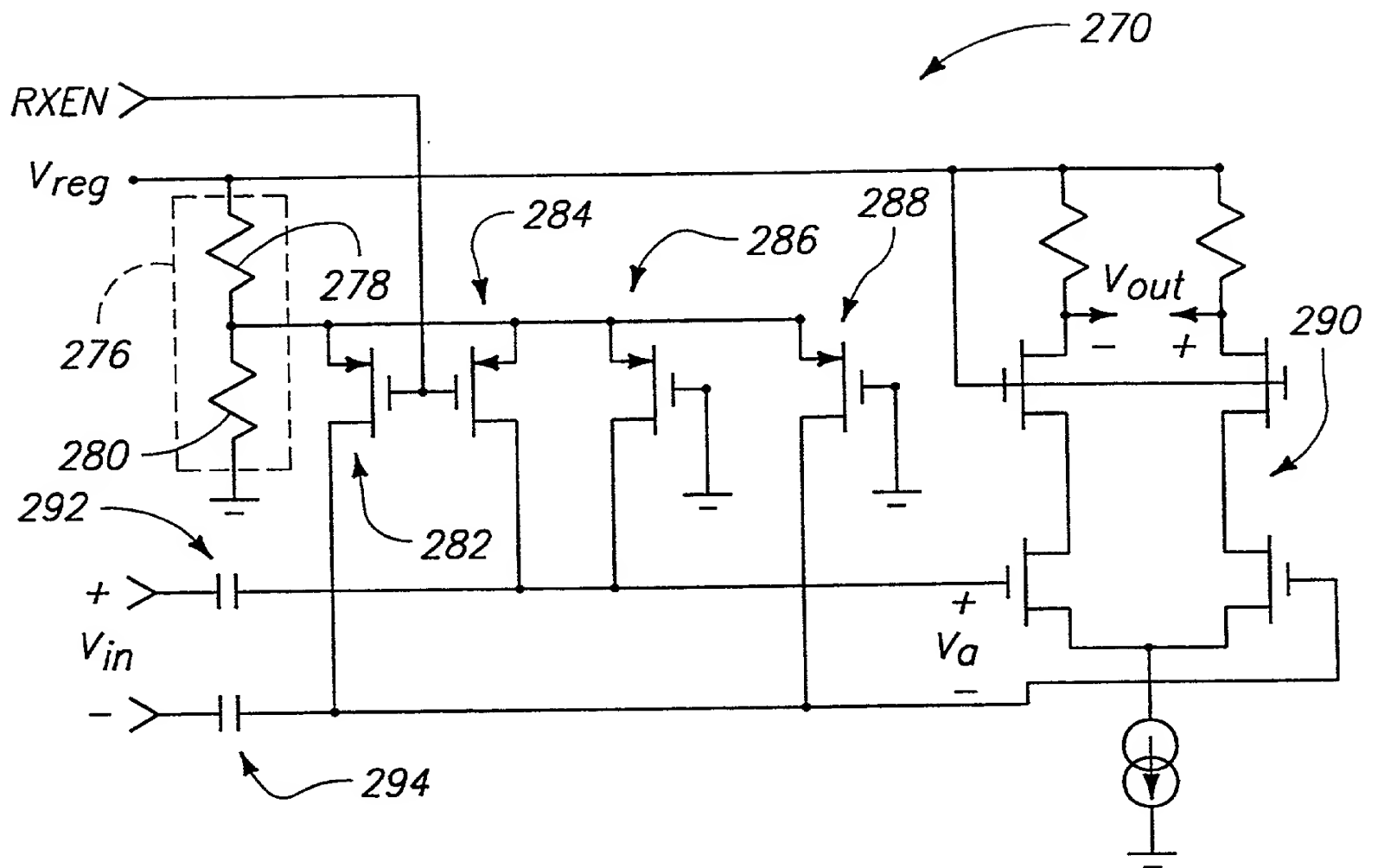


FIG. 2

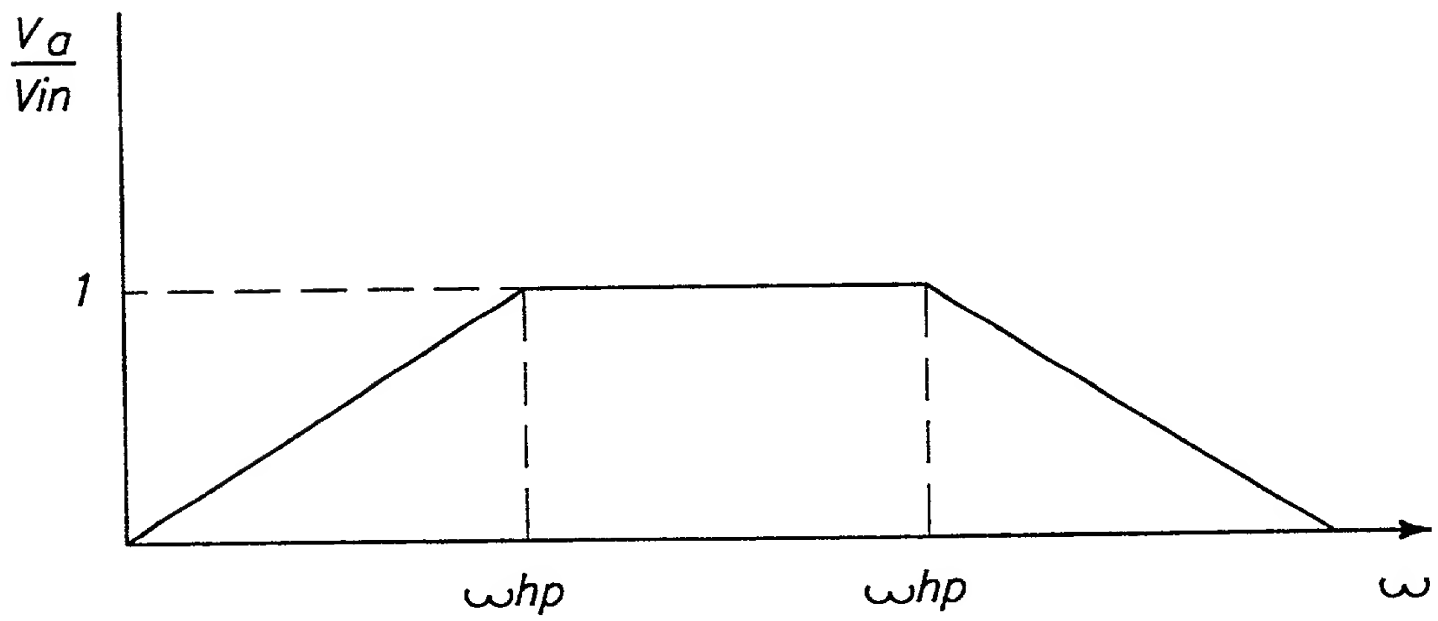


FIG. 3

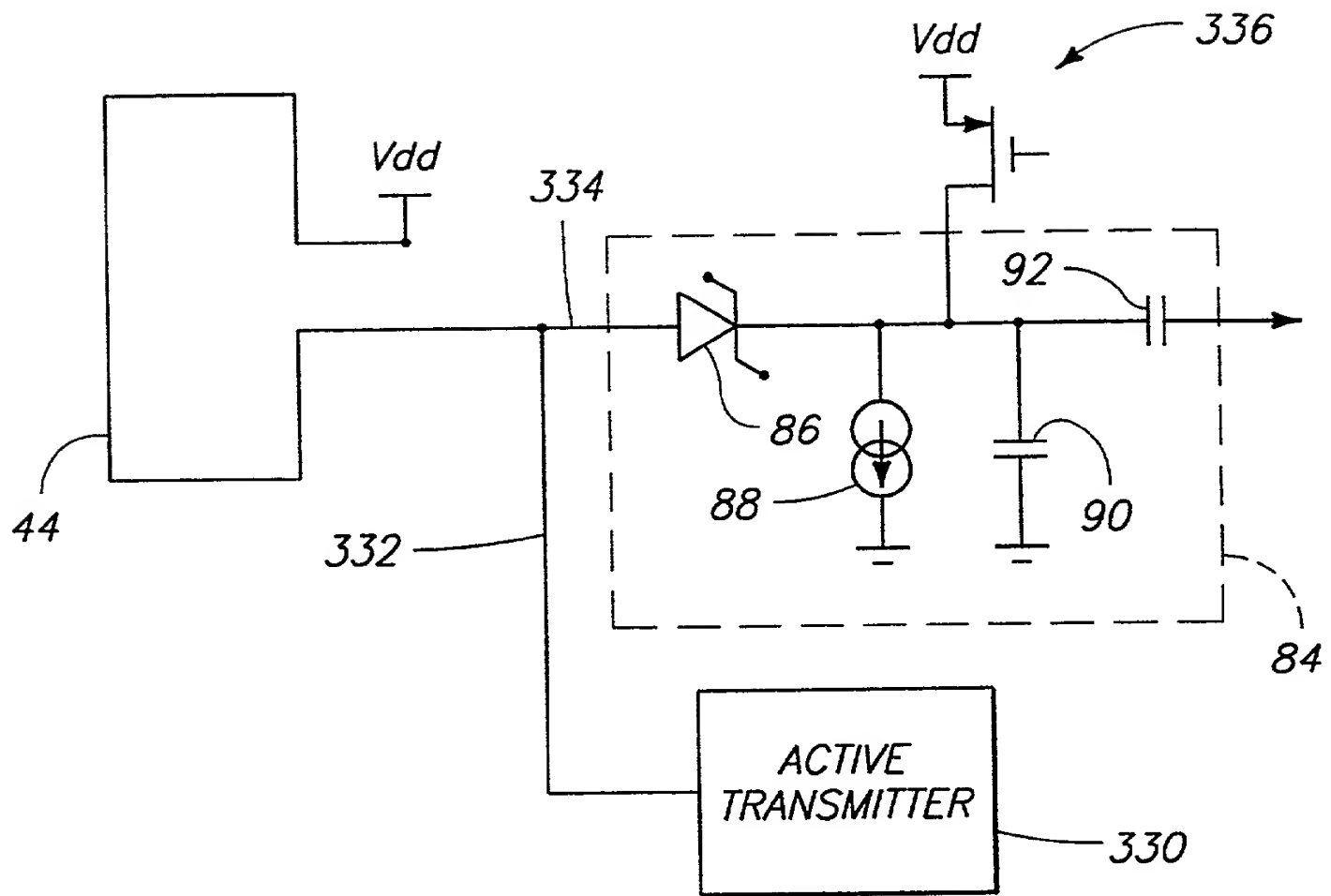


FIG. 50

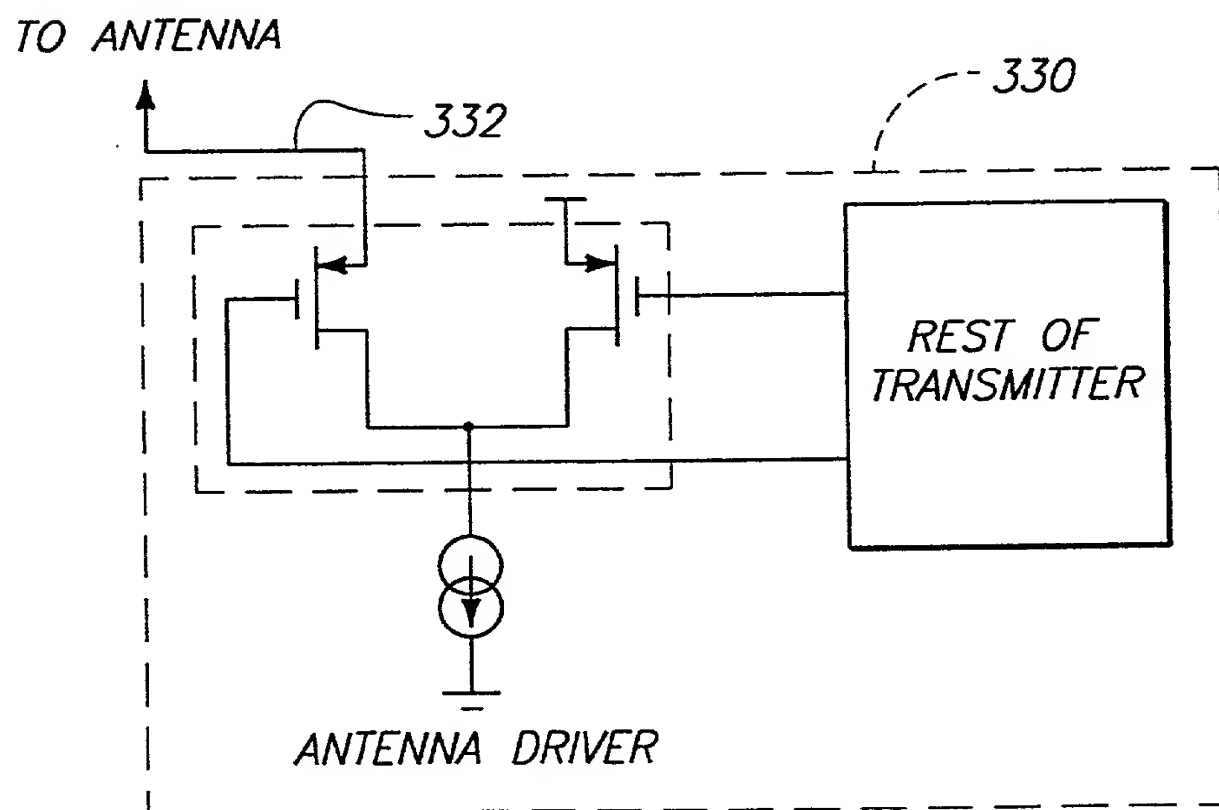


FIG. 51

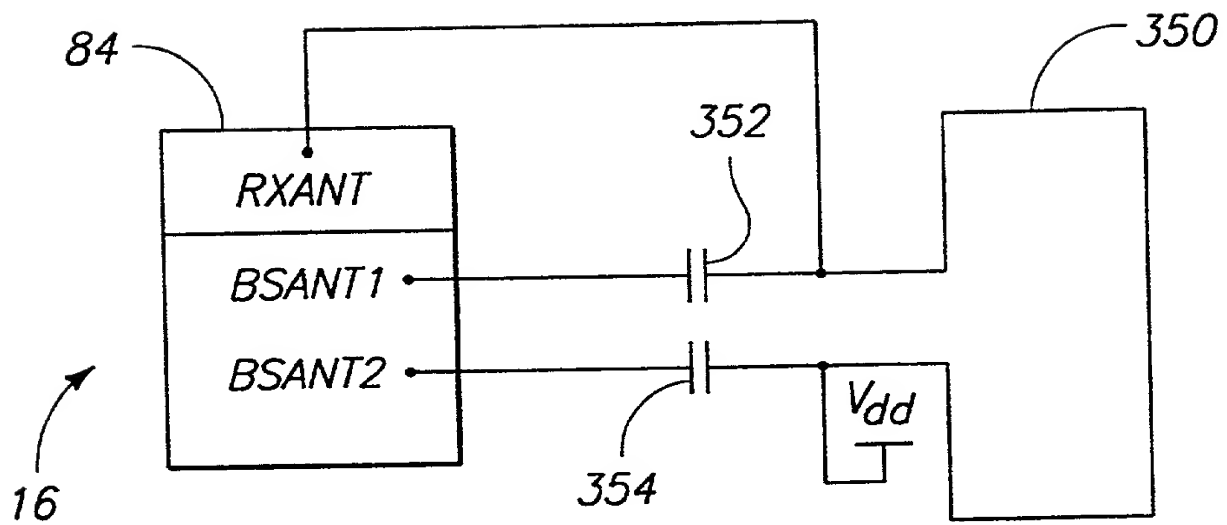


FIG. 5A

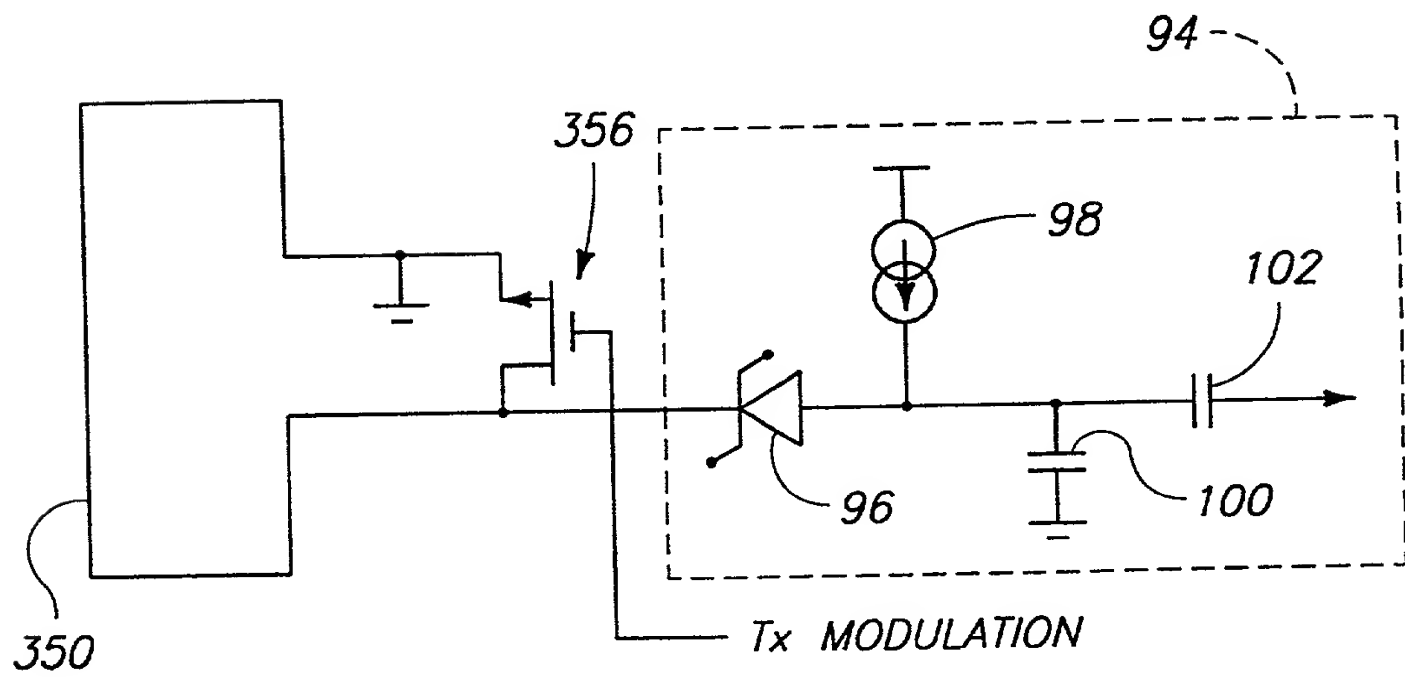
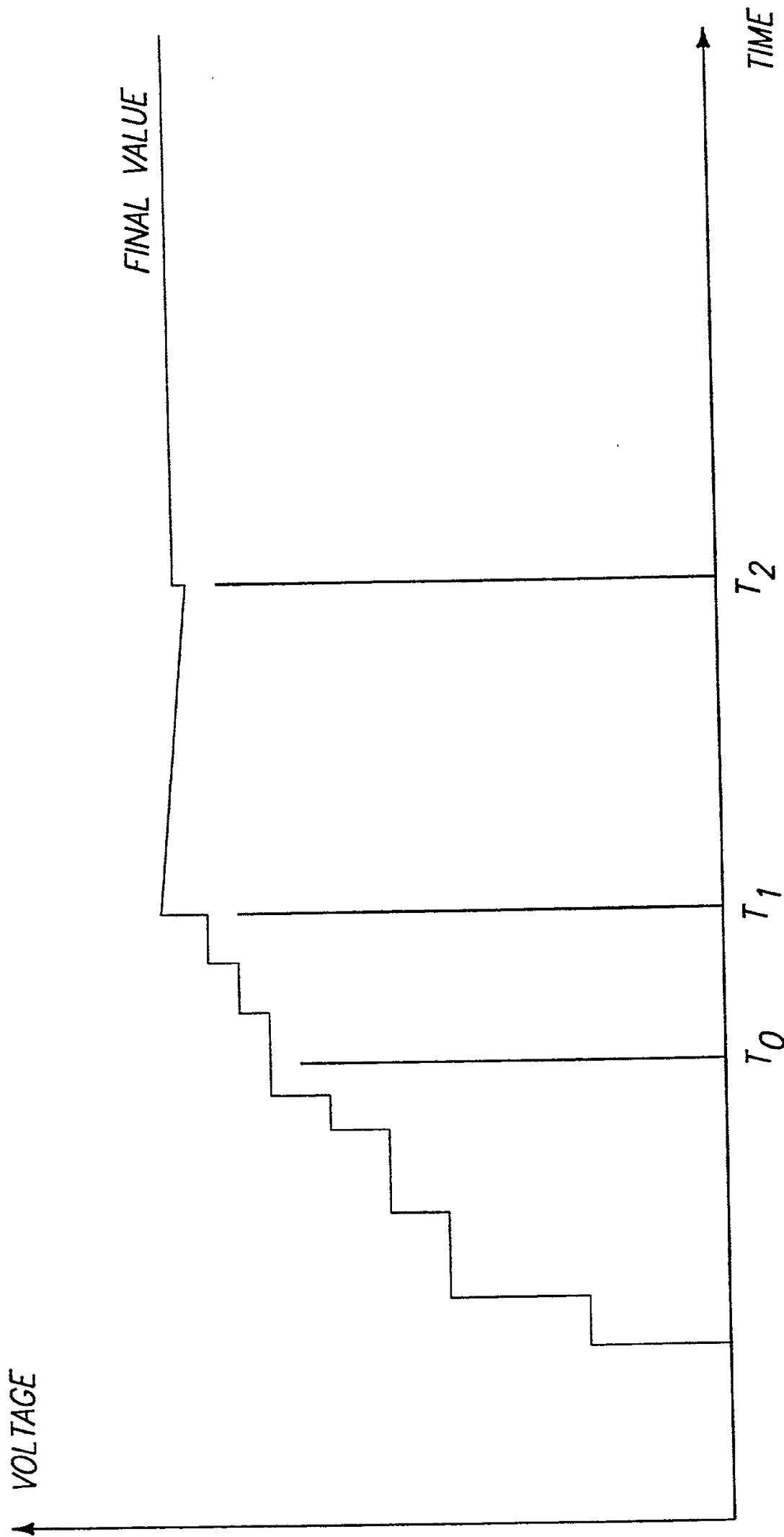
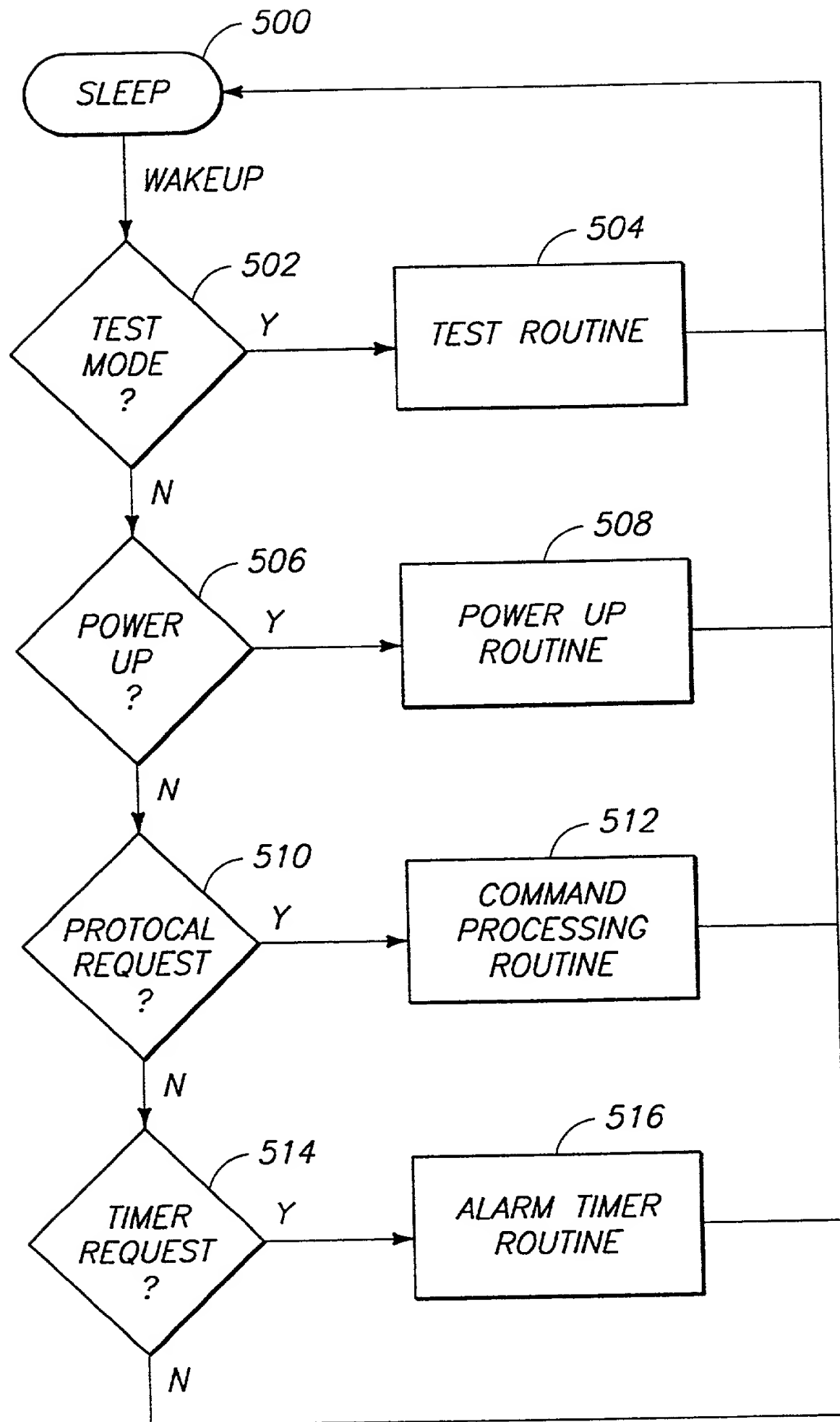
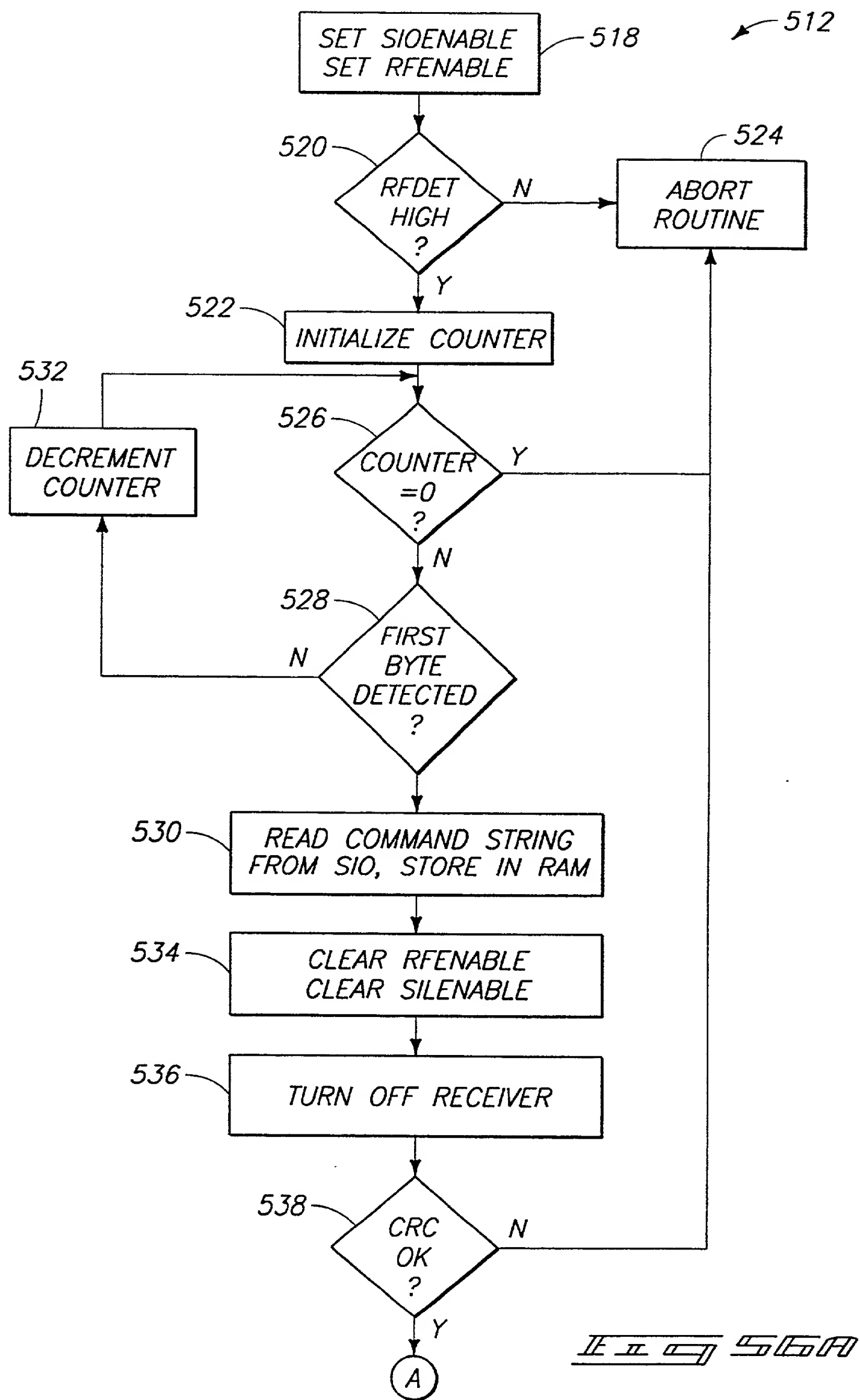


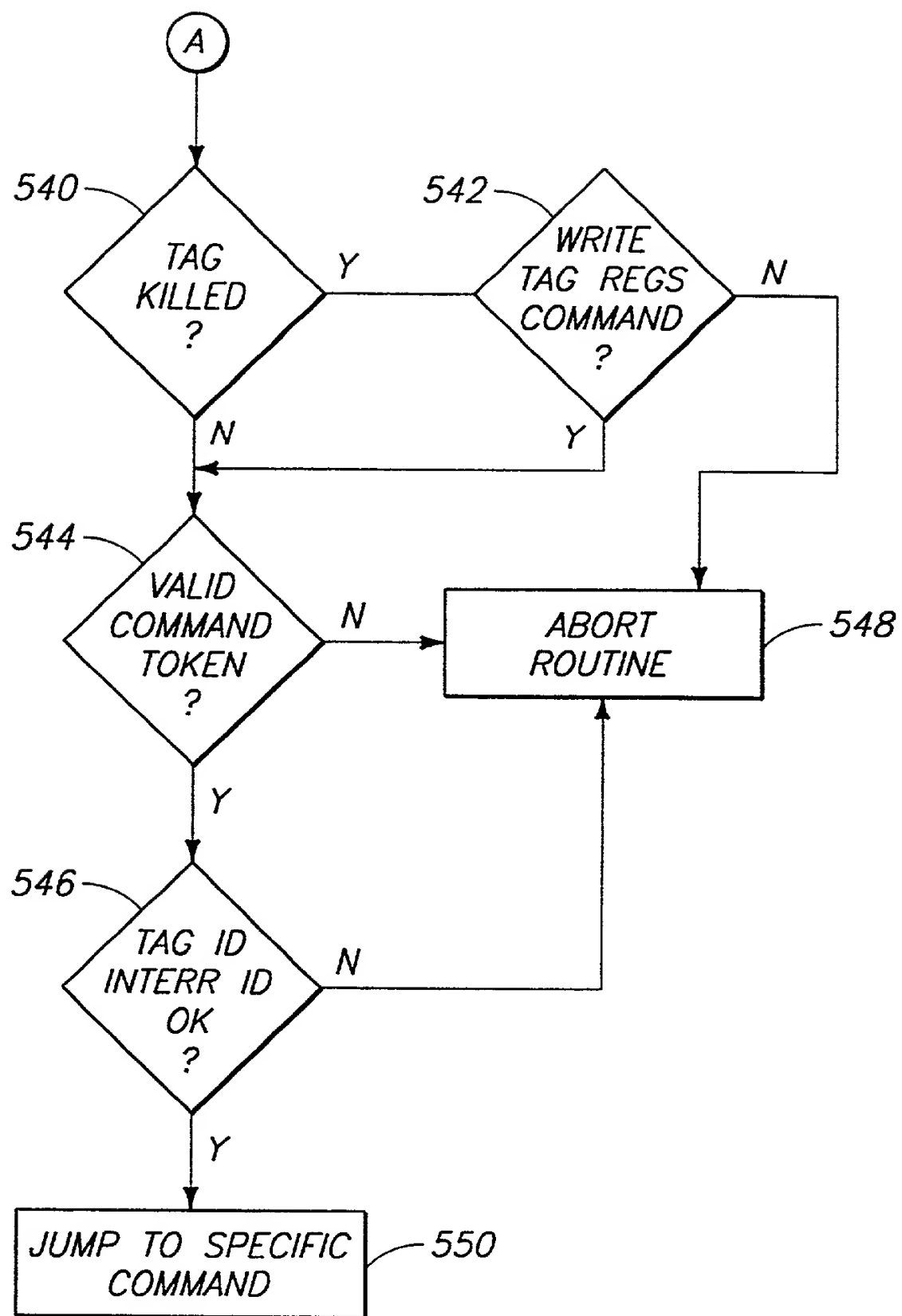
FIG. 5B

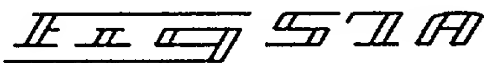


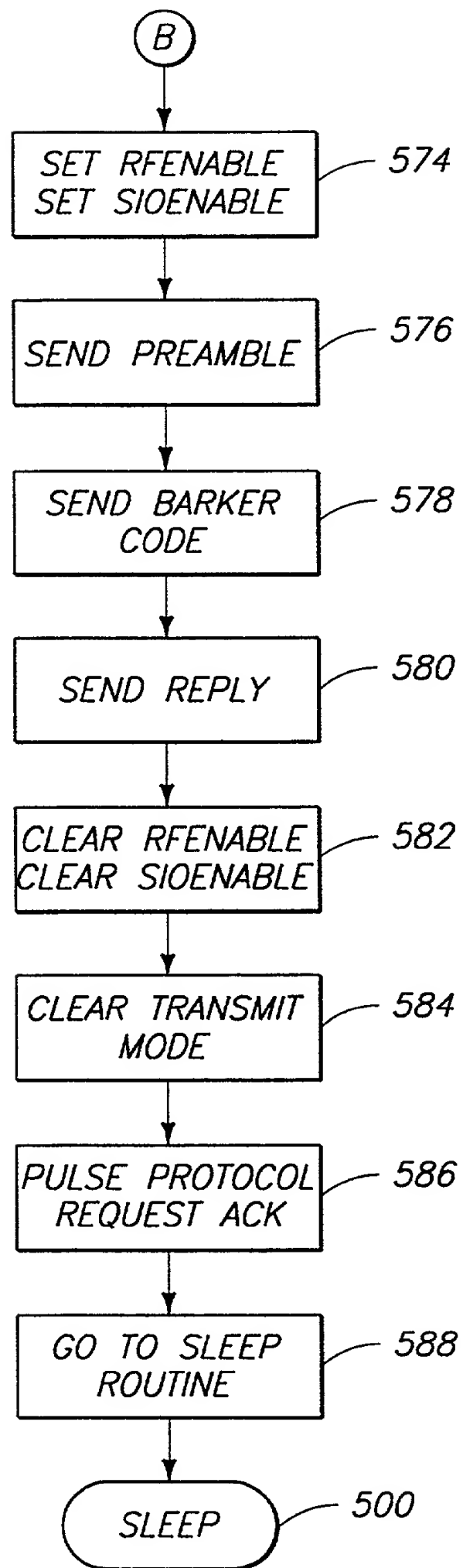
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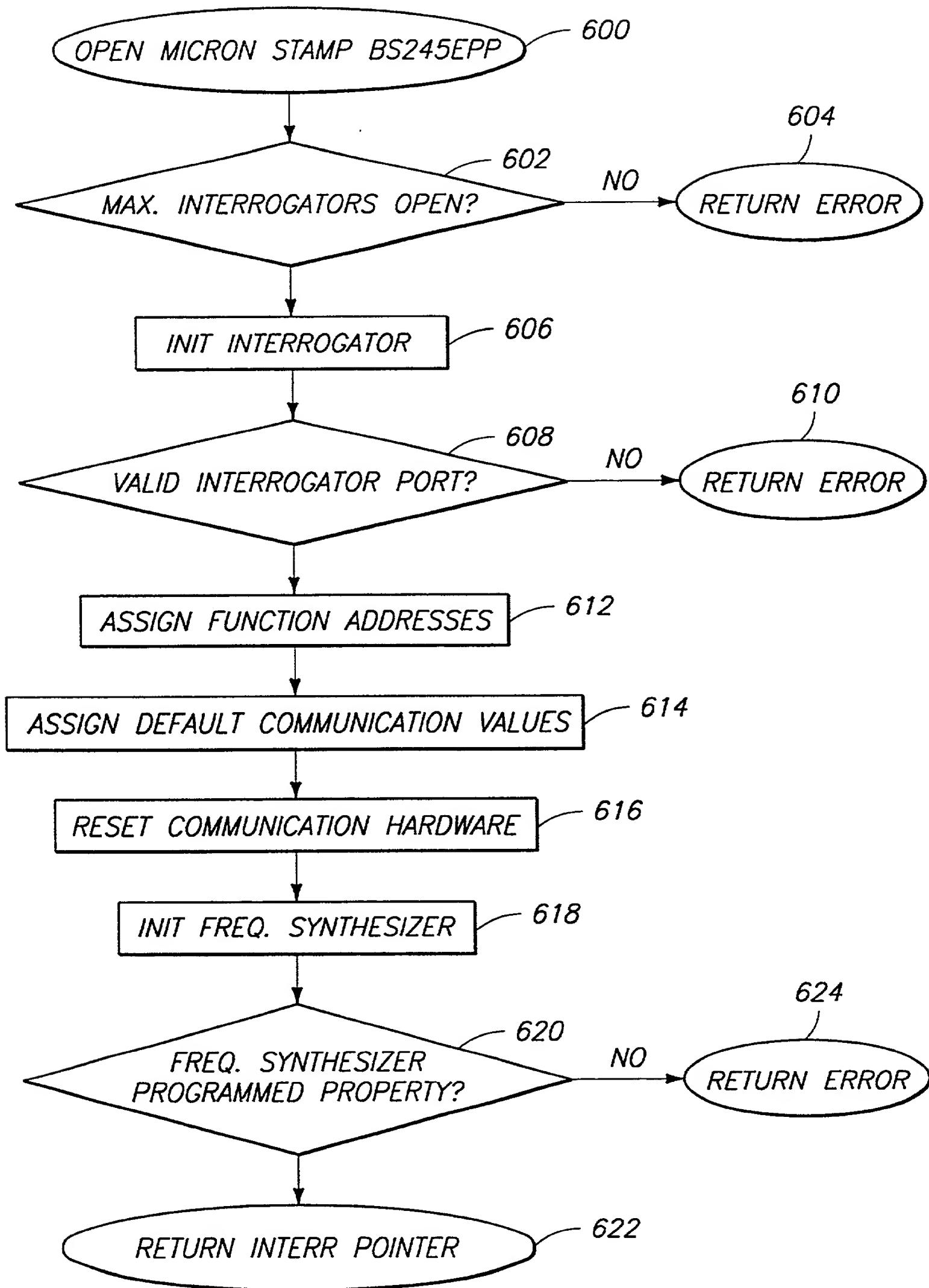


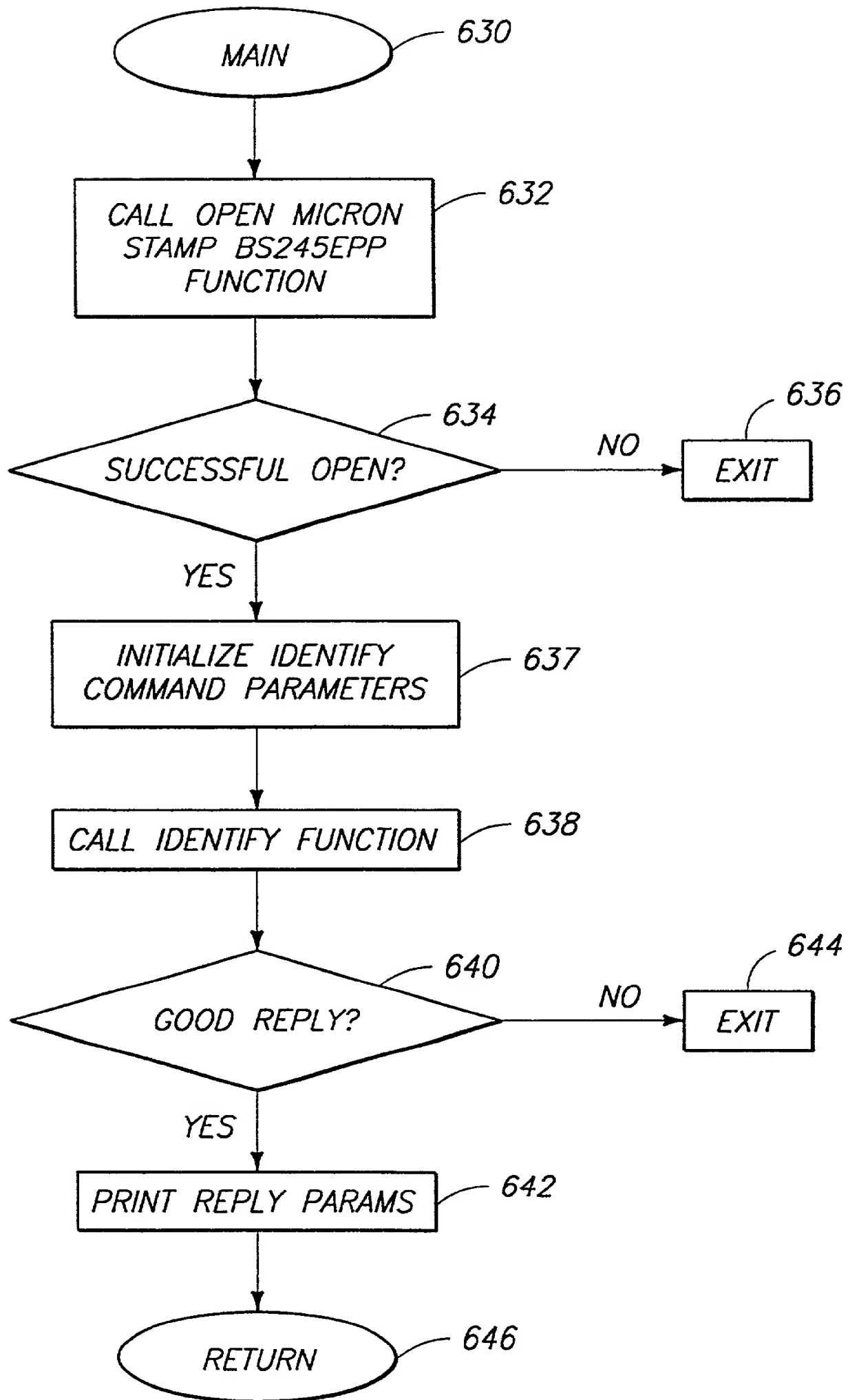


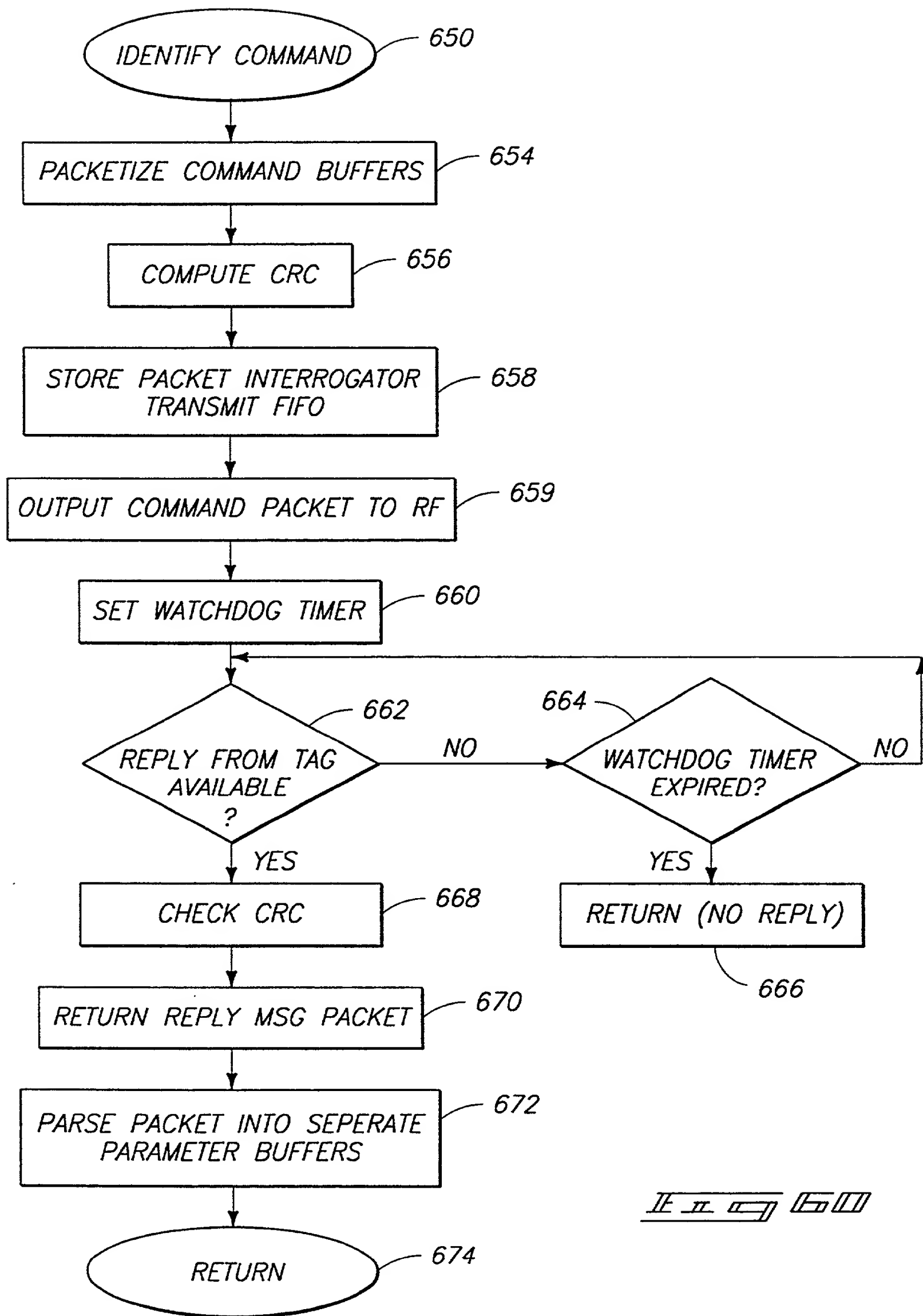


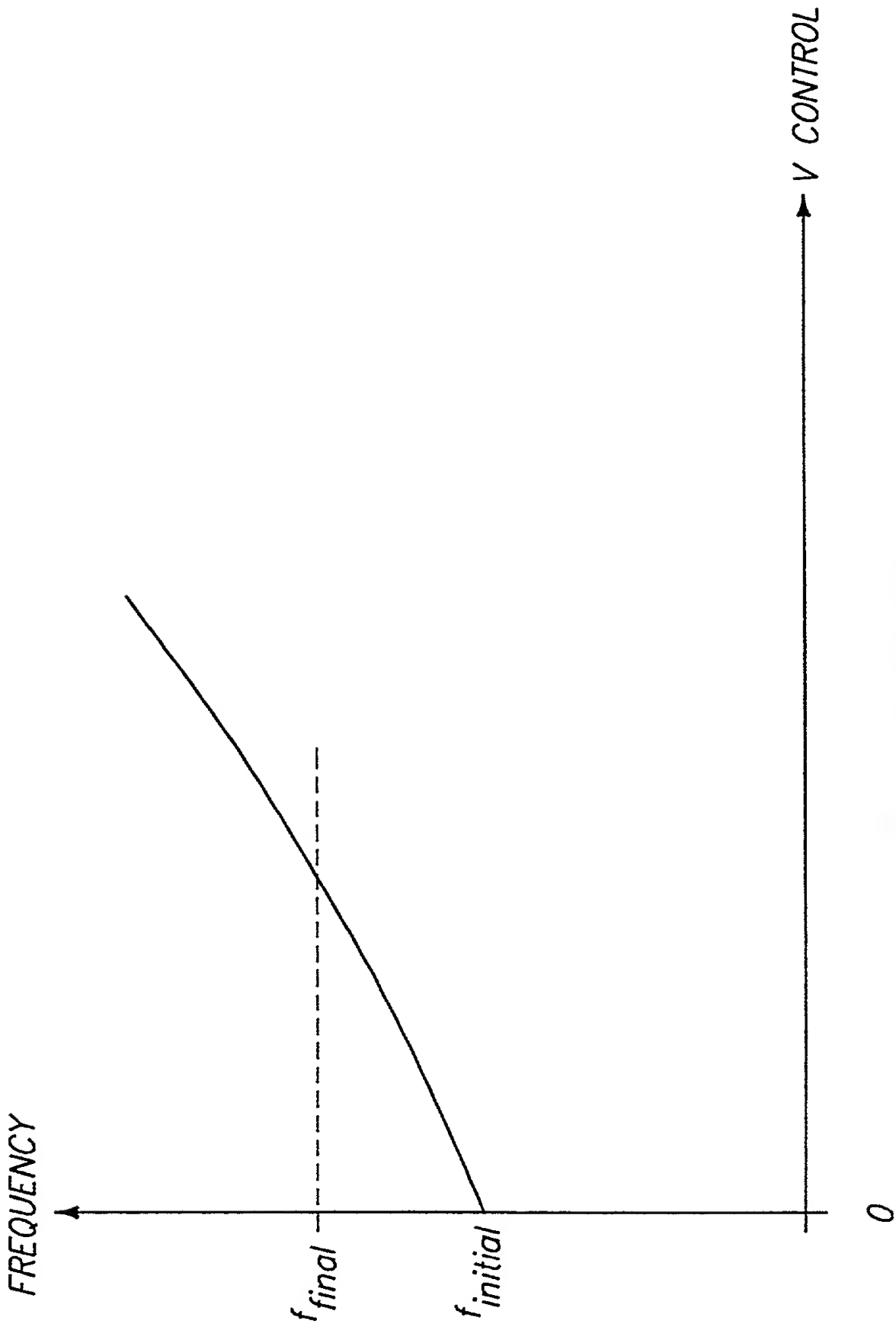




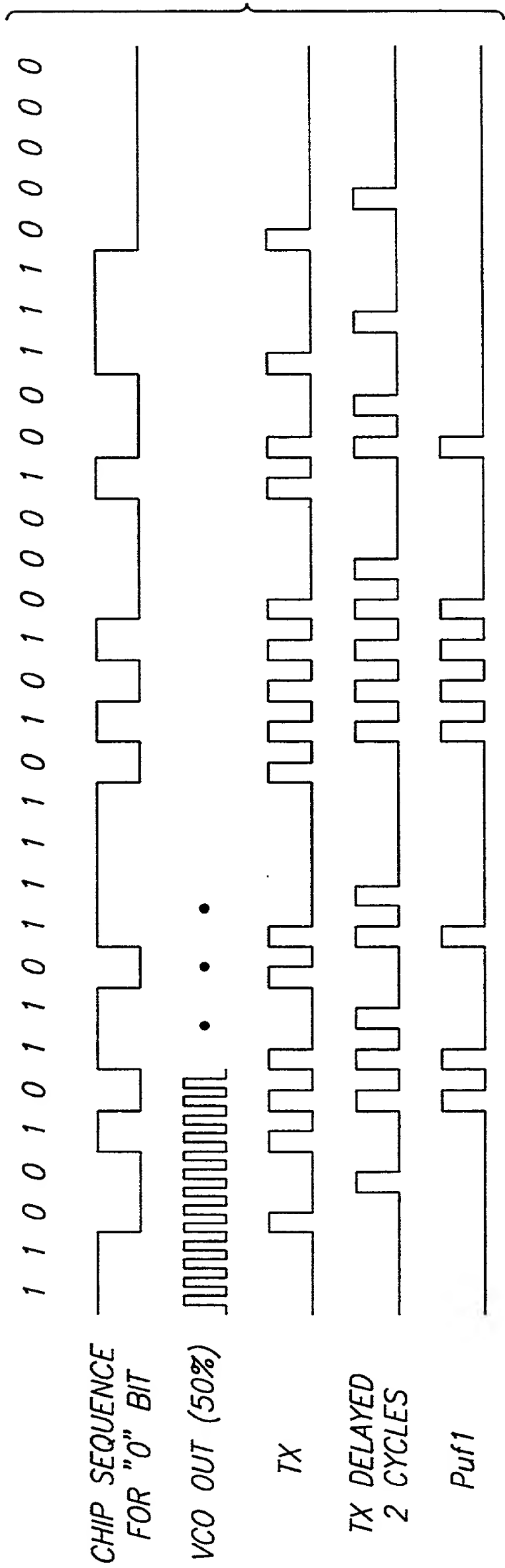




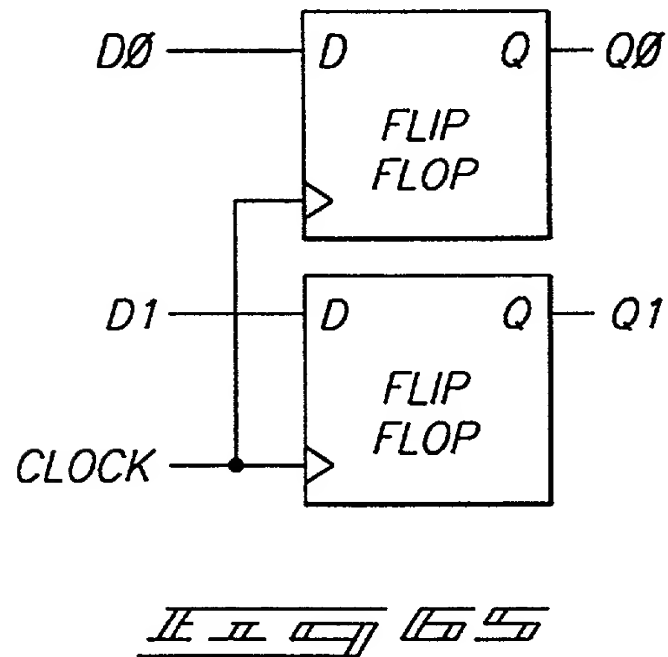
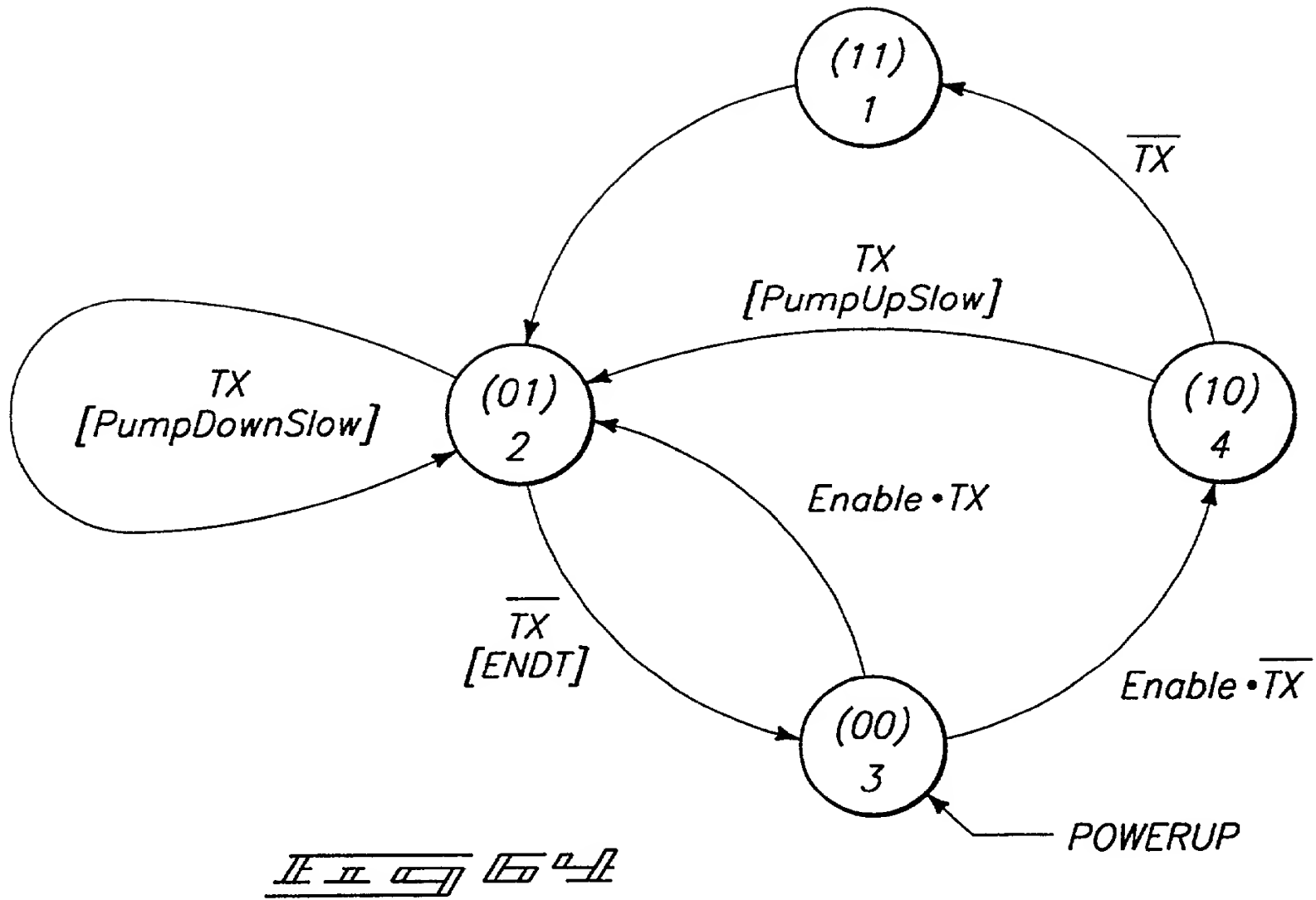
FIG. 6



SECRET



11001011011101010001000111000000



PRESENT STATE				NEXT STATE	
ENABLE	TX	Q1	Q0	D1	D0
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	1	0
1	1	0	0	0	1
X	0	0	1	0	0
X	1	0	1	0	1
X	X	1	1	0	1
X	0	1	0	1	1
X	1	1	0	0	1

II II II II

En TX

Q1 Q0

D0:

	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	1	1	1	1
10	0	0	1	1

II II II II II

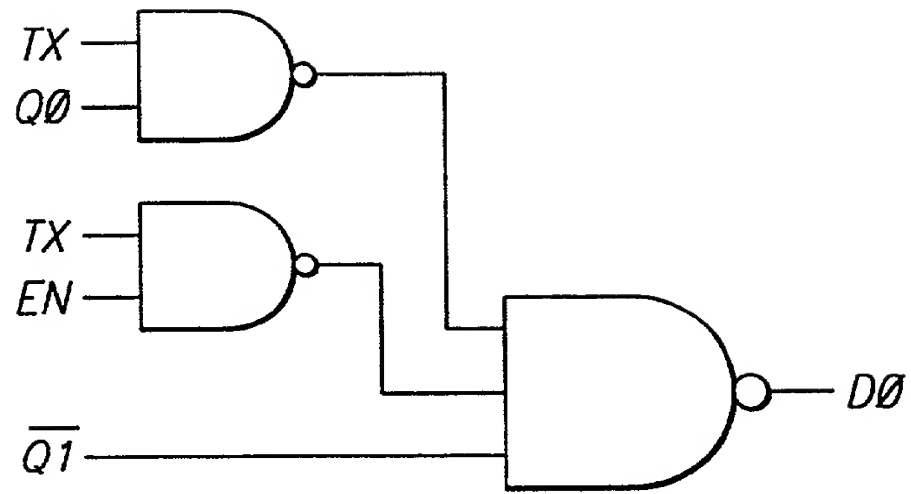
En TX

Q1 Q0

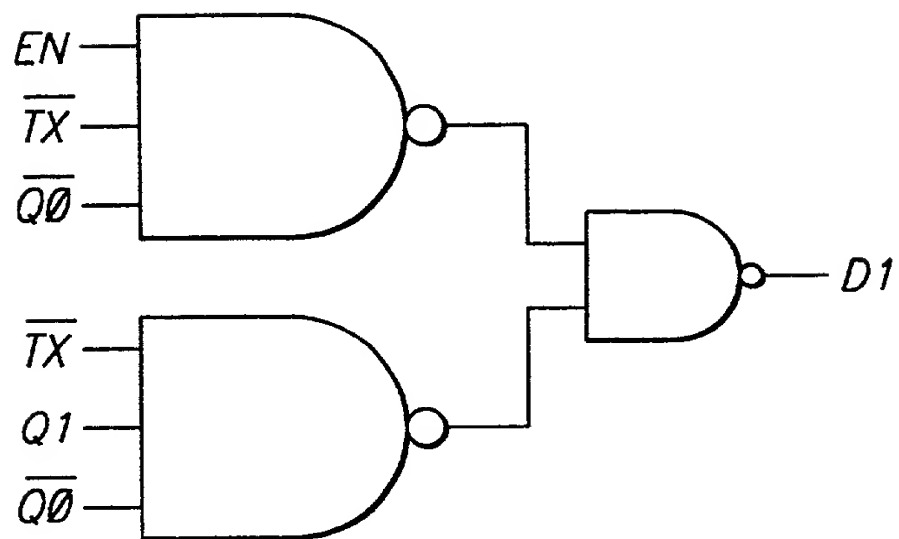
D1:

	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

II II II II II

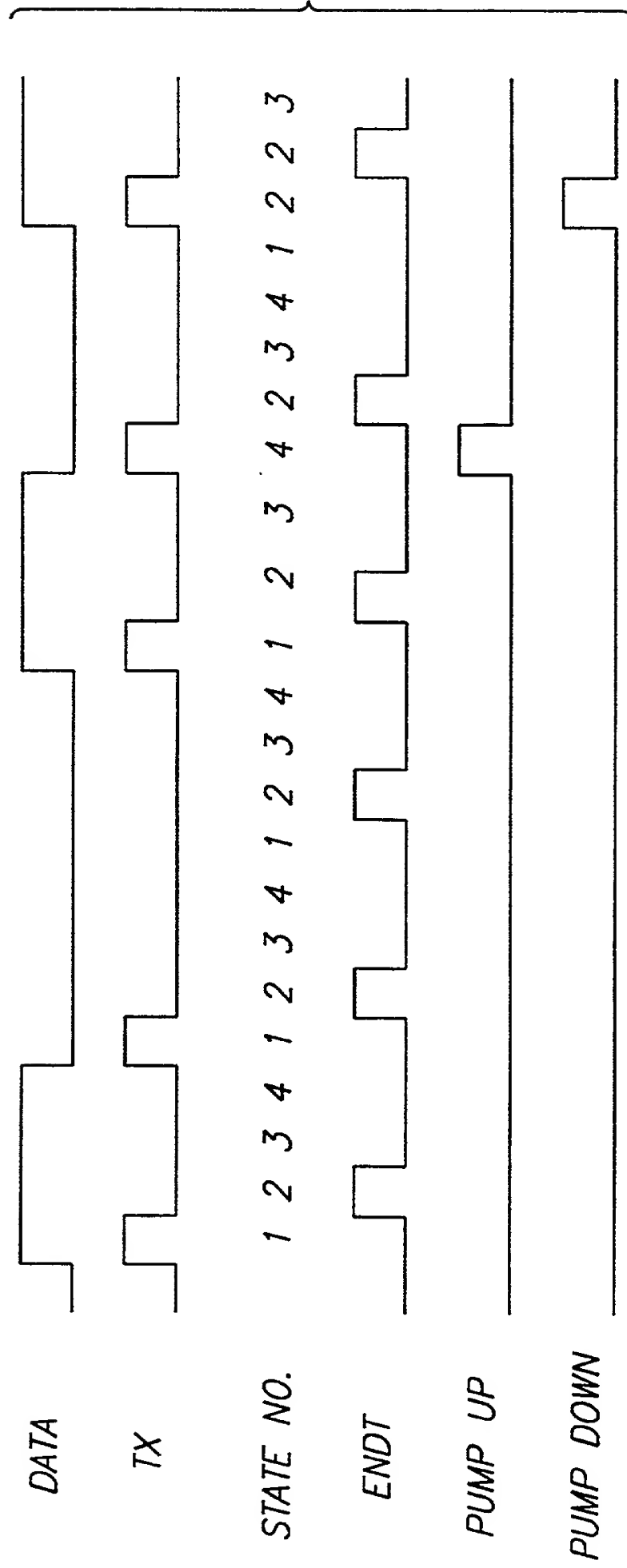


II II II II II



II II II II II

MI40-030



II II II II

1 **POWER OF ATTORNEY:**

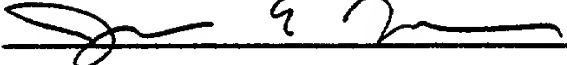
2 As a named Inventor, I hereby appoint the following attorneys and
3 agent to prosecute this application and transact all business in the
4 Patent and Trademark Office connected therewith: Richard J. St. John,
5 Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory,
6 Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg.
7 No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen,
8 Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G.
9 Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S.
10 Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D.
11 Shaurette, Reg. No. 39,833; W. Bryan Farney, Reg. No. 32,651; Lia M.
12 Pappas, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

13 Send correspondence to: WELLS, ST. JOHN, ROBERTS,
14 GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane,
15 WA 99204-0317. Direct telephone calls to: Deepak Malhotra,
16 (509) 624-4276.

17 I hereby declare that all statements made herein of my own
18 knowledge are true and that all statements made on information and
19 belief are believed to be true; and further that these statements were
20 made with the knowledge that willful false statements and the like so
21 made are punishable by fine or imprisonment, or both, under
22 Section 1001 of Title 18 of the United States Code and that such willful
23 false statement may jeopardize the validity of the application or any
24 patent issued therefrom.

* * * * *

Full name of inventor: **James E. O'Toole**

Inventor's Signature: 

Date: 9/26/96


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Citizenship: **U.S.A.**

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* * * * *

Full name of inventor: John R. Tuttle

Inventor's Signature: 

Date: 9-27-96

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Citizenship: U.S.A.

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Full name of inventor: Mark E. Tuttle

Inventor's Signature: Mark E. Tuttle

Date: 9-27-96

Residence: Boise, Idaho

Citizenship: U.S.A.

Post Office Address: 1998 Table Rock Road
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Full name of inventor: **Tyler Lowrey**

Inventor's Signature: *Tyler Lowrey*

Date: 10/14/96

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Citizenship: **U.S.A.**

Post Office Address: **2599 E. Plateau Drive
Boise, ID 83712**

* * * * *

Full name of inventor: Kevin M. Devereaux

Inventor's Signature: Kevin M. Devereaux

Date: 9/27/96

Residence: Boise, Idaho

Citizenship: U.S.A.

Post Office Address: 3593 Summerset Way
Boise, ID 83709

* * * * *

Full name of inventor: **George E. Pax**

Inventor's Signature: _____

George E. Pax

Date: 9-26-96


Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1201 E. Oakridge Drive
Boise, ID 83705**

* * * * *

Full name of inventor: **Brian P. Higgins**

Inventor's Signature: 

Date: 9/27/96

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1325 S. Owyhee Street
Boise, ID 83705**

* * * * *

Full name of inventor: **David K. Ovard**

Inventor's Signature: David K Ovard

Date: 9/27/96

Residence: **Meridian, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1019 E. Dominica
Meridian, ID 83642**

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Radio Frequency Data Communications Device**, Serial No. 08/705,043, filed August 29, 1996.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen,

1 Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G.
2 Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S.
3 Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D.
4 Shaurette, Reg. No. 39,833; W. Bryan Farney, Reg. No. 32,651; Lia M.
5 Pappas, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

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7 GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane,
8 WA 99204-0317. Direct telephone calls to: Deepak Malhotra
9 (509) 624-4276.

10 I hereby declare that all statements made herein of my own
11 knowledge are true and that all statements made on information and
12 belief are believed to be true; and further that these statements were
13 made with the knowledge that willful false statements and the like so
14 made are punishable by fine or imprisonment, or both, under
15 Section 1001 of Title 18 of the United States Code and that such willful
16 false statement may jeopardize the validity of the application or any
17 patent issued therefrom.

* * * * *

Full name of sole inventor: **Shu-Sun Yu**

Inventor's Signature: *Shu Sun Yu*

Date: 10/28/96

Residence: **Boise, Idaho**

Citizenship: **R.O.C.**

Post Office Address: **275 W. Groveview Lane
Boise, ID 83702**

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Radio Frequency Data Communications Device**, Serial No. 08/705,043, filed August 29, 1996.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

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1 Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G.
2 Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S.
3 Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D.
4 Shaurette, Reg. No. 39,833; W. Bryan Farney, Reg. No. 32,651; Lia M.
5 Pappas, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

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7 GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane,
8 WA 99204-0317. Direct telephone calls to: Deepak Malhotra
9 (509) 624-4276.

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13 made with the knowledge that willful false statements and the like so
14 made are punishable by fine or imprisonment, or both, under
15 Section 1001 of Title 18 of the United States Code and that such willful
16 false statement may jeopardize the validity of the application or any
17 patent issued therefrom.

* * * * *

Full name of sole inventor: Robert R. Rotzoll

Inventor's Signature: Robert R. Rotzoll

Date: October 25, 1996

Residence: Colorado Springs, Colorado

Citizenship: U.S.

Post Office Address: ~~6040 Navajo Trail~~
~~Colorado Springs, CO 80809~~

6040 Navajo Trail
Chipita Park, CO 80809
RRR 10/25/96

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Priority Application Serial No. 09/152,662
3 Priority Filing Date September 14, 1998
4 Inventor James E. O'Toole et al.
5 Assignee Micron Technology, Inc.
6 Priority Group Art Unit 2817
7 Priority Examiner Steven Mottola
8 Attorney's Docket No. MI40-273
9 Title: Method of Speeding Power-Up of an Amplifier, and Amplifier

10
11 _____
12
13 Assistant Commissioner for Patents

14 Washington, D.C. 20231

15 **ASSOCIATE POWER OF ATTORNEY**

16 Please recognize Frederick M. Fliegel, Reg. No. 36,138; Donald B. Kenady, Reg.
17 No. 40,045; James E. Lake, Reg. No. 44,854; and Bernard Berman, Reg. No. 37,279,
18 whose post office address is 601 W. First Avenue, Suite 1300, Spokane,
19 Washington 99201-3828, as associate attorneys or agents in the above-entitled
20 application.

21 Date: February 11, 2000

22 Deepak Malhotra

23 Deepak Malhotra
 Reg. No. 33,560